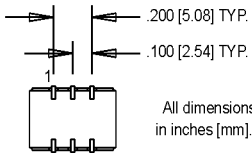
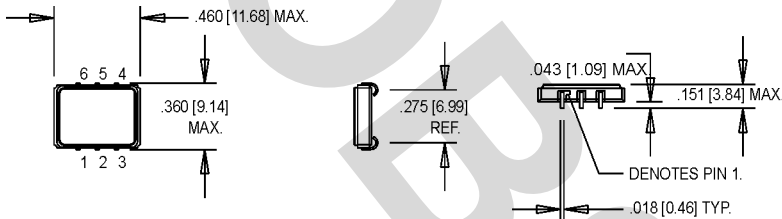


# K1526B & K1536B Series

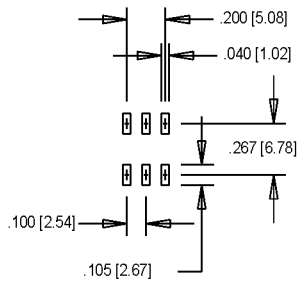
## 9x11 mm, 5.0 or 3.3 Volt, CMOS/TTL, VCXO



- Former **Champion TECHNOLOGIES, INC.** Product
- Phase-Locked Loops (PLL's), Clock Recovery, Reference Signal Tracking, Synthesizers, Frequency Modulation/Demodulation



SUGGESTED SOLDER PAD LAYOUT



### Pin Connections

PIN	FUNCTION
1	Voltage Control
2	Tristate
3	Ground & Gnd Plane
4	Output
5	N/C
6	+Vdd

**Ordering Information**

**K15X6BX X X 00.0000 MHz**

**Product Series**  
 K1526B = 5.0 Volt  
 K1536B = 3.3 Volt

**Model Selection:**  
 See Electrical Specs

**Temperature Range**  
**Blank:** 0°C to +70°C  
**M:** -40°C to +85°C

**Symmetry/Logic Compatibility**  
**Blank:** TTL/CMOS 40%/60%  
**C:** CMOS 45%/55%  
**T:** TTL 45%/55%

**Frequency (customer specified)**

PARAMETER	Symbol				Units		
<b>Model</b>		K1526BA K1536BA	K1526BD K1536BD	K1526BE			
<b>Frequency Range</b>	F	2 to 55	55.1 to 80	2 to 55	2 to 40		
<b>Frequency Stability:</b> Overall	$\Delta F/F$	Inclusive of Calibration, Temperature, Voltage, Load, and Aging					
0°C to +70°C		±25	±40	±25	±32		
-40°C to +85°C		±50	±60	±50	±50		
<b>Pullability</b> Minimum		±100	±80	±80	±200		
Maximum		±150	±160	±130			
<b>PARAMETER</b>	<b>Symbol</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Units</b>	<b>Condition/Notes</b>	
<b>Operating Temperature</b>	T <sub>A</sub>	(See Ordering Information)					
<b>Storage Temperature</b>	T <sub>s</sub>	-40		+125	°C		
<b>Aging</b> 1st Year		-3/-5		+3/+5	ppm	< 52 MHz / ≥ 52 MHz	
Thereafter (per year)		-1/-2		+1/+2	ppm	< 52 MHz / ≥ 52 MHz	
<b>Control Voltage</b>	V <sub>c</sub>	0.5 0.3 0	2.5 1.65	4.5 3.0 5.0	V	K1526B K1536B K1526BE	
<b>Linearity</b>				10	%	Positive Monotonic Slope	
<b>Modulation Bandwidth</b>	f <sub>m</sub>	20			kHz	+3 dB	
<b>Input Impedance</b>	Z <sub>in</sub>	50k			Ohms	@ 10 kHz	
<b>Input Voltage</b>	V <sub>dd</sub>	4.5 3.0	5.0 3.3	5.5 3.6	V	K1526B K1536B	
<b>Input Current</b>	I <sub>dd</sub>			30	mA		
<b>Output Type</b>						CMOS/TTL	
<b>Load</b>				15	pF	HCMOS	
<b>Symmetry (Duty Cycle)</b>		(See Ordering Information)					
<b>Logic "1" Level</b>	V <sub>oh</sub>	V <sub>dd</sub> - 0.5			V		
<b>Logic "0" Level</b>	V <sub>ol</sub>			0.5	V		
<b>Output Current</b>				20	mA		
<b>Rise/Fall Time</b>	T <sub>r</sub> /T <sub>f</sub>			5	ns	20% to 80% V <sub>dd</sub> , C <sub>L</sub> = 15 pF	
<b>Tristate Function</b>		Input Logic "1" or floating: output active Input Logic "0": output disables to high-Z					
<b>Start up Time</b>				10	ms		
<b>Phase Jitter @ 26 MHz</b>	φ <sub>J</sub>		4		ps RMS	Integrated 12 kHz - 20 MHz	
<b>Phase Noise (Typical) @ 26 MHz</b>		100 Hz -65	1 kHz -95	10 kHz -115	100 kHz -130	100 kHz -140	Offset from carrier dBc/Hz

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# MtronPTI Lead Free Solder Profile

