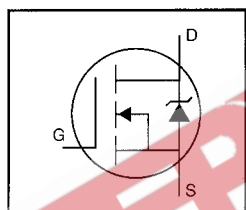


HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements

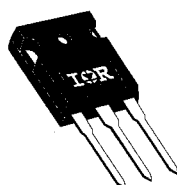


$V_{DSS} = 600V$
 $R_{DS(on)} = 0.40\Omega$
 $I_D = 16A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.



TO-247AC

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Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	16	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	10	
I_{DM}	Pulsed Drain Current ①	64	
$P_D @ T_C = 25^\circ C$	Power Dissipation	280	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	1000	mJ
I_{AR}	Avalanche Current ①	16	A
E_{AR}	Repetitive Avalanche Energy ①	28	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	40	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

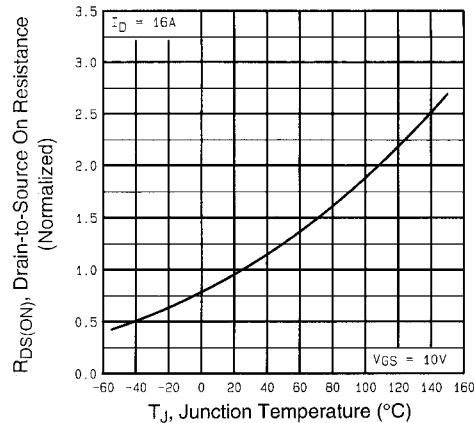
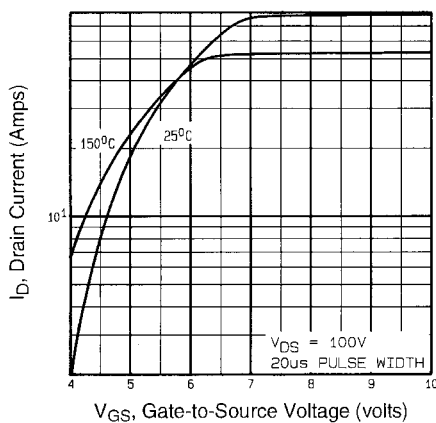
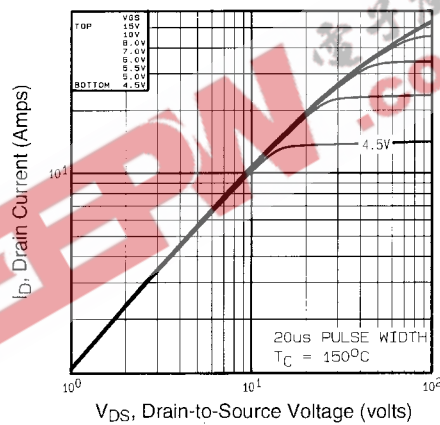
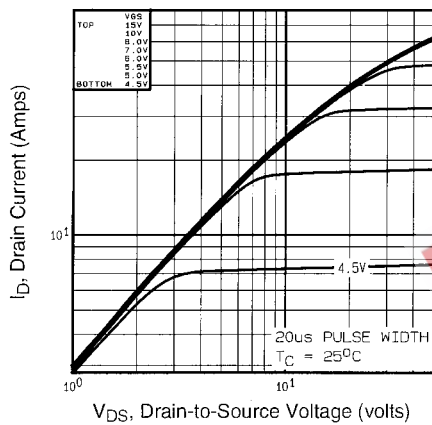
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	600	—	—	V	V _{GS} =0V, I _D =250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.83	—	V/°C	Reference to 25°C, I _D =1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.40	Ω	V _{GS} =10V, I _D =9.6A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
g _{fs}	Forward Transconductance	13	—	—	S	V _{DS} =50V, I _D =9.6A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	100	μA	V _{DS} =600V, V _{GS} =0V
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{DS} =480V, V _{GS} =0V, T _J =125°C
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V _{GS} =20V
Q _g	Total Gate Charge	—	—	210	nC	V _{DS} =360V
Q _{gs}	Gate-to-Source Charge	—	—	26	nC	V _{GS} =10V See Fig. 6 and 13 ④
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	110	nC	
t _{d(on)}	Turn-On Delay Time	—	19	—	ns	V _{DS} =300V
t _r	Rise Time	—	54	—	ns	I _D =16A
t _{d(off)}	Turn-Off Delay Time	—	110	—	ns	R _G =4.5Ω
t _f	Fall Time	—	56	—	ns	R _D =18Ω See Figure 10 ④
L _D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	13	—	nH	
C _{iss}	Input Capacitance	—	3900	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	440	—	pF	V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	98	—	pF	f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	16	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	64	A	
V _{SD}	Diode Forward Voltage	—	—	1.8	V	T _J =25°C, I _S =16A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	610	920	ns	T _J =25°C, I _F =16A
Q _{rr}	Reverse Recovery Charge	—	6.6	9.9	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V_{DS}=50V, starting T_J=25°C, L=7.2mH R_G=25Ω, I_{AS}=16A (See Figure 12)
- ③ I_{SD}≤16A, di/dt≤140A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.



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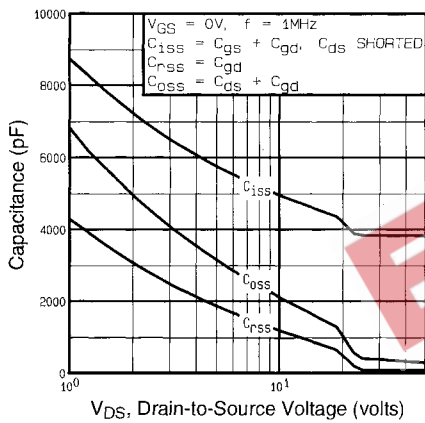


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

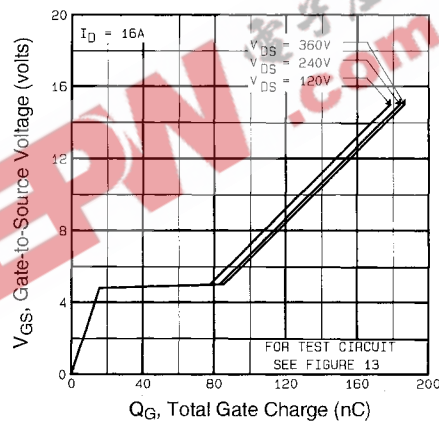


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

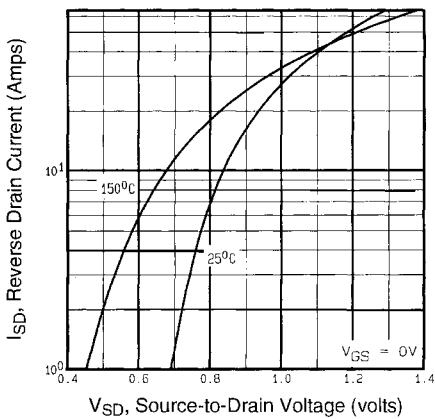


Fig 7. Typical Source-Drain Diode Forward Voltage

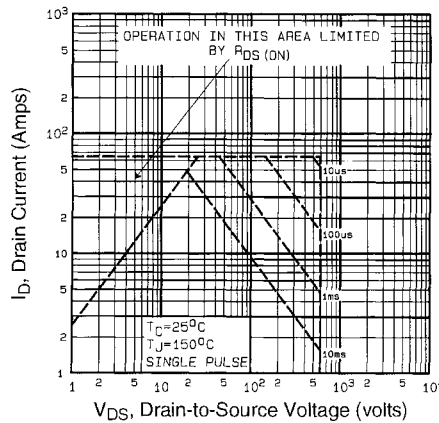


Fig 8. Maximum Safe Operating Area

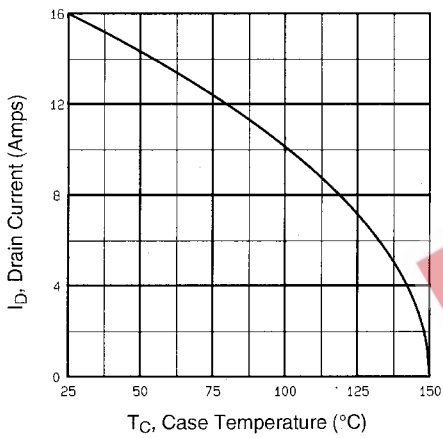


Fig 9. Maximum Drain Current Vs. Case Temperature

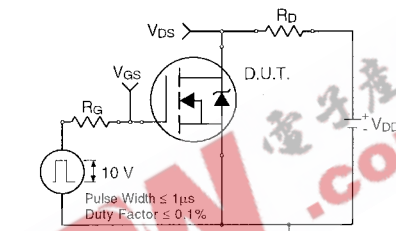


Fig 10a. Switching Time Test Circuit

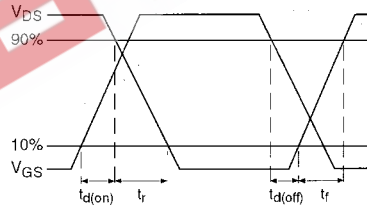


Fig 10b. Switching Time Waveforms

DATA SHEETS

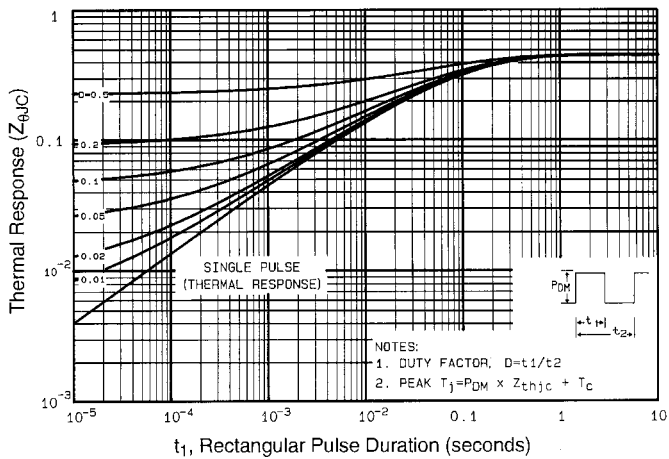


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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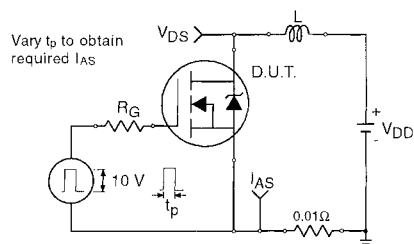


Fig 12a. Unclamped Inductive Test Circuit

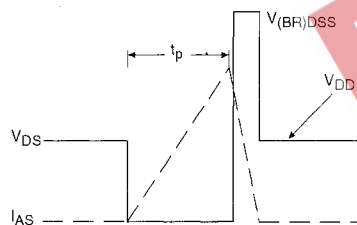


Fig 12b. Unclamped Inductive Waveforms

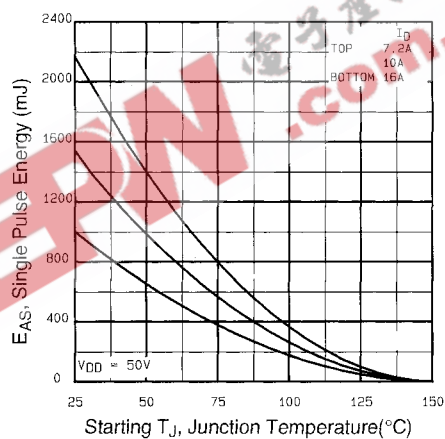


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

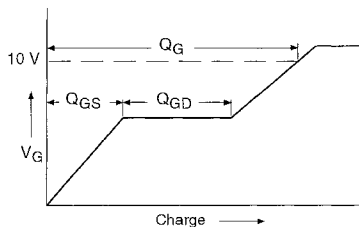


Fig 13a. Basic Gate Charge Waveform

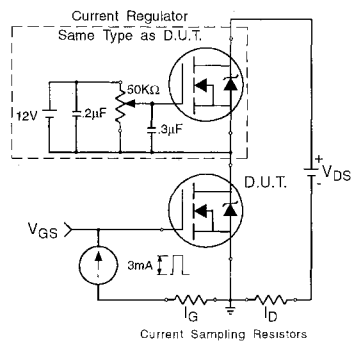


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1511

Appendix C: Part Marking Information – See page 1517

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