-6.5A, -100V, 0.300 Ohm, P-Channel Power MOSFET

This P-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17511.

Ordering Information

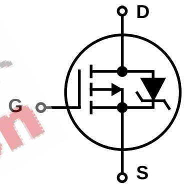
PART NUMBER	PACKAGE	BRAND
IRFF9130	TO-205AF	IRFF9130

NOTE: When ordering, include the entire part number.

Features

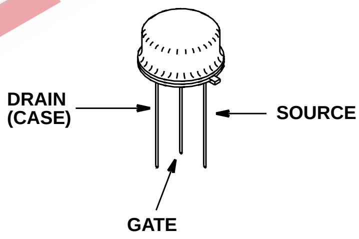
- -6.5A, -100V
- $r_{DS(ON)} = 0.300\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Symbol



Packaging

JEDEC TO-205AF



CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD Handling Procedures.

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

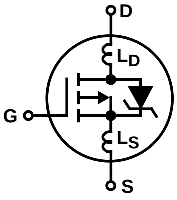
		IRFF9130	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	-100	V
Drain to Gate Voltage (R_{GS} = 20MΩ) (Note 1)	V_{DGR}	-100	V
Continuous Drain Current	I_D	-6.5	A
Pulsed Drain Current (Note 3)	I_{DM}	-26	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation (Figure 1)	P_D	25	W
Linear Derating Factor (Figure 1)		0.2	$W/^oC$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	500	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

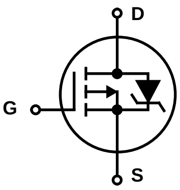
NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250µA, (Figure 10)	-100	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = -250µA	-2.0	-	-4.0	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	-25	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_C = 125^oC$	-	-	-250	µA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = -10V	-6.5	-	-	A
Gate to Source Leakage	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -3A, (Figures 8, 9)	-	0.25	0.300	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq I_{D(ON)} \times r_{DS(ON)MAX}$, I_D = -3A, (Figure 12)	2.5	3.5	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 0.5 x Rated BV_{DSS}, $I_D \approx$ -6.5A, R_G = 9.1Ω, R_L = 7.4Ω for BV_{DSS} = -100V R_L =5.8Ω for BV_{DSS} = -80V (Figures 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	30	60	ns
Rise Time	t_r		-	70	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	70	140	ns
Fall Time	t_f		-	70	140	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = -10V, I_D = -6.5A, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{G(REF)}$ = -1.5mA, (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	25	45	nC
Gate to Source Charge	Q_{gs}		-	13	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	12	-	nC
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz, (Figure 11)	-	500	-	pF
Output Capacitance	C_{OSS}		-	300	-	pF
Reverse-Transfer Capacitance	C_{RSS}		-	100	-	pF
Internal Drain Inductance	L_D	Measured From the Drain Lead, 5mm (0.2in) From Package to Center of Die Modified MOSFET Symbol Showing the Internal Devices Inductances  	-	5.0	-	nH
Internal Source Inductance	L_S	Measured From The Source Lead, 5mm (0.2in) From Header to Source Bonding Pad	-	15	-	nH
Junction to Case	$R_{\theta JC}$		-	-	5.0	$^oC/W$
Junction to Ambient	$R_{\theta JA}$	Typical Socket Mount	-	-	175	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode		-	-	-6.5	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	-26	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_C = 25^oC$, $I_{SD} = 6.5A$, $V_{GS} = 0V$ (Figure 13)		-	-	-1.5	V
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, $I_{SD} = 6.5A$, $dI_{SD}/dt = 100A/\mu s$		-	300	-	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 150^oC$, $I_{SD} = 6.5A$, $dI_{SD}/dt = 100A/\mu s$		-	1.8	-	μC

NOTES:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 25V$, starting $T_J = 25^oC$, $L = 17.75mH$, $R_G = 25\Omega$, peak $I_{AS} = 6.5A$. (Figures 15, 16).

Typical Performance Curves Unless Otherwise Specified

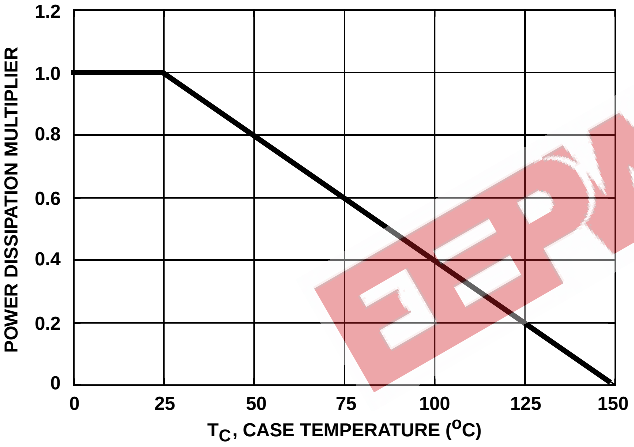


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

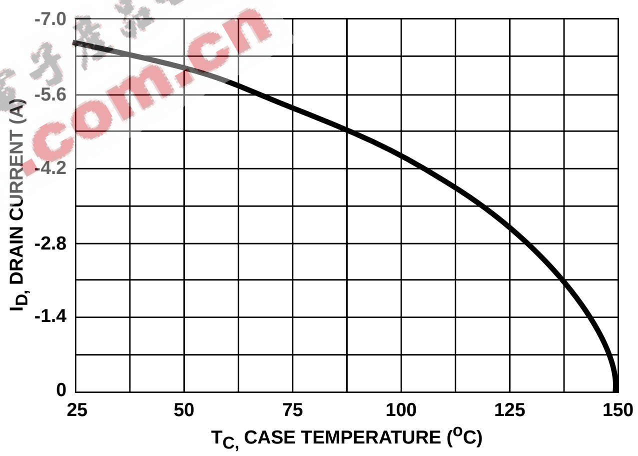
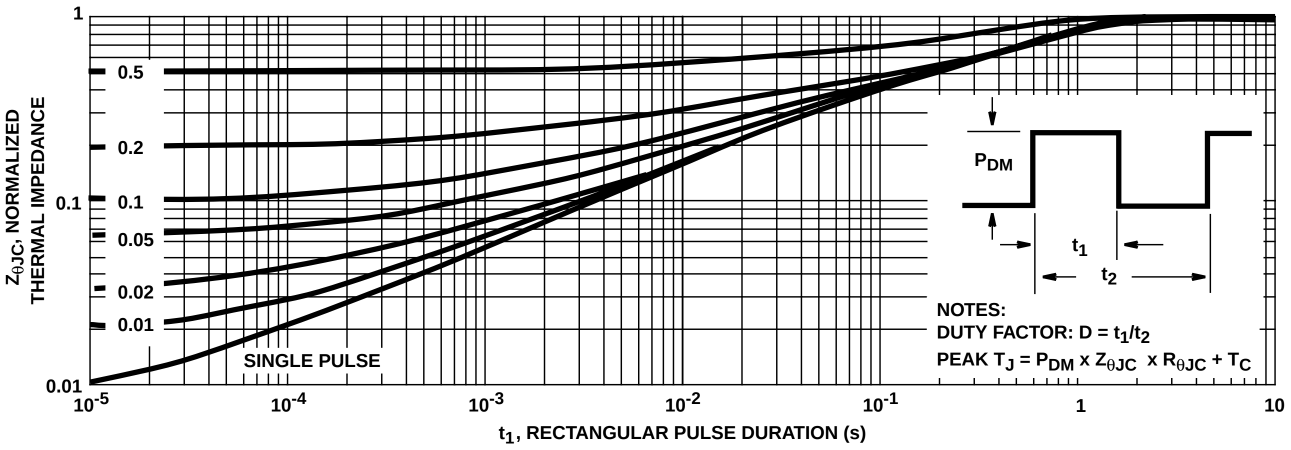


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE



NOTES:
DUTY FACTOR: $D = t_1/t_2$
PEAK $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

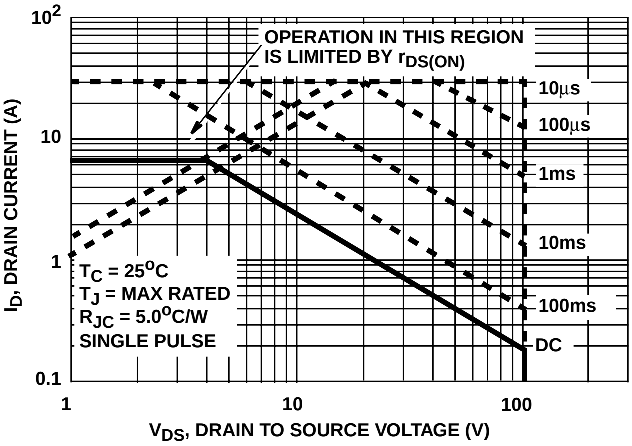


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

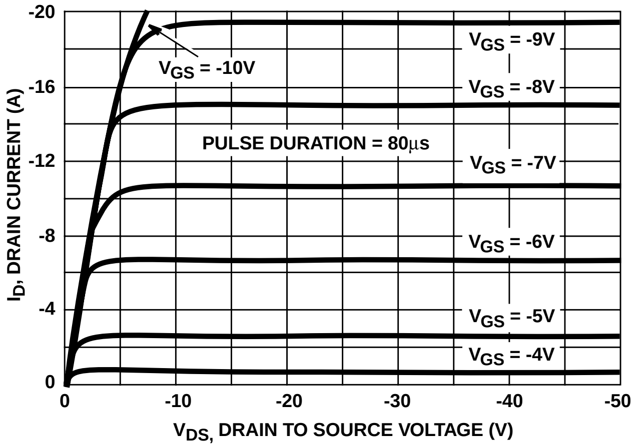


FIGURE 5. OUTPUT CHARACTERISTICS

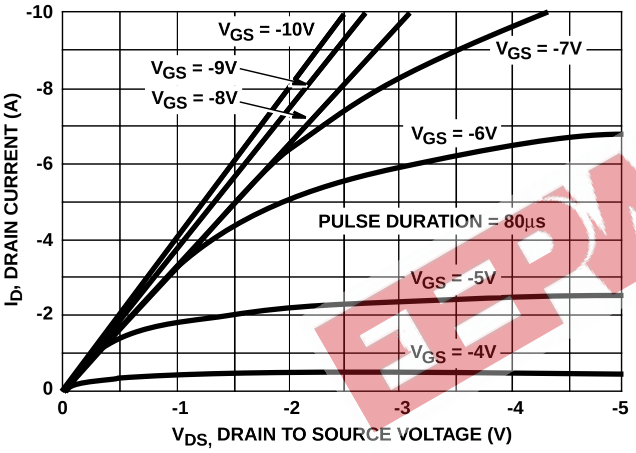


FIGURE 6. SATURATION CHARACTERISTICS

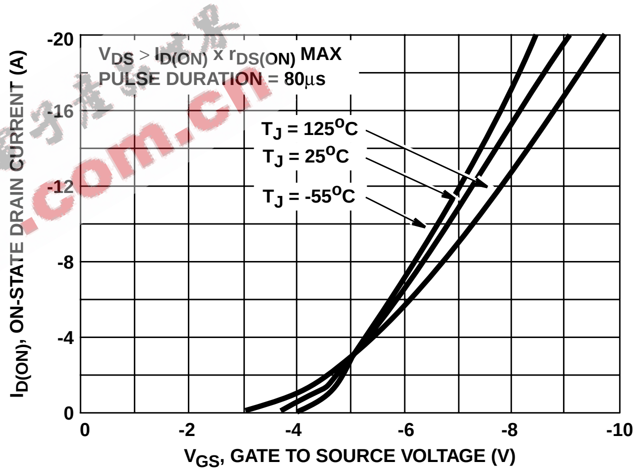


FIGURE 7. TRANSFER CHARACTERISTICS

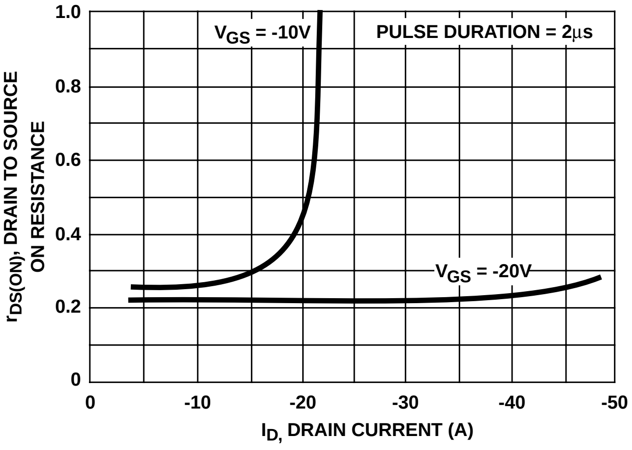


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

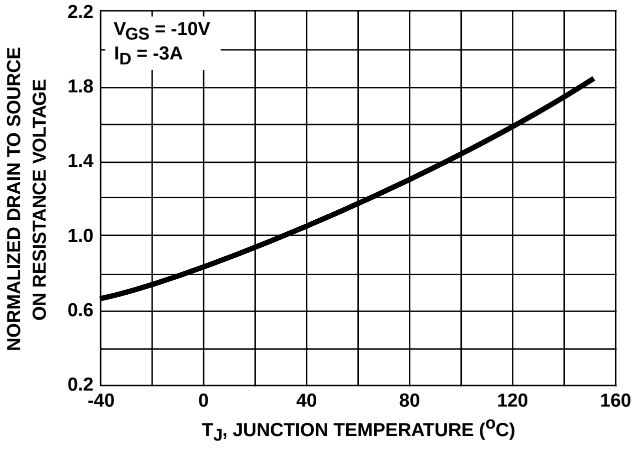


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

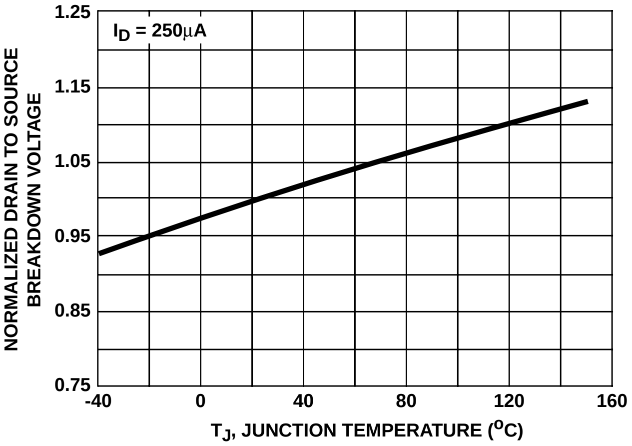


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

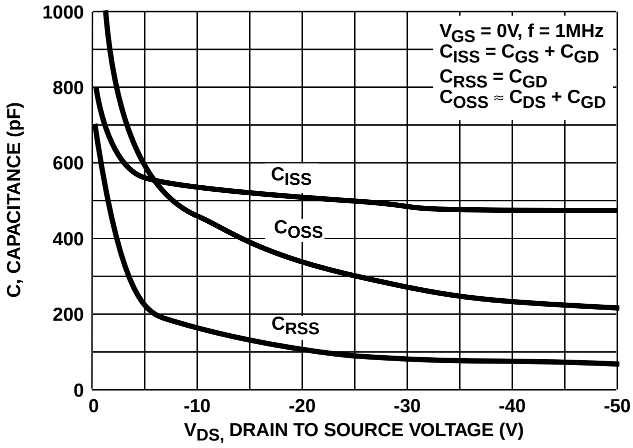


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

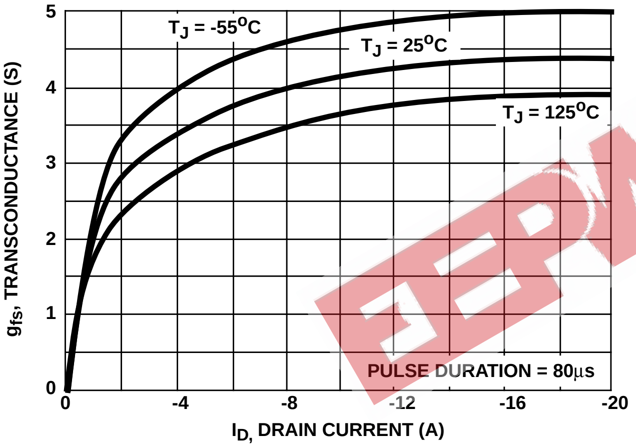


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

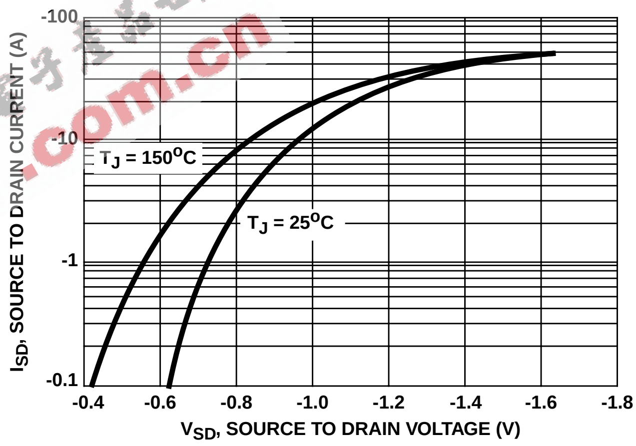


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

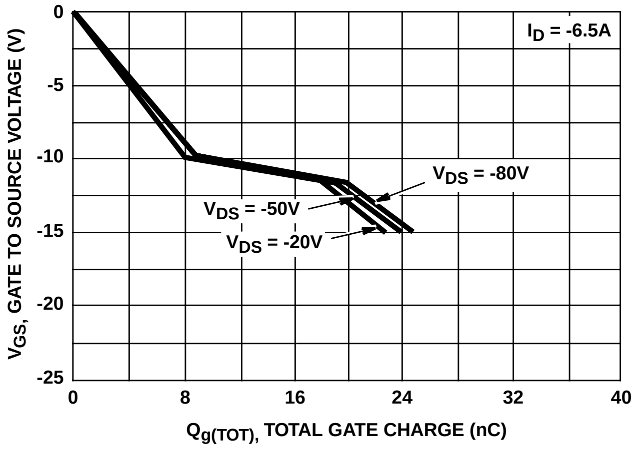


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

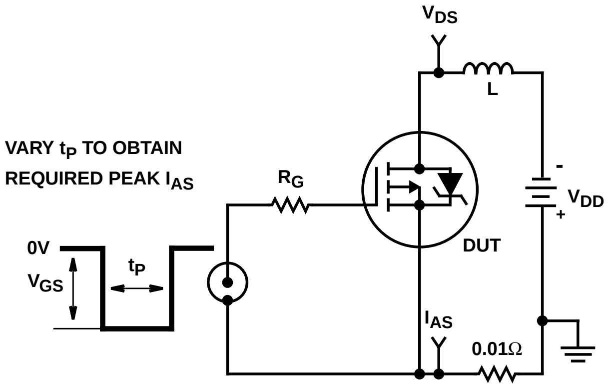


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

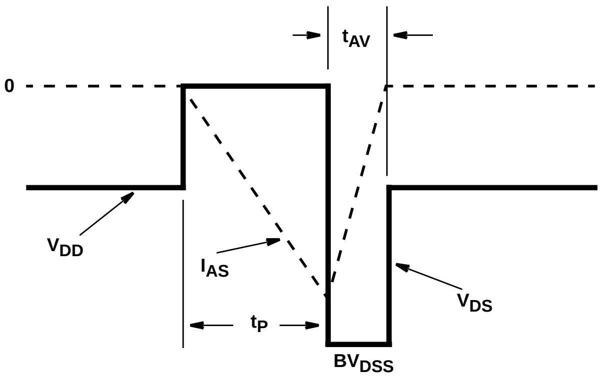


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

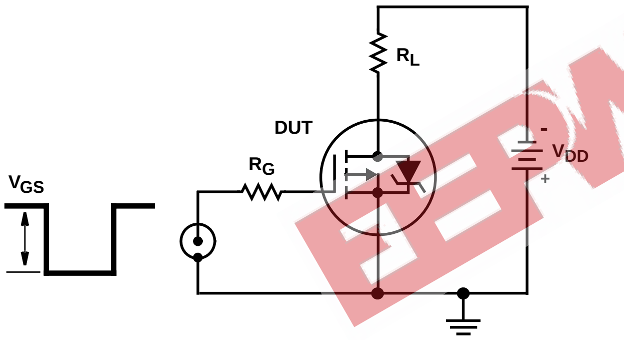


FIGURE 17. SWITCHING TIME TEST CIRCUIT

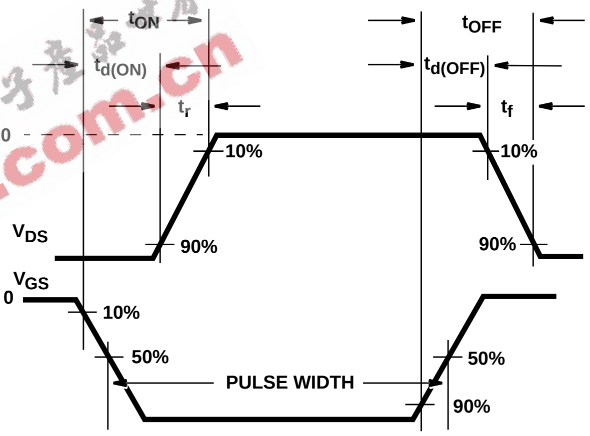


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

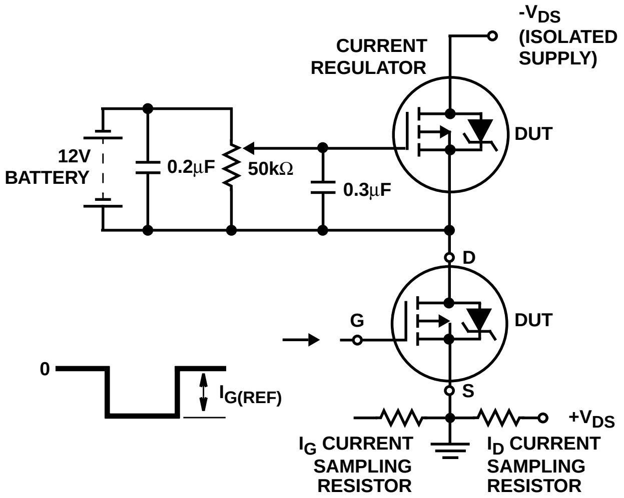


FIGURE 19. GATE CHARGE TEST CIRCUIT

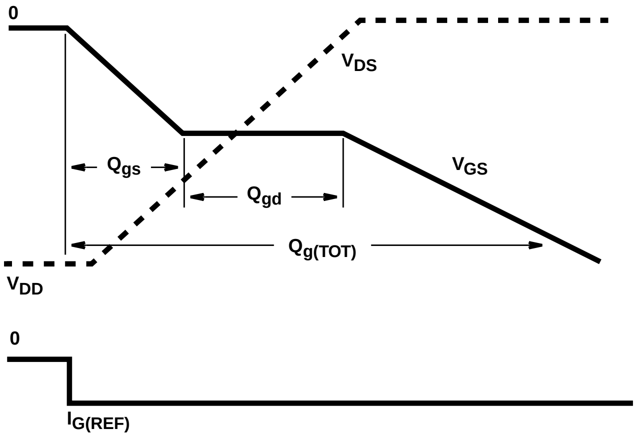


FIGURE 20. GATE CHARGE WAVEFORMS

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Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029