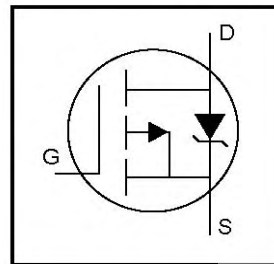


- Ultra Low On-Resistance
- P-Channel
- Surface Mount (IRFR9024N)
- Straight Lead (IRFU9024N)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

HEXFET® Power MOSFET



$$V_{DS} = -55V$$

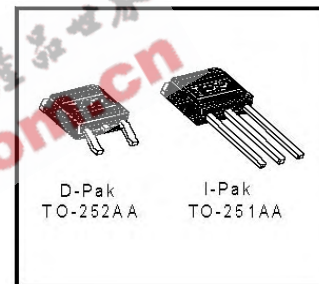
$$R_{DS(on)} = 0.175\Omega$$

$$I_D = -11A$$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-11	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-8	
I_{DM}	Pulsed Drain Current ①	-44	
$P_D @ T_C = 25^\circ C$	Power Dissipation	38	W
	Linear Derating Factor	0.30	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	62	mJ
I_{AR}	Avalanche Current①	-6.6	A
E_{AR}	Repetitive Avalanche Energy①	3.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-10	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	3.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	---	50	
$R_{\theta JA}$	Junction-to-Ambient	---	110	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-55	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.05	—	V/°C	Reference to 25°C, I _D = -1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.175	Ω	V _{GS} = -10V, I _D = -6.6A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	2.5	—	—	S	V _{DS} = -25V, I _D = -7.2A⑥
I _{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	V _{DS} = -55V, V _{GS} = 0V
		—	—	-250	μA	V _{DS} = -44V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V _{GS} = -20V
Q _g	Total Gate Charge	—	—	19	nC	I _D = -7.2A
Q _{gs}	Gate-to-Source Charge	—	—	5.1	nC	V _{DS} = -44V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	10	nC	V _{GS} = -10V, See Fig. 6 and 13 ④⑤
t _{d(on)}	Turn-On Delay Time	—	13	—	ns	V _{DD} = -28V
t _r	Rise Time	—	55	—	ns	I _D = -7.2A
t _{d(off)}	Turn-Off Delay Time	—	23	—	ns	R _e = 24Ω
t _f	Fall Time	—	37	—	ns	R _D = 3.7Ω, See Fig. 10 ④⑥
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)
L _S	Internal Source Inductance	—	7.5	—	nH	from package and center of die contact⑤
C _{iss}	Input Capacitance	—	350	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	170	—	pF	V _{DS} = -25V
C _{rss}	Reverse Transfer Capacitance	—	92	—	pF	f = 1.0MHz, See Fig. 5⑥

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-11	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-44	A	
V _{SD}	Diode Forward Voltage	—	—	-1.6	V	T _J = 25°C, I _S = -7.2A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	47	71	ns	T _J = 25°C, I _F = -7.2A
Q _{rr}	Reverse Recovery Charge	—	84	130	nC	di/dt = 100A/μs ④⑥
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
 ② Starting T_J = 25°C, L = 2.8mH
 R_G = 25Ω, I_{AS} = -6.6A. (See Figure 12)
 ③ I_{SD} ≤ -6.6A, di/dt ≤ 240A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact

⑥ Uses IRF9Z24N data and test conditions.

** When mounted on 1" square PCB (FR-4 or G-10 Material) .
 For recommended footprint and soldering techniques refer to application note #AN-994

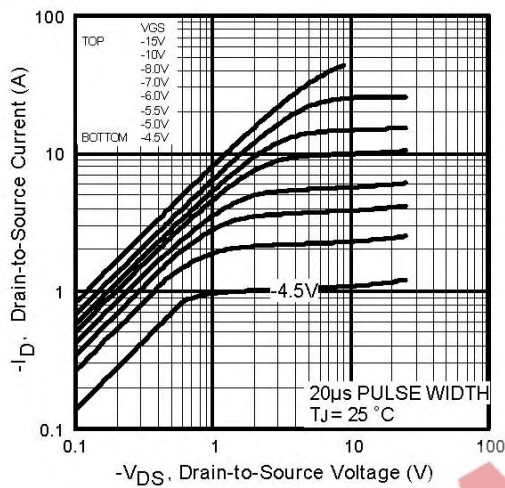


Fig 1. Typical Output Characteristics

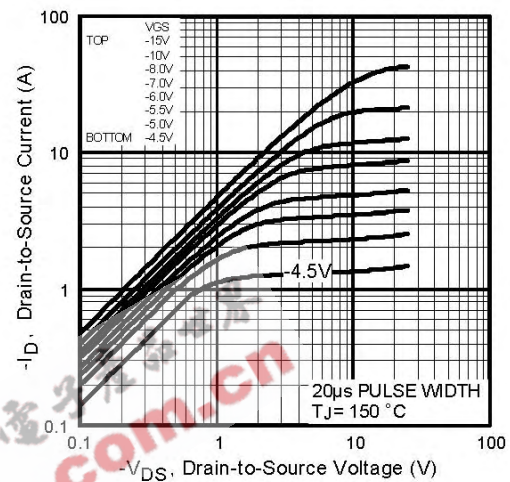


Fig 2. Typical Output Characteristics

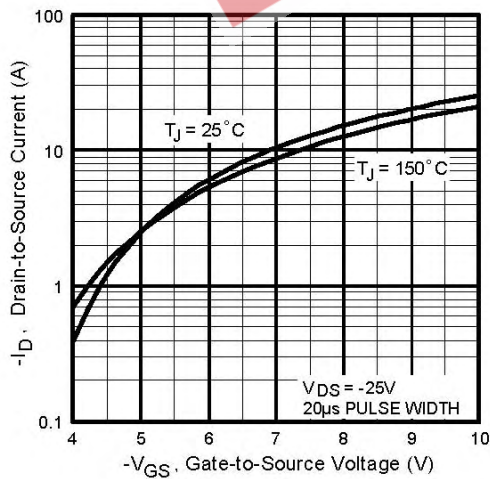


Fig 3. Typical Transfer Characteristics

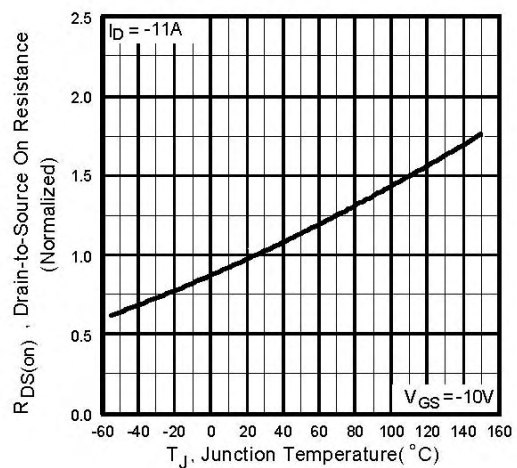


Fig 4. Normalized On-Resistance
Vs. Temperature

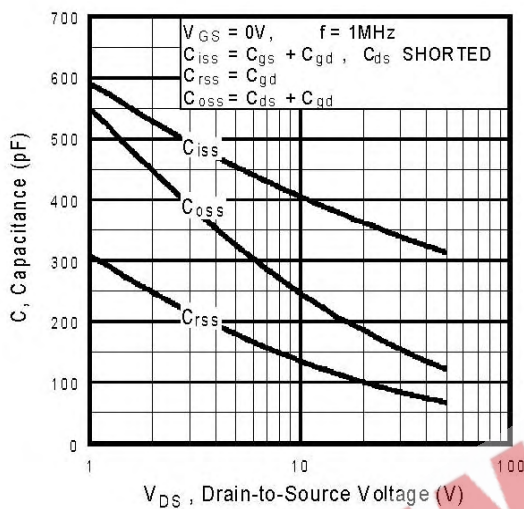


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

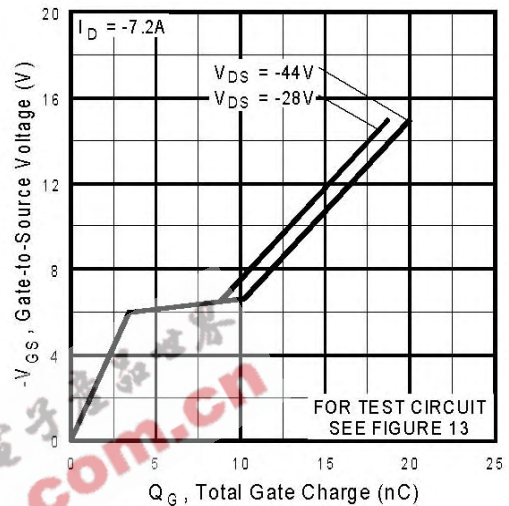


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

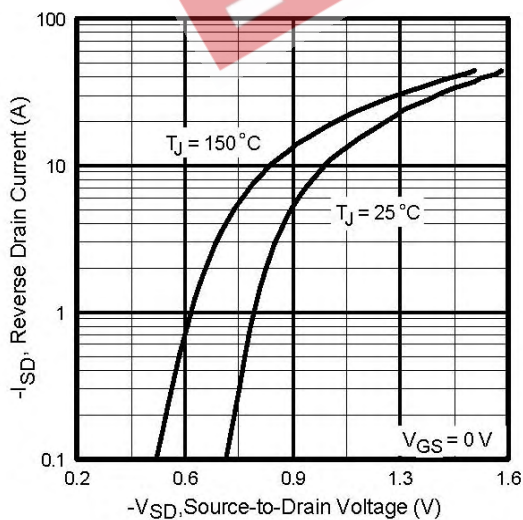


Fig 7. Typical Source-Drain Diode Forward Voltage

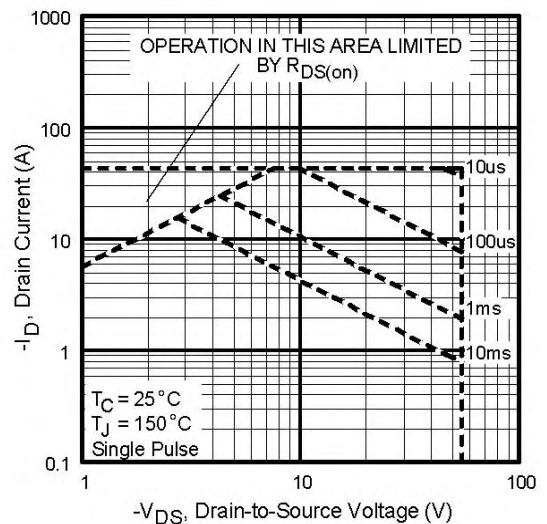


Fig 8. Maximum Safe Operating Area

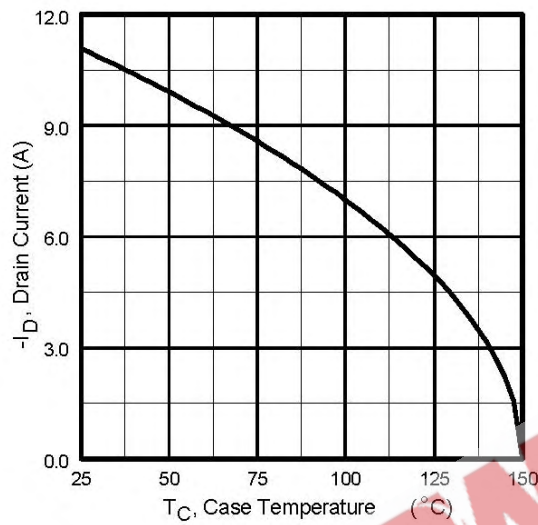


Fig 9. Maximum Drain Current Vs. Case Temperature

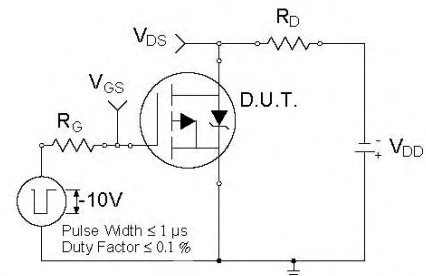


Fig 10a. Switching Time Test Circuit

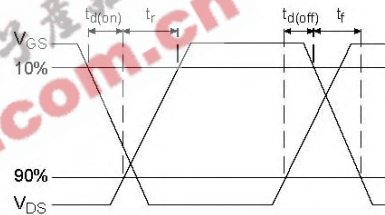


Fig 10b. Switching Time Waveforms

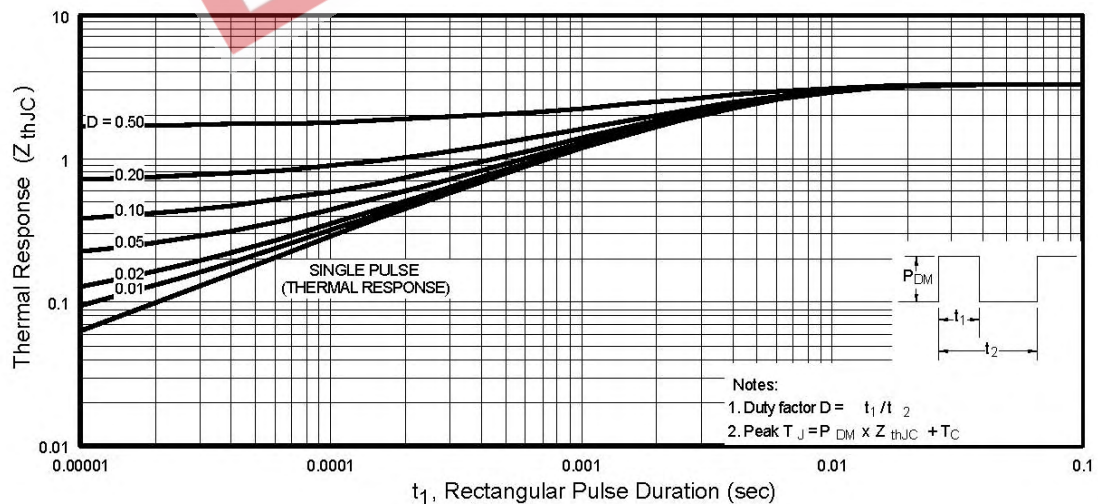


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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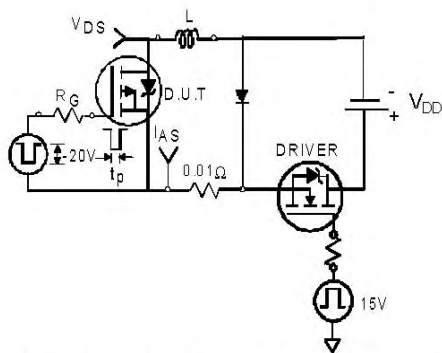


Fig 12a. Unclamped Inductive Test Circuit

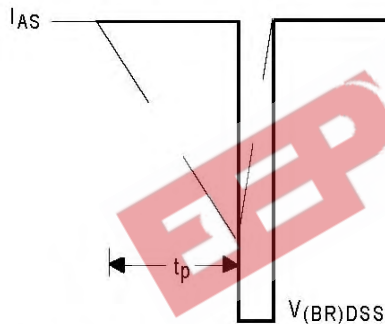


Fig 12b. Unclamped Inductive Waveforms

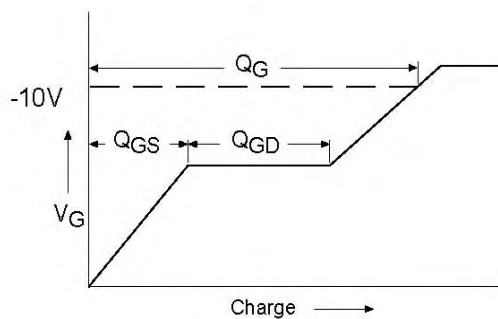


Fig 13a. Basic Gate Charge Waveform

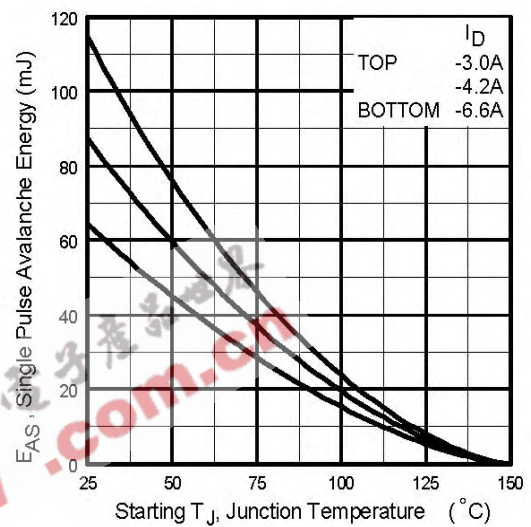


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

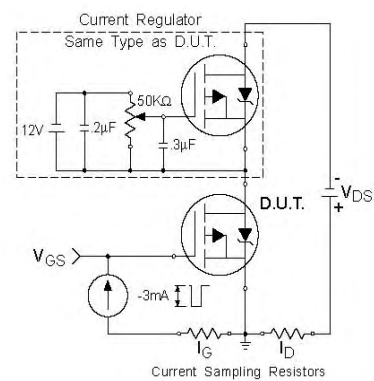
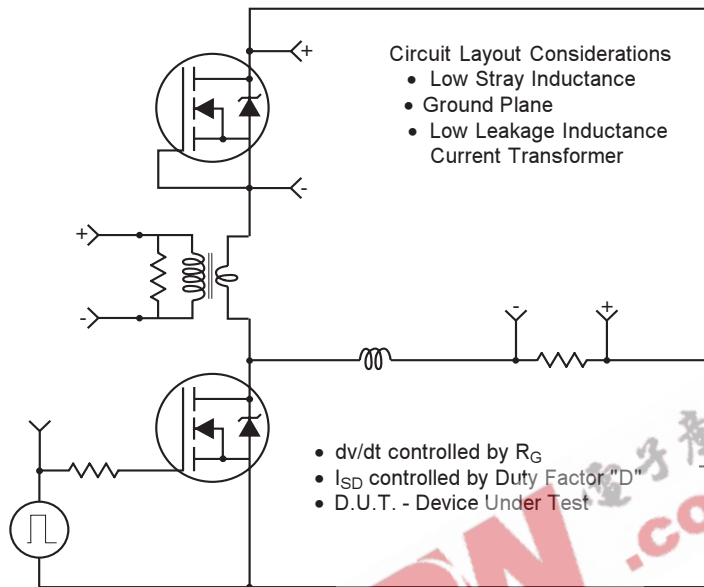


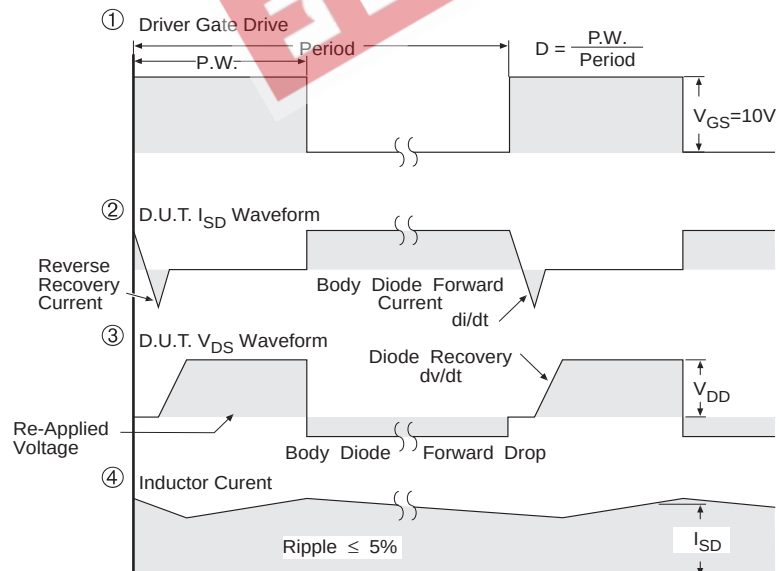
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements

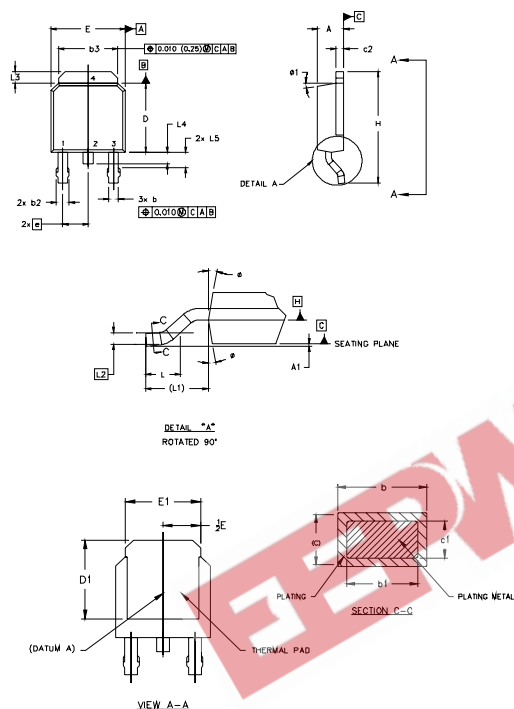


*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14 For P Channel HEXFETS

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Dimensions are shown in millimeters (inches)



NOTES:

1.0 DIMENSION AND TOLERANCING PER ASME Y14.5 M – 1994.

2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]

3.0 DIMENSION UNCONTROLLED IN L5

4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.

5.0 SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540] FROM THE LEAD TIP.

6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO–252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.13		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	0.031	5
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	.686	.016	.022	5
d	.094	0.89	.018	.036	5
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170	–	4
e	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.		106 REF.		
L2	0.051 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	3
ø	0"	10"	0"	10"	
ø1	0"	15"	0"	15"	

LEAD ASSIGNMENTS

HEXFET

1. – GATE

2. – DRAIN

3. – SOURCE

4. – DRAIN

IGBTs, CoPACK

1. – GATE

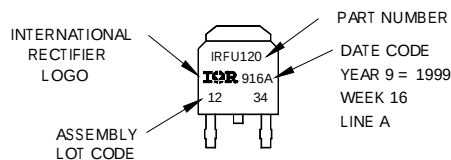
2. – COLLECTOR

3. – EMITTER

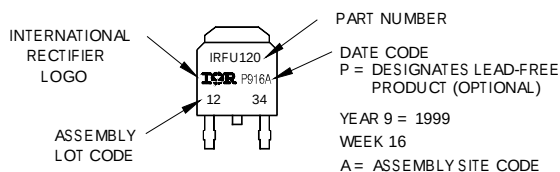
4. – COLLECTOR

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

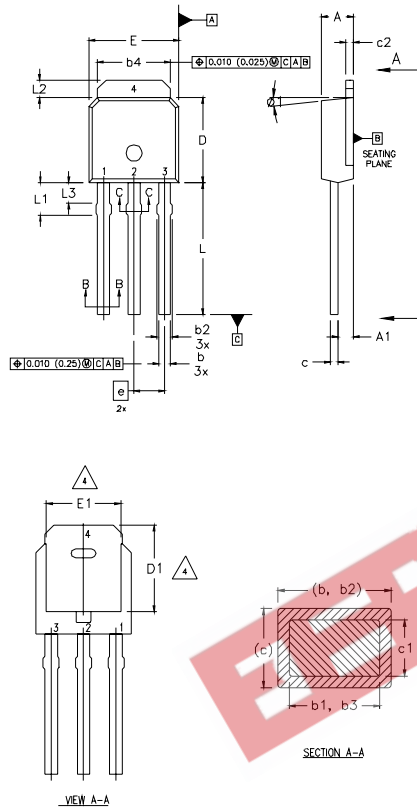


OR



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

HEXFET

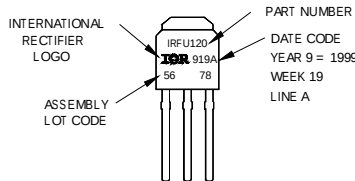
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	0.46	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	0"	15"	0"	15"	

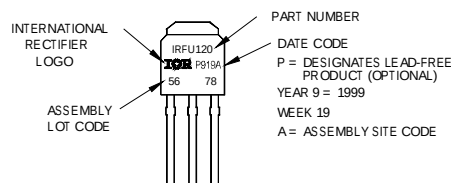
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line
position indicates "Lead-Free"



OR

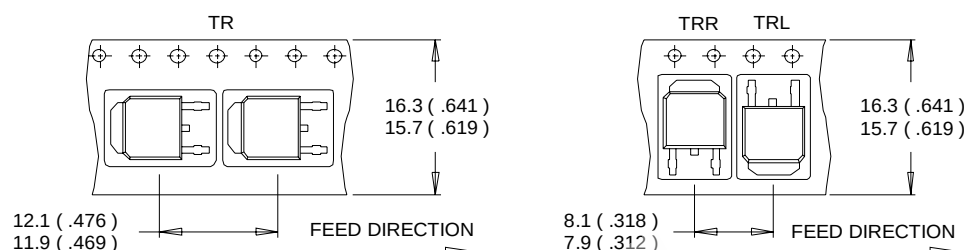


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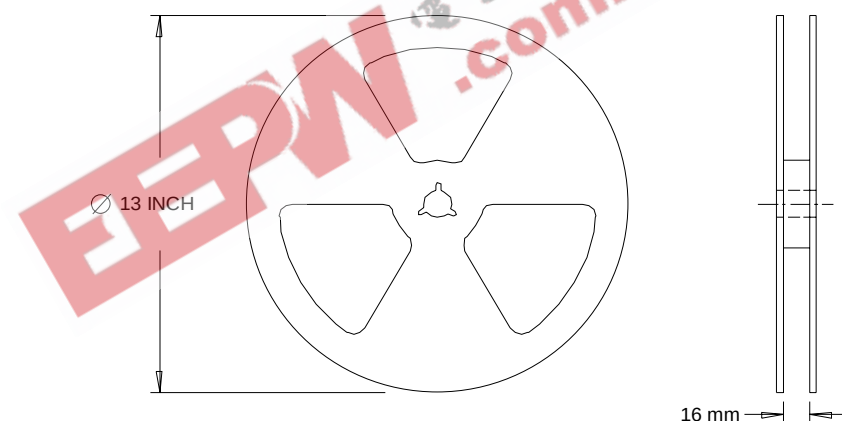
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.12/04

www.irf.com

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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