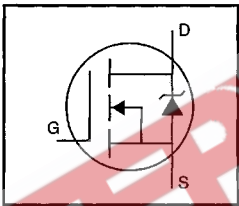


HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- For Automatic Insertion
- End Stackable
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements

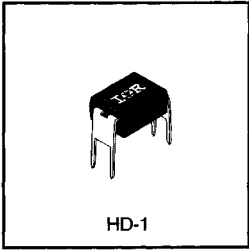


$V_{DSS} = 60V$
$R_{DS(on)} = 0.20\Omega$
$I_D = 1.7A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4-pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1 inch pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 watt.



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Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	1.7	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	1.2	
I_{DM}	Pulsed Drain Current ①	14	
$P_D @ T_C = 25^\circ C$	Power Dissipation	1.3	W
	Linear Derating Factor	0.0083	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	130	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	—	—	120	°C/W

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V _{GS} =0V, I _D =250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.063	—	V/°C	Reference to 25°C, I _D =1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.20	Ω	V _{GS} =10V, I _D =1.0A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
g _{fs}	Forward Transconductance	0.96	—	—	S	V _{DS} =25V, I _D =1.0A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} =60V, V _{GS} =0V
		—	—	250	μA	V _{DS} =48V, V _{GS} =0V, T _J =150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} =20V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V _{GS} =-20V
Q _g	Total Gate Charge	—	—	11	nC	I _D =10A
Q _{gs}	Gate-to-Source Charge	—	—	3.1	nC	V _{DS} =48V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	5.8	nC	V _{GS} =10V See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	10	—	ns	V _{DD} =30V
t _r	Rise Time	—	50	—	ns	I _D =10A
t _{d(off)}	Turn-Off Delay Time	—	13	—	ns	R _G =24Ω
t _f	Fall Time	—	19	—	ns	R _D =2.7Ω See Figure 10 ④
L _D	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	6.0	—	nH	
C _{iss}	Input Capacitance	—	310	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	160	—	pF	V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	37	—	pF	f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	1.7	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	14	A	
V _{SD}	Diode Forward Voltage	—	—	1.6	V	T _J =25°C, I _S =1.7A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	70	140	ns	T _J =25°C, I _F =10A
Q _{rr}	Reverse Recovery Charge	—	0.20	0.40	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V_{DD}=25V, starting T_J=25°C, L=52mH, R_G=25Ω, I_{AS}=1.7A (See Figure 12)
- ③ I_{SD}≤10A, di/dt≤90A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤175°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.

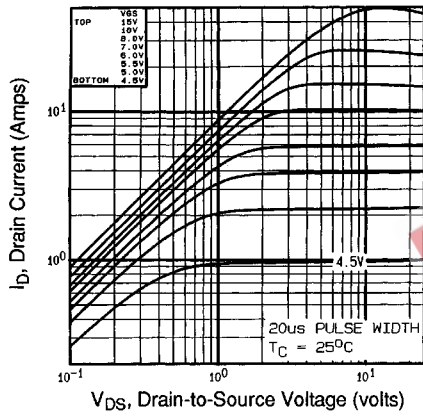


Fig 1. Typical Output Characteristics,
 $T_C=25^\circ\text{C}$

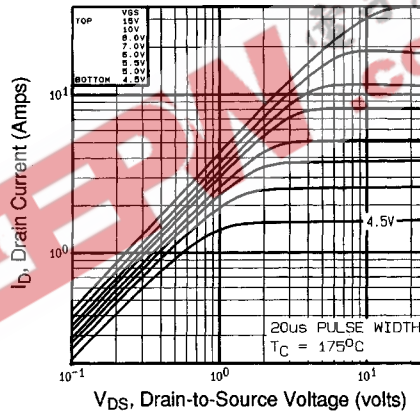


Fig 2. Typical Output Characteristics,
 $T_C=175^\circ\text{C}$

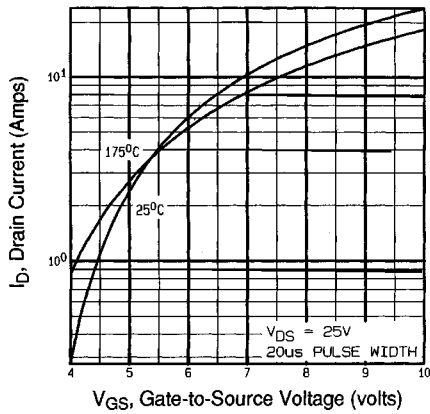


Fig 3. Typical Transfer Characteristics

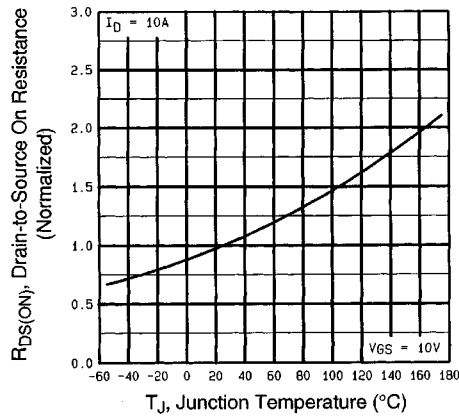


Fig 4. Normalized On-Resistance
Vs. Temperature

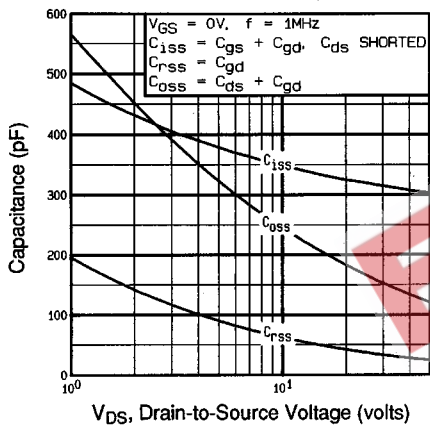


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

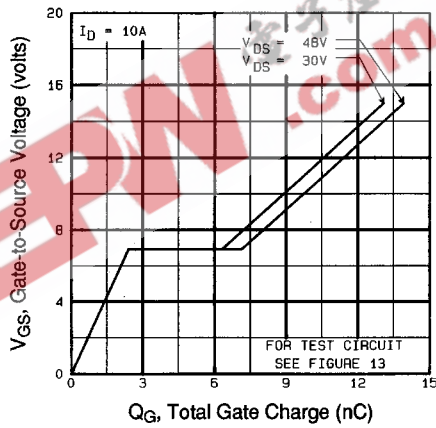


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

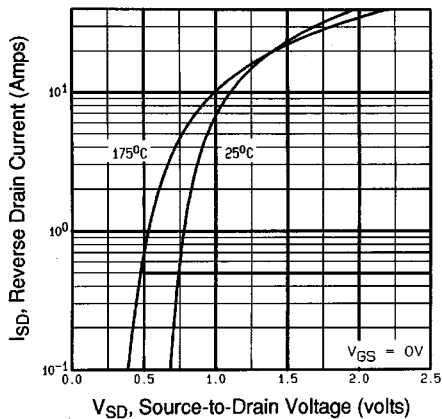


Fig 7. Typical Source-Drain Diode Forward Voltage

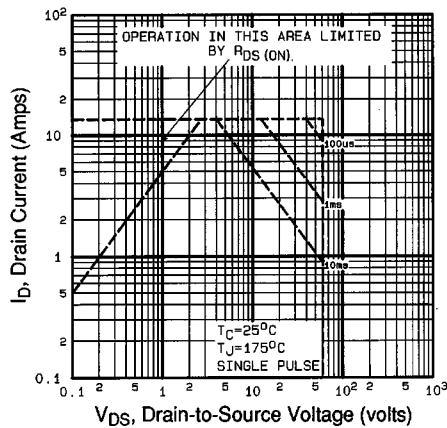


Fig 8. Maximum Safe Operating Area

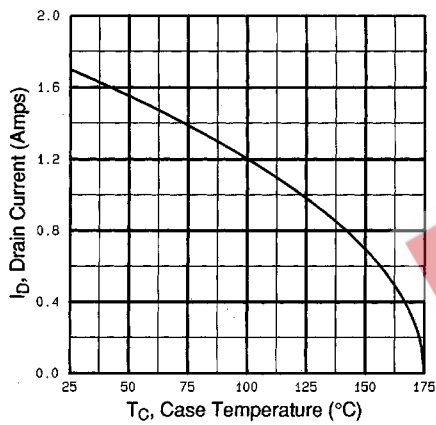


Fig 9. Maximum Drain Current Vs. Case Temperature

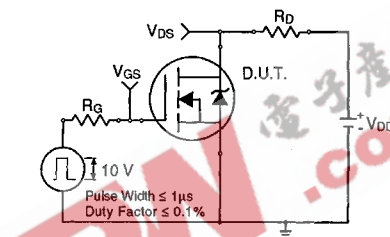


Fig 10a. Switching Time Test Circuit

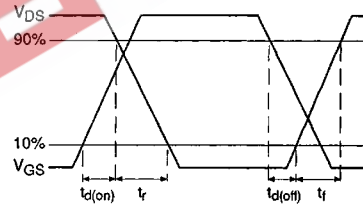


Fig 10b. Switching Time Waveforms

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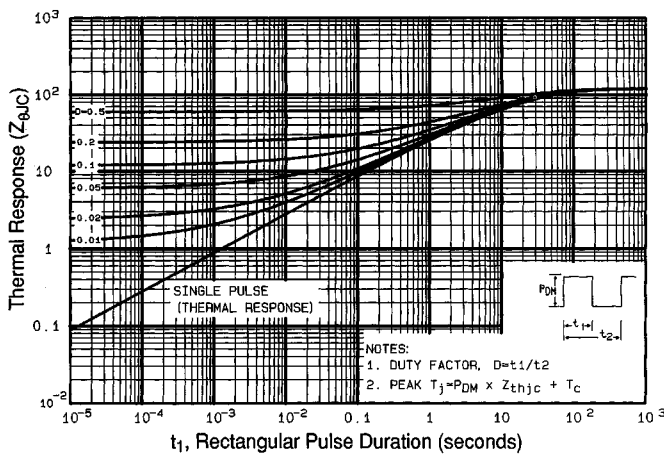


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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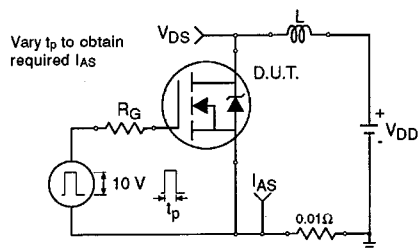


Fig 12a. Unclamped Inductive Test Circuit

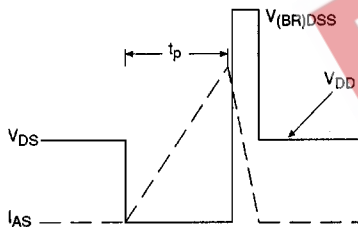


Fig 12b. Unclamped Inductive Waveforms

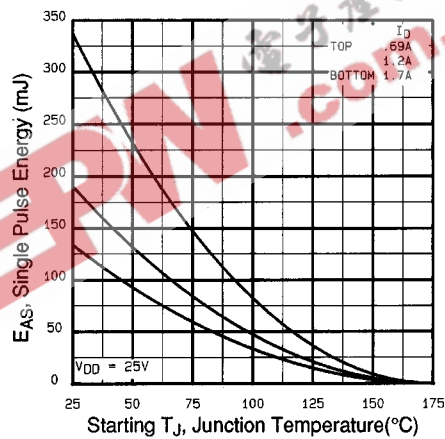


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

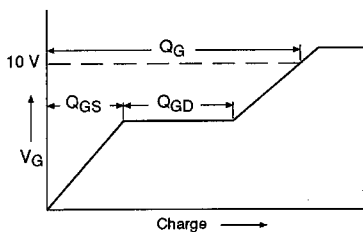


Fig 13a. Basic Gate Charge Waveform

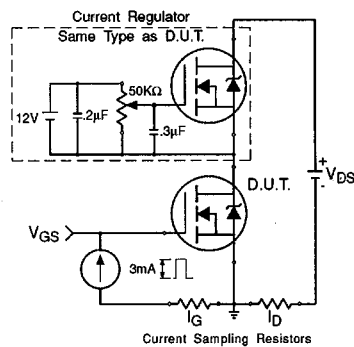


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1507

Appendix C: Part Marking Information – See page 1515

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