# STD95NH02L

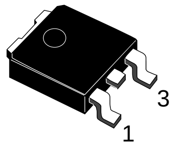
## N-CHANNEL 24V - 0.0039Ω - 80A DPAK
## ULTRA LOW GATE CHARGE STripFET™ MOSFET

**Table 1: General Features**

| TYPE | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| STD95NH02L | 24 V | < 0.005Ω | 80(*) A |

- TYPICAL $R_{DS}$(on) = 0.0039Ω @ 10 V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

**Figure 1: Package**

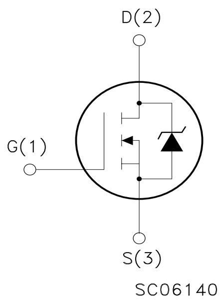



**DPAK**
**TO-252**
(Suffix “T4”)

### DESCRIPTION

The **STD95NH02L** is based on the latest generation of ST’s proprietary STripFET™ technology. An innovative layout enables the device to also exhibit extremely low gate charge for the most demanding requirements in high-frequency DC-DC converters. It’s therefore ideal for high-density converters in Telecom and Computer applications.

**Figure 2: Internal Schematic Diagram**




### APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS



**Table 2: Order Codes**

| PART NUMBER | MARKING | PACKAGE | PACKAGING |
|---|---|---|---|
| STD95NH02LT4 | D95NH02L | DPAK | TAPE & REEL |

Rev. 2

**Table 3: Absolute Maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{spike}$(1) | Drain-source Voltage Rating | 30 | V |
| $V_{DS}$ | Drain-source Voltage ($V_{GS}$ = 0) | 24 | V |
| $V_{DGR}$ | Drain-gate Voltage ($R_{GS}$ = 20 kΩ) | 24 | V |
| $V_{GS}$ | Gate- source Voltage | ± 20 | V |
| $I_D$ (*) | Drain Current (continuous) at $T_C$ = 25°C | 80 | A |
| $I_D$ | Drain Current (continuous) at $T_C$ = 100°C | 68 | A |
| $I_{DM}$ (2) | Drain Current (pulsed) | 320 | A |
| $P_{TOT}$ | Total Dissipation at $T_C$ = 25°C | 100 | W |
| | Derating Factor | 0.67 | W/°C |
| $E_{AS}$ (3) | Single Pulse Avalanche Energy | 600 | mJ |
| $T_{stg}$ | Storage Temperature | -55 to 175 | °C |
| $T_j$ | Max. Operating Junction Temperature | | |

(1) Garanted when external $R_g$ = 4.7 Ω and $t_f$ < $t_f$ max.
(2) Pulse width limited by safe operating area.
(3) Starting $T_j$ = 25°C, $I_D$ = 40A, $V_{DD}$ = 22V
(*) Value limited by wires

**Table 4: Thermal Data**

| | | | |
|---|---|---|---|
| Rthj-case | Thermal Resistance Junction-case Max | 1.5 | °C/W |
| Rthj-amb | Thermal Resistance Junction-ambient Max | 100 | °C/W |
| $T_l$ | Maximum Lead Temperature For Soldering Purpose | 275 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_{CASE}$ =25°C UNLESS OTHERWISE SPECIFIED)

**Table 5: On/Off**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D$ = 250 µA, $V_{GS}$ = 0 | 24 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current ($V_{GS}$ = 0) | $V_{DS}$ = Max Rating<br>$V_{DS}$ = Max Rating, $T_C$ = 125 °C | | | 1<br>10 | µA<br>µA |
| $I_{GSS}$ | Gate-body Leakage Current ($V_{DS}$ = 0) | $V_{GS}$ = ± 20V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA | 1 | | | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 40 A<br>$V_{GS}$ = 5 V, $I_D$ =40 A | | 0.0039<br>0.0055 | 0.005<br>0.009 | Ω<br>Ω |

## ELECTRICAL CHARACTERISTICS (CONTINUED)

### Table 6: Dynamic

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (4) | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 10 A | | 30 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input Capacitance<br>Output Capacitance<br>Reverse Transfer Capacitance | $V_{DS}$ = 15V, f = 1 MHz, $V_{GS}$ = 0 | | 2070<br>990<br>90 | | pF<br>pF<br>pF |
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$ | Turn-on Delay Time<br>Rise Time<br>Turn-off Delay Time<br>Fall Time | $V_{DD}$ = 12 V, $I_D$ = 40 A,<br>$R_G$= 4.7 Ω $V_{GS}$ = 10 V<br>(see Figure 16) | | 20<br>110<br>47<br>20 | | ns<br>ns<br>ns<br>ns |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total Gate Charge<br>Gate-Source Charge<br>Gate-Drain Charge | $V_{DD}$ = 12 V, $I_D$ = 80 A,<br>$V_{GS}$ = 5 V<br>(see Figure 19) | | 17<br>7.6<br>6.8 | | nC<br>nC<br>nC |
| $Q_{oss}$ (5) | Output Charge | $V_{DS}$ = 19 V, $V_{GS}$ = 0 V | | 22.6 | | nC |
| $Q_{gls}$ (6) | Third-Quadrant Gate Charge | $V_{DS}$ < 0 V, $V_{GS}$ = 5 V | | 15 | | nC |
| $R_G$ | Gate Input Resistance | f = 1 MHz Gate DC Bias = 0<br>Test Signal Level = 20 mV<br>Open Drain | | 1.8 | | Ω |

### Table 7: Source Drain Diode

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$ | Source-drain Current<br>Source-drain Current (pulsed) | | | | 80<br>320 | A<br>A |
| $V_{SD}$ (4) | Forward On Voltage | $I_{SD}$ = 40A, $V_{GS}$ = 0 | | | 1.3 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 80A, di/dt = 100 A/µs,<br>$V_{DD}$ =20 V, $T_j$ = 150°C<br>(see Figure 16) | | 42<br>50.4<br>2.4 | | ns<br>nC<br>A |

(4). Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(5). $Q_{oss} = C_{oss}*\Delta V_{in}$, $C_{oss} = C_{gd}+C_{ds}$. See Appendix A.
(6). Gate charge for Syncronous Operation.

**Figure 3: Safe Operating Area**

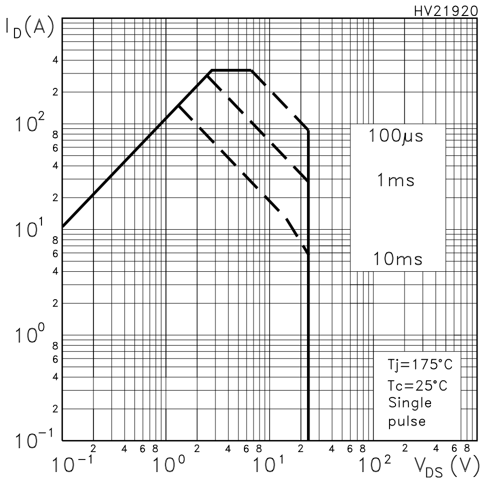



**Figure 6: Thermal Impedance**

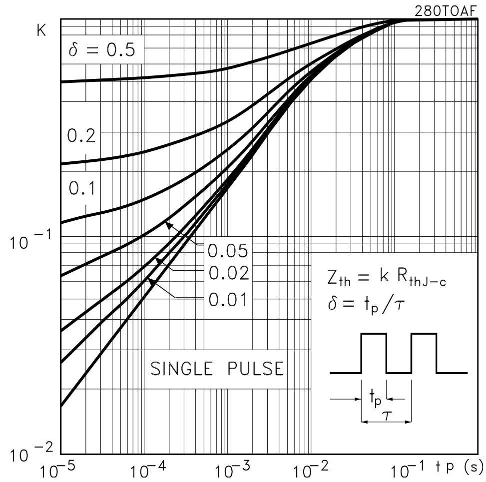



**Figure 4: Output Characteristics**

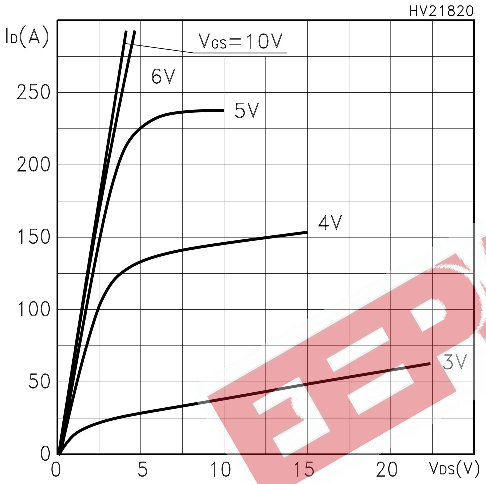



**Figure 7: Transfer Characteristics**

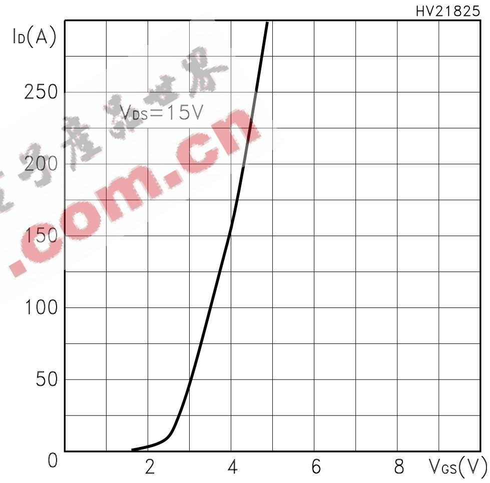



**Figure 5: Transconductance**

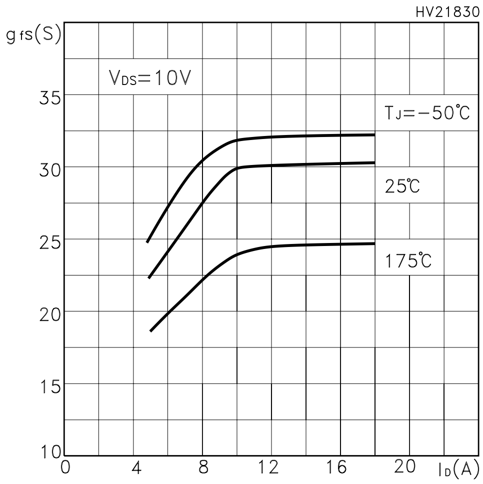



**Figure 8: Static Drain-source On Resistance**

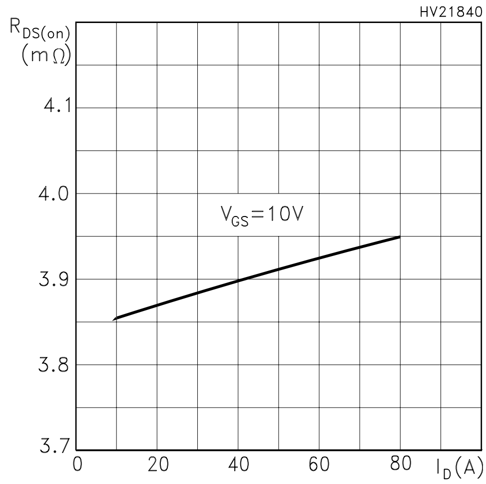


**Figure 9: Gate Charge vs Gate-source Voltage**

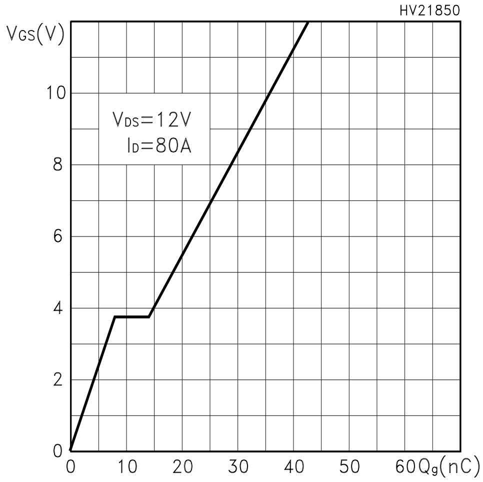



**Figure 12: Capacitance Variations**

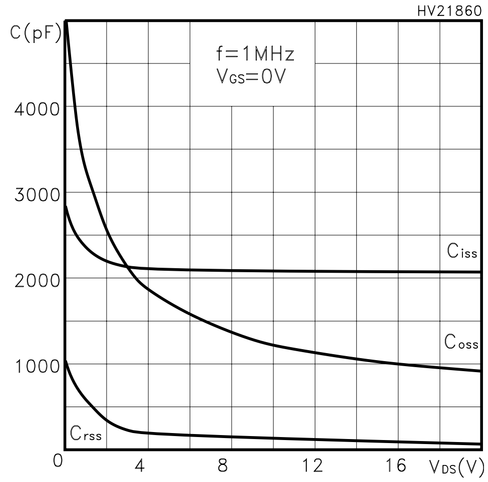



**Figure 10: Normalized Gate Thereshold Voltage vs Temperature**

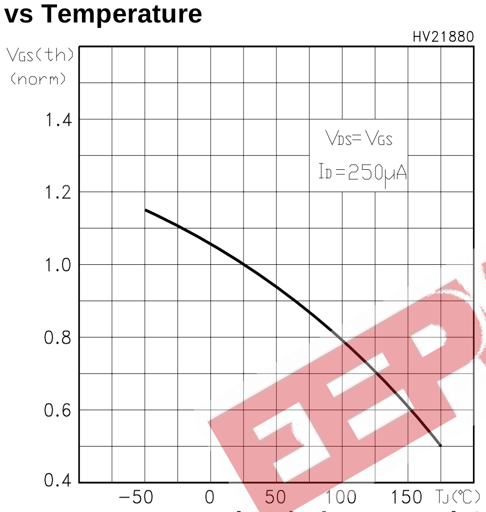



**Figure 13: Normalized On Resistance vs Temperature**

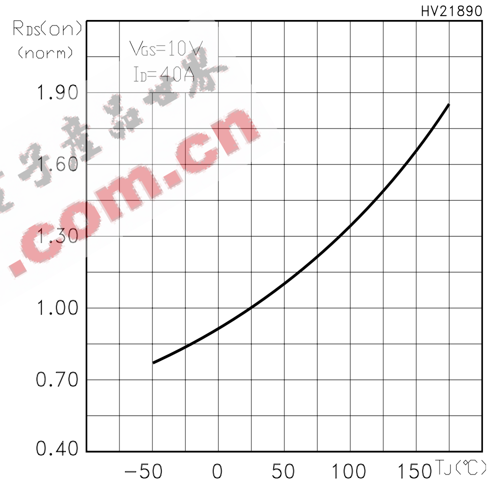



**Figure 11: Dource-Drain Diode Forward Characteristics**

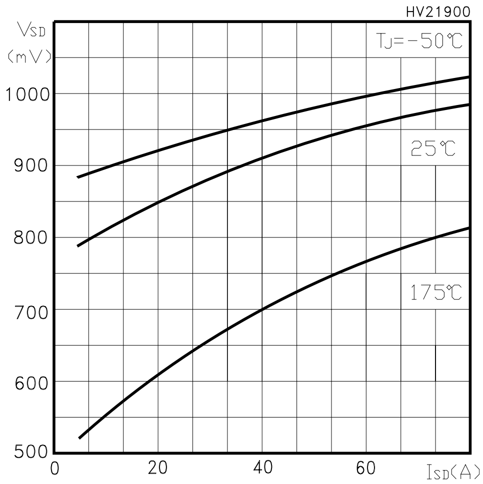



**Figure 14: Normalized Breakdown Voltage vs Temperature**

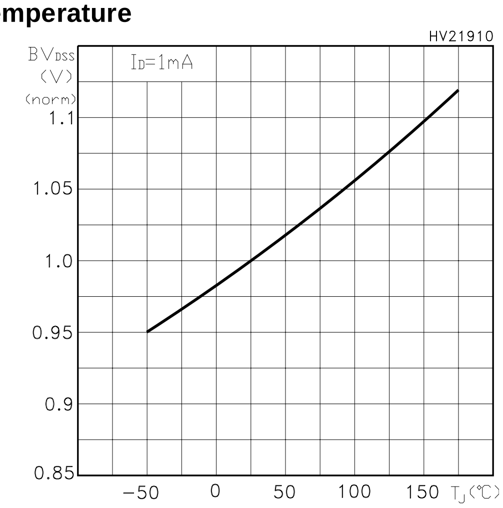


**Figure 15: Unclamped Inductive Load Test Circuit**

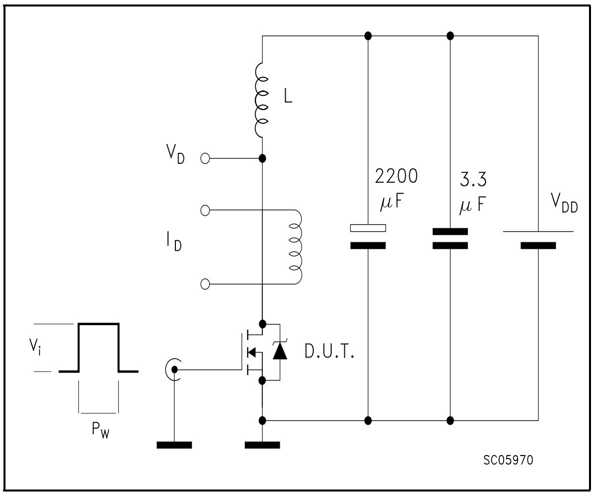



**Figure 16: Switching Times Test Circuit For Resistive Load**

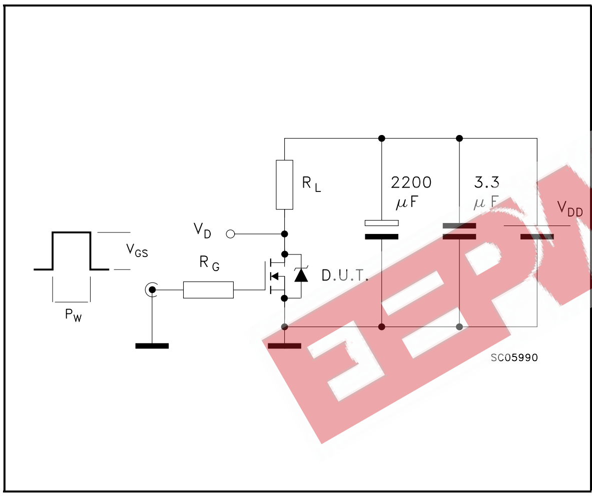



**Figure 17: Test Circuit For Inductive Load Switching and Diode Recovery Times**

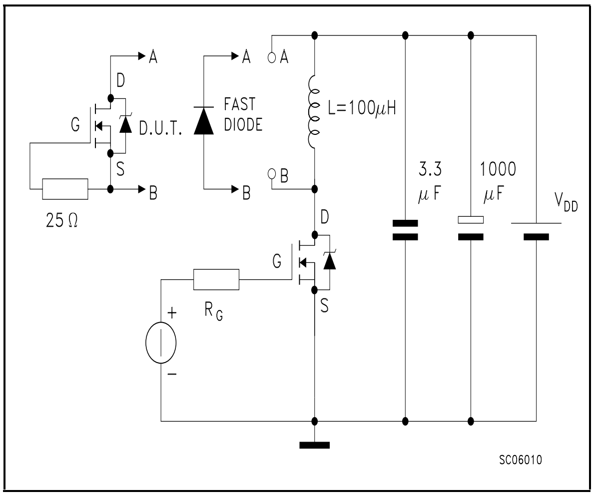



**Figure 18: Unclamped Inductive Wafeform**

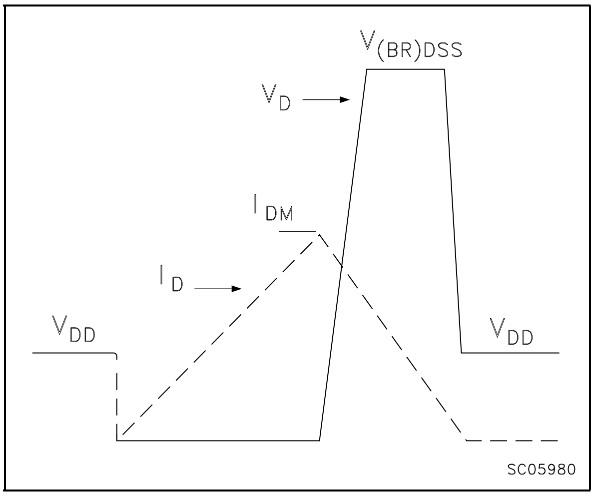
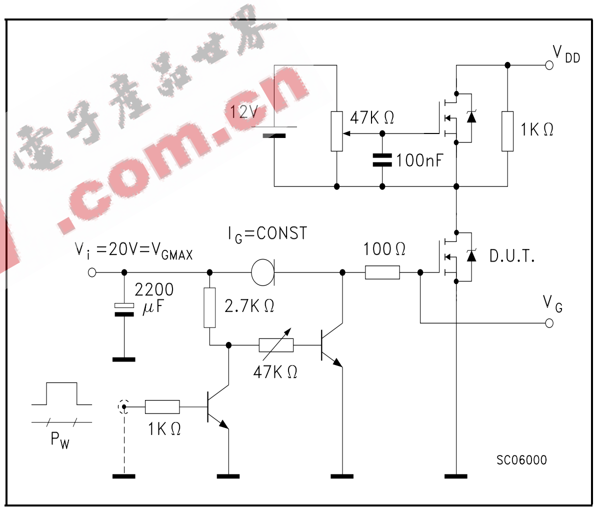
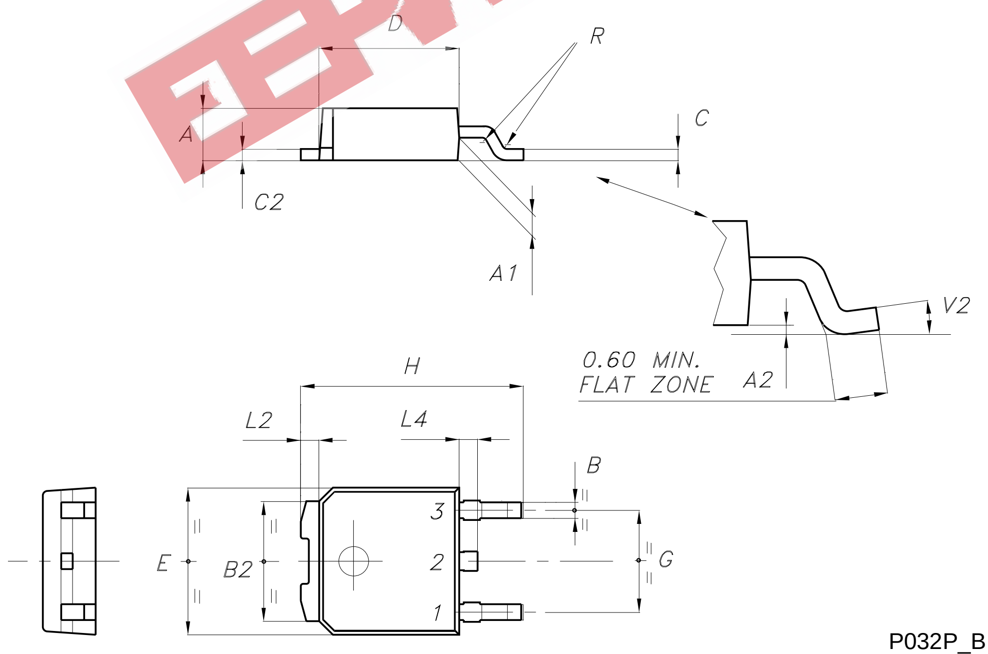



**Figure 19: Gate Charge Test Circuit**



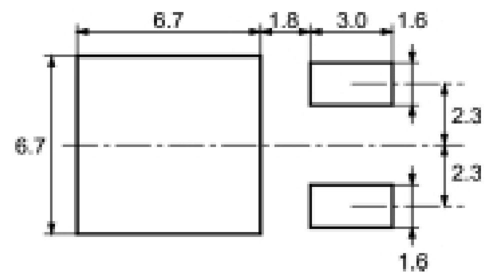
## TO-252 (DPAK) MECHANICAL DATA

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.20 | | 2.40 | 0.087 | | 0.094 |
| A1 | 0.90 | | 1.10 | 0.035 | | 0.043 |
| A2 | 0.03 | | 0.23 | 0.001 | | 0.009 |
| B | 0.64 | | 0.90 | 0.025 | | 0.035 |
| B2 | 5.20 | | 5.40 | 0.204 | | 0.213 |
| C | 0.45 | | 0.60 | 0.018 | | 0.024 |
| C2 | 0.48 | | 0.60 | 0.019 | | 0.024 |
| D | 6.00 | | 6.20 | 0.236 | | 0.244 |
| E | 6.40 | | 6.60 | 0.252 | | 0.260 |
| G | 4.40 | | 4.60 | 0.173 | | 0.181 |
| H | 9.35 | | 10.10 | 0.368 | | 0.398 |
| L2 | | 0.8 | | | 0.031 | |
| L4 | 0.60 | | 1.00 | 0.024 | | 0.039 |
| V2 | 0° | | 8° | 0° | | 0° |



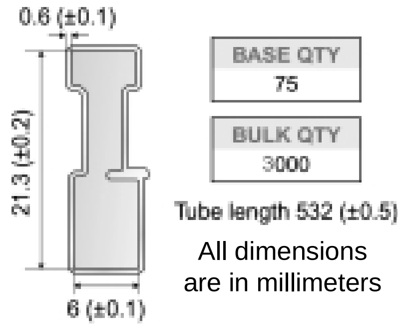

P032P_B

## DPAK FOOTPRINT



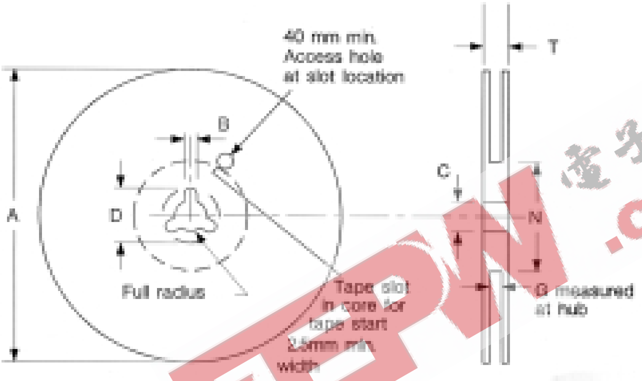

All dimensions are in millimeters

## TUBE SHIPMENT (no suffix)*




All dimensions are in millimeters

## TAPE AND REEL SHIPMENT (suffix ”T4”)*



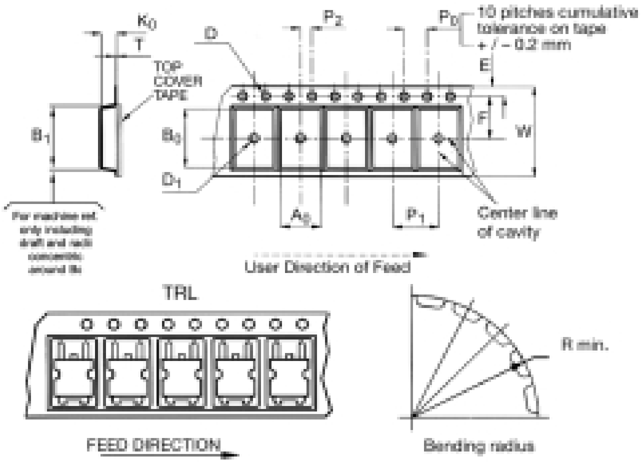

REEL MECHANICAL DATA

| DIM. | mm | | inch | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | | 330 | | 12.992 |
| B | 1.5 | | 0.059 | |
| C | 12.8 | 13.2 | 0.504 | 0.520 |
| D | 20.2 | | 0.795 | |
| G | 16.4 | 18.4 | 0.645 | 0.724 |
| N | 50 | | 1.968 | |
| T | | 22.4 | | 0.881 |

| BASE QTY | BULK QTY |
|---|---|
| 2500 | 2500 |

TAPE MECHANICAL DATA

| DIM. | mm | | inch | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A0 | 6.8 | 7 | 0.267 | 0.275 |
| B0 | 10.4 | 10.6 | 0.409 | 0.417 |
| B1 | | 12.1 | | 0.476 |
| D | 1.5 | 1.6 | 0.059 | 0.063 |
| D1 | 1.5 | | 0.059 | |
| E | 1.65 | 1.85 | 0.065 | 0.073 |
| F | 7.4 | 7.6 | 0.291 | 0.299 |
| K0 | 2.55 | 2.75 | 0.100 | 0.108 |
| P0 | 3.9 | 4.1 | 0.153 | 0.161 |
| P1 | 7.9 | 8.1 | 0.311 | 0.319 |
| P2 | 1.9 | 2.1 | 0.075 | 0.082 |
| R | 40 | | 1.574 | |
| W | 15.7 | 16.3 | 0.618 | 0.641 |

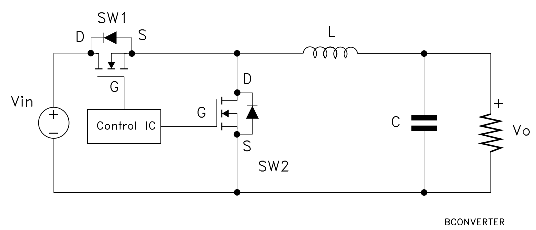



* on sales type

# Appendix A: Buck Converter Power Losses Estimation

## DESCRIPTION

The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.




| | | High Side Switch (SW1) | Low Side Switch (SW2) |
|---|---|---|---|
| $P_{conduction}$ | | $R_{DS(on)SW1} * I_L^2 * \delta$ | $R_{DS(on)SW2} * I_L^2 * (1-\delta)$ |
| $P_{switching}$ | | $V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$ | Zero Voltage Switching |
| $P_{diode}$ | Recovery | Not Applicable | $^{1}V_{in} * Q_{rr(SW2)} * f$ |
| | Conduction | Not Applicable | $V_{f(SW2)} * I_L * t_{deadtime} * f$ |
| $P_{gate(Q_G)}$ | | $Q_{g(SW1)} * V_{gg} * f$ | $\mathbf{Q_{gls(SW2)} * V_{gg} * f}$ |
| $P_{Qoss}$ | | $\frac{V_{in} * Q_{oss(SW1)} * f}{2}$ | $\frac{V_{in} * Q_{oss(SW2)} * f}{2}$ |

### The low side (SW2) device requires:

- Very low RDS(on) to reduce conduction losses
- Small $Q_{gls}$ to reduce the gate charge losses
- Small $C_{oss}$ to reduce losses due to output capaci tance
- Small $Q_{rr}$ to reduce losses on SW1 during its turn-on
- The $C_{gd}/C_{gs}$ ratio lower than $V_{th}/V_{GG}$ ratio especially with low drain to source voltage to avoid the cross conduction phenomenon

### The high side (SW1) device requires:

- Small $R_g$ and $L_s$ to allow higher gate current peak and to limit the voltage feedback on the gate
- Small $Q_g$ to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses

| Parameter | Meaning |
|---|---|
| δ | Duty-Cycle |
| $Q_{gsth}$ | Post Threshold Gate Charge |
| $Q_{gls}$ | Third Quadrant Gate Charge |
| Pconduction | On State Losses |
| Pswitching | On-off Transition Losses |
| Pdiode | Conduction and Reverse Recovery Diode Losses |
| Pdiode | Gate Drive Losses |
| $P_{Qoss}$ | Output Capacitance Losses |

**Table 8: Revision History**

| Date | Revision | Description of Changes |
|---|---|---|
| 27-Aug-2004 | 1 | First Release. |
| 10-Sep-2004 | 2 | Values changed in table 7 |