

STP80NF12

N-channel 120V - 0.013Ω - 80A - TO-220 STripFET™ II Power MOSFET

General features

Туре	V _{DSS} (@Tjmax)	R _{DS(on)}	I _D
STP80NF12	120V	<0.018Ω	80A ⁽¹⁾

- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization

Description

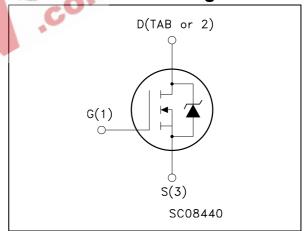
This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced highefficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

Applications

■ Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging	
STP80NF12	P80NF12	TO-220	Tube	

Contents STP80NF12

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STP80NF12 Electrical ratings

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Valu	е	l lmit
Symbol	Parameter	STB_P_W80NF12	STP80NF12FP	Unit
V _{DS}	Drain-source voltage (V _{GS} = 0)	120		V
V _{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	120		V
V _{GS}	Gate-source voltage	± 22	2	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25°C	80	11 ⁽²⁾	Α
I _D	Drain current (continuous) at T _C =100°C	60	60 ⁽²⁾	Α
I _{DM} ⁽³⁾	Drain current (pulsed)	320	320 ⁽²⁾	Α
P _{TOT}	Total dissipation at T _C = 25°C	300	45	W
	Derating factor	2.0	0.3	W/°C
dv/dt ⁽⁴⁾	Peak diode recovery voltage slope	10		V/ns
V _{ISO}	Insulation withstand voltage (DC)	34 34	2500	V
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to	175	°C

^{1.} Limited by Package

- 2. Limited only by maximum temperature allowed
- 3. Pulse width limited by safe operating area
- 4. Starting $T_J = 25$ °C, $I_D = 40A$, $V_{DD} = 45V$

Table 2. Thermal data

			Value			
Symbol	Parameter	TO-247	D ² PAK TO-220	TO-220FP	Unit	
R _{thJC}	Thermal resistance junction-case Max	0.5	0.5	3.33	°C/W	
R _{thJA}	Thermal resistance junction-ambient Max	50	62.5	62.5	°C/W	
T _I	Maximum lead temperature for soldering purpose	300	300	300	°C	

STP80NF12 **Electrical characteristics**

Electrical characteristics 2

(T_{CASE}=25°C unless otherwise specified)

On/off states Table 3.

Symbol	Parameter Test conditions		Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	120			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	$V_{DS} = Max rating,$ $V_{DS} = Max rating @ 125°C$			1 10	μ Α μ Α
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2			V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 40A		0.013	0.018	Ω

Table 4. **Dynamic**

Table 4.	Dynamic	4.48				
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	$V_{DS} = 15V$, $I_D = 40A$		80		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} =25V, f=1 MHz, V _{GS} =0		4300 600 230		pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 80V, I_{D} = 80A$ $V_{GS} = 10V$		140 23 51	189	nC nC nC

^{1.} Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 5. **Switching times**

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$\begin{array}{c} t_{d(on)} \\ t_{r} \\ t_{d(off)} \\ t_{f} \end{array}$	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 50 V, I_{D} = 40A, R_{G} =4.7 Ω , V_{GS} =10V Figure 13 on page 8		40 145 134 115		ns ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
I _{SD}	Source-drain current				80	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				320	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} =80A, V _{GS} =0			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} =80A, di/dt = 100A/ μ s, V_{DD} =35V, T_{J} = 150°C		155 0.85 11		ns µC A

- 1. Pulse width limited by safe operating area
- 2. Pulsed: pulse duration=300µs, duty cycle 1.5%



Electrical characteristics STP80NF12

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance

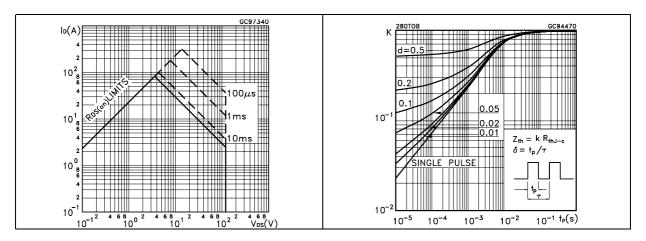


Figure 3. Output characteristics

Figure 4. Transfer characteristics

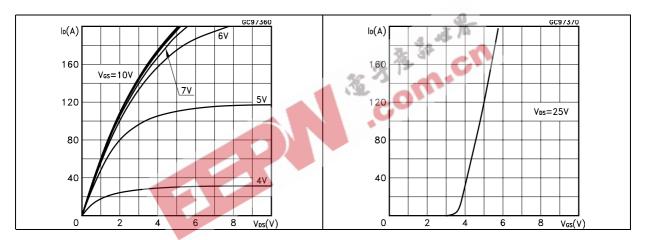
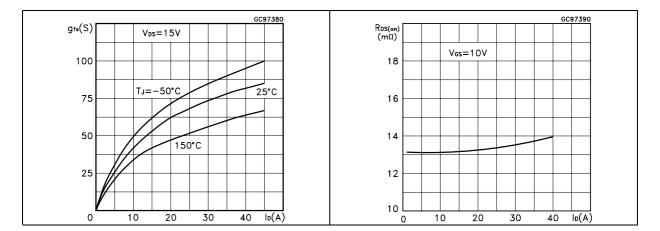


Figure 5. Transconductance

Figure 6. Static drain-source on resistance



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Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

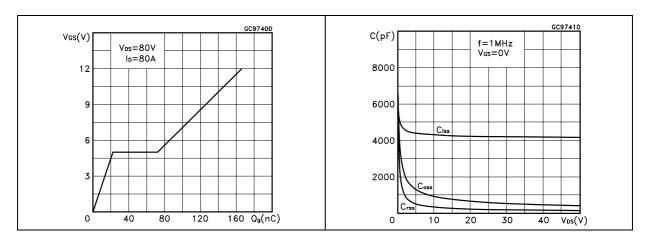


Figure 9. Normalized gate threshold voltage vs. temperature

Figure 10. Normalized on resistance vs. temperature

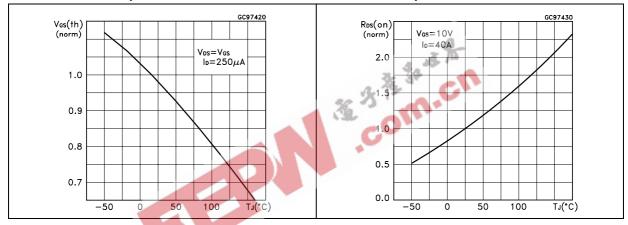
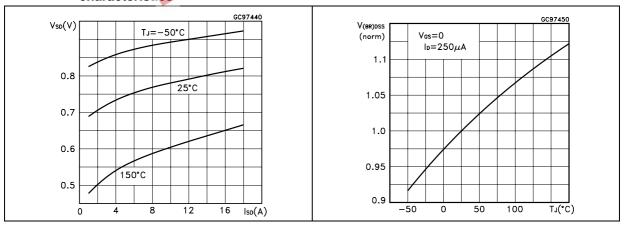


Figure 11. Source-drain diode forward characteristics

Figure 12. Normalized B_{VDSS} vs. temperature



Test circuit STP80NF12

3 Test circuit

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

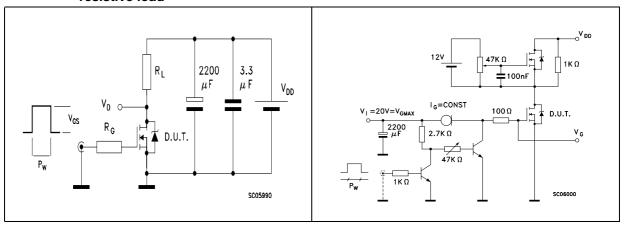


Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped Inductive load test circuit

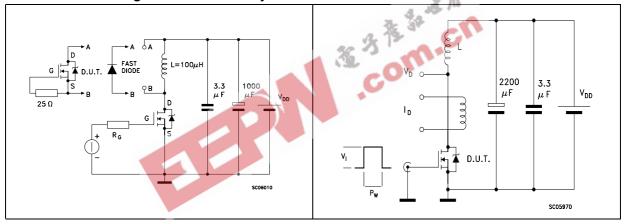
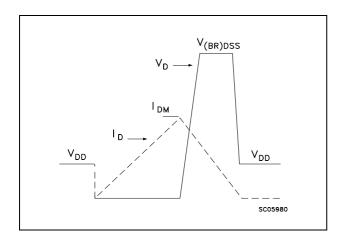


Figure 17. Unclamped inductive waveform



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4 Package mechanical data

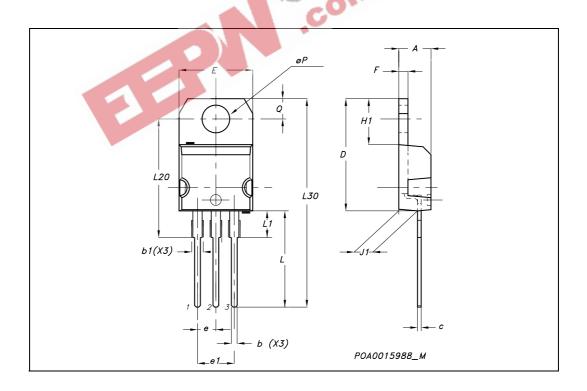
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TO-220 MECHANICAL DATA

DIM		mm.			inch	
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
С	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
Е	10		10.40	0.393		0.409
е	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40		4	0.645	
L30		28.90		4 15 14	1.137	
øΡ	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



STP80NF12 Revision history

5 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Jun-2004	2	Preliminary version
24-Jul-2006	3	The document has been reformatted, SOA updated
31-Jan-2007	4	Typo mistake on Table 1.



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