



STP45NF3LL - STP45NF3LLFP STB45NF3LL

N-CHANNEL 30V - 0.014Ω - 45A TO-220 - TO220FP - D²PAK
STripFET II™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP45NF3LL	30 V	<0.018Ω	45 A
STP45NF3LLFP	30 V	<0.018Ω	45 A
STB45NF3LL	30 V	<0.018Ω	27 A

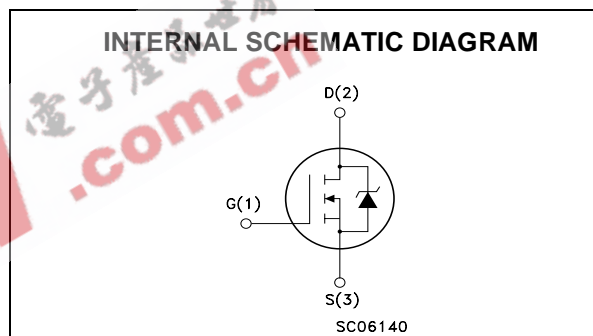
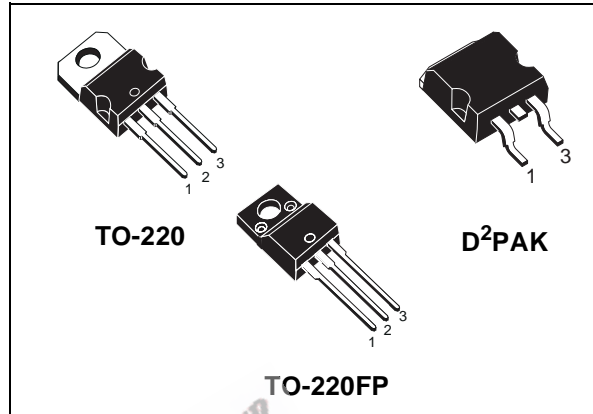
- TYPICAL R_{DS(on)} = 0.014Ω @4.5V
- OPTIMAL R_{DS(ON)} x Q_g TRADE-OFF @ 4.5V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

DESCRIPTION

This application specific Power MOSFET is the third generation of STMicroelectronics unique "Single Feature™" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		TO-220/D ² PAK	TO-220FP	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30		V
V _{GS}	Gate- source Voltage	± 16		V
I _D	Drain Current (continuous) at T _C = 25°C	45	27	A
I _D	Drain Current (continuous) at T _C = 100°C	32	19	A
I _{DM} (●)	Drain Current (pulsed)	180	108	A
P _{TOT}	Total Dissipation at T _C = 25°C	70	25	W
	Derating Factor	0.46	0.167	W/°C
E _{AS} (1)	Single Pulse Avalanche Energy	241		mJ
V _{iso}	Insulation Withstand Voltage (DC)	--	2500	V
T _{stg}	Storage Temperature	- 55 to 175		°C
T _j	Max. Operating Junction Temperature			

(●) Pulse width limited by safe operating area
November 2002

(1) Starting T_j = 25°C, I_D = 22.5A, V_{DD} = 24V

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THERMAL DATA

		TO-220 D ² PAK	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	2.14	6	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5		°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300		°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16 V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 22.5 A V _{GS} = 4.5V, I _D = 22.5 A		0.014 0.016	0.018 0.020	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15 V, I _D = 22.5 A		20		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		800		pF
C _{oss}	Output Capacitance			250		pF
C _{rss}	Reverse Transfer Capacitance			60		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}, I_D = 22.5\text{ A}$		17		ns
t_r	Rise Time	$R_G = 4.7\Omega, V_{GS} = 4.5\text{ V}$ (Resistive Load, see Fig. 3)		100		ns
Q_g	Total Gate Charge	$V_{DD} = 24\text{ V}, I_D = 45\text{ A},$		12.5	17	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 5\text{ V}$		4.6		nC
Q_{gd}	Gate-Drain Charge			5.2		nC

SWITCHING OFF

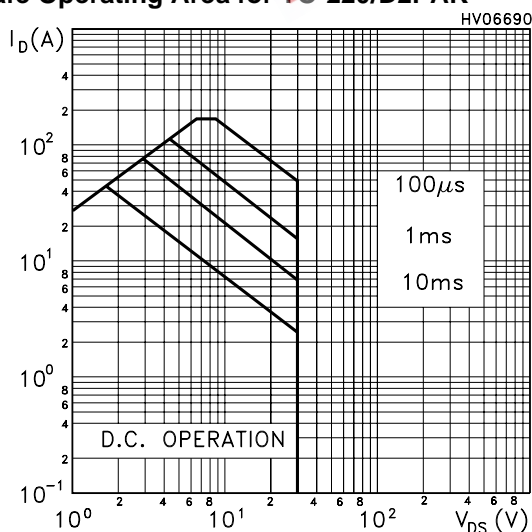
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 15\text{ V}, I_D = 22.5\text{ A},$		20		ns
t_f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 4.5\text{ V}$ (Resistive Load, see Fig. 3)		21		ns

SOURCE DRAIN DIODE

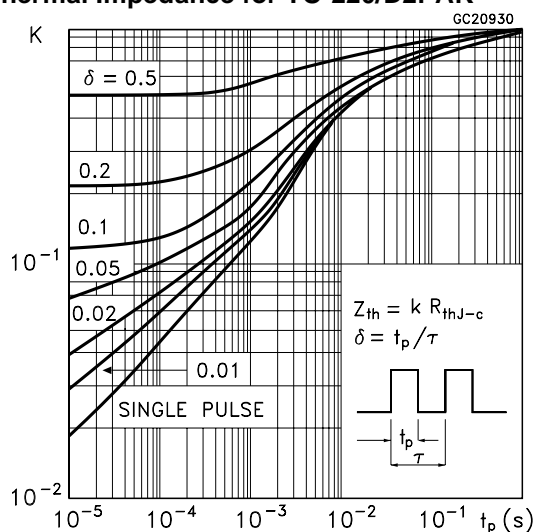
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				45	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				180	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 45\text{ A}, V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 45\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$		35		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 15\text{ V}, T_J = 150^\circ\text{C}$		44		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		2.5		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Safe Operating Area for TO-220/D2PAK

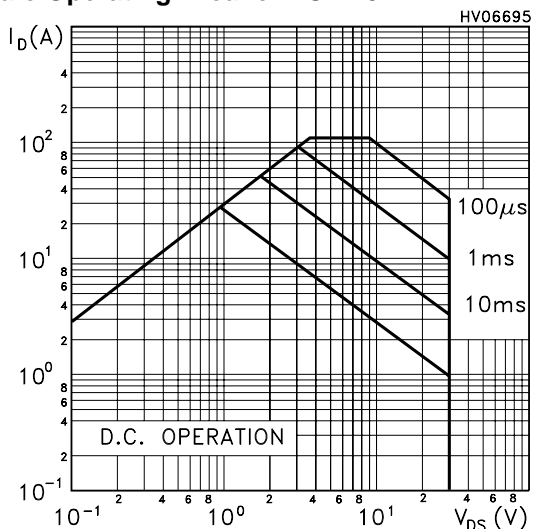


Thermal Impedance for TO-220/D2PAK

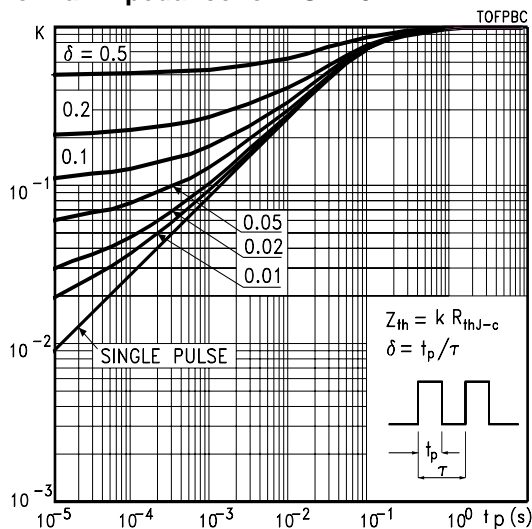


STP45NF3LL - STB45NF3LL

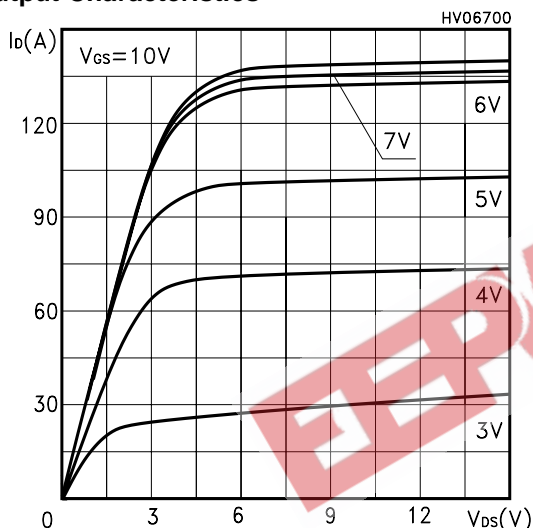
Safe Operating Area for TO-220FP



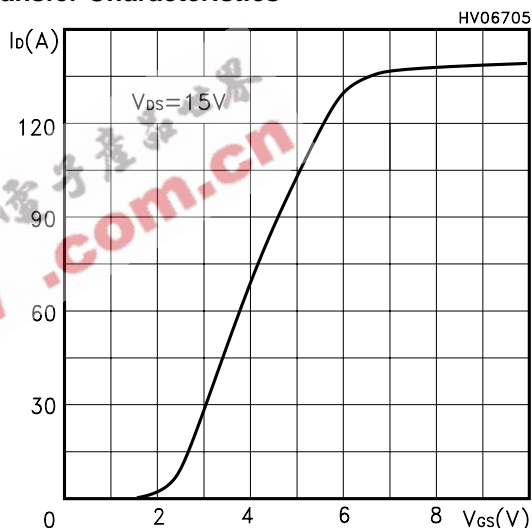
Thermal Impedance for TO-220FP



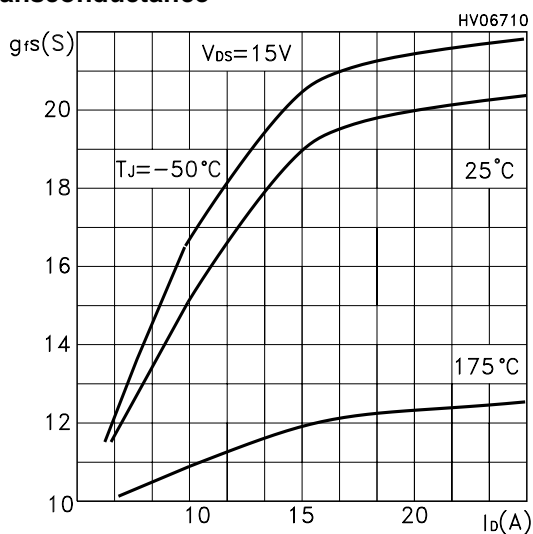
Output Characteristics



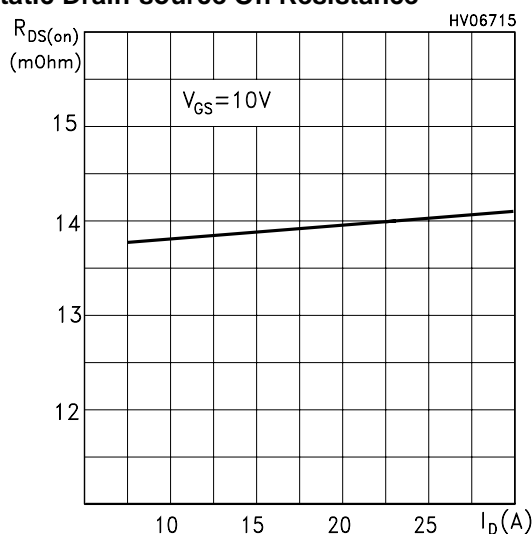
Transfer Characteristics



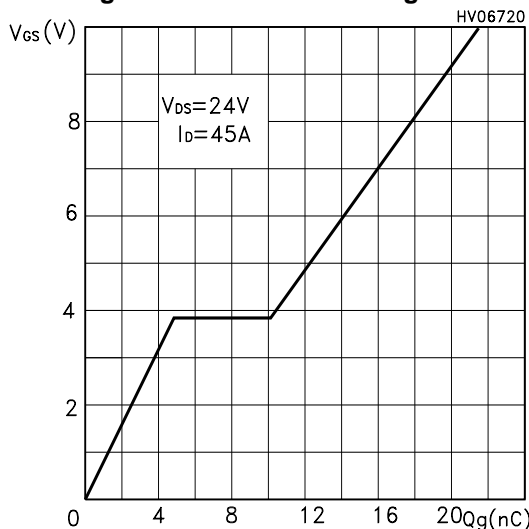
Transconductance



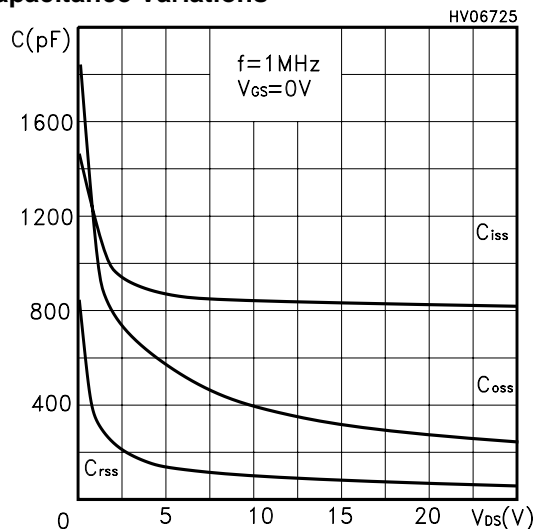
Static Drain-source On Resistance



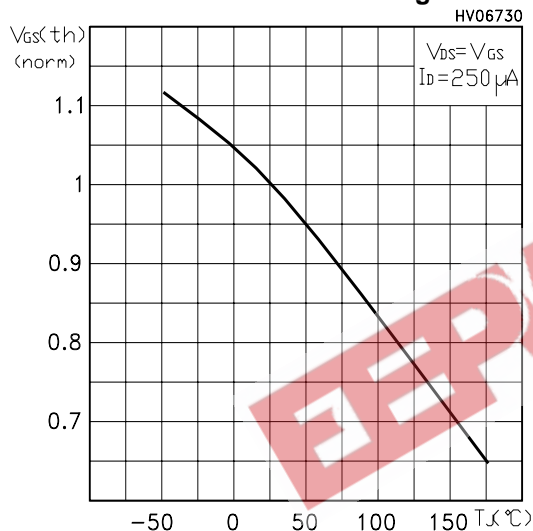
Gate Charge vs Gate-source Voltage



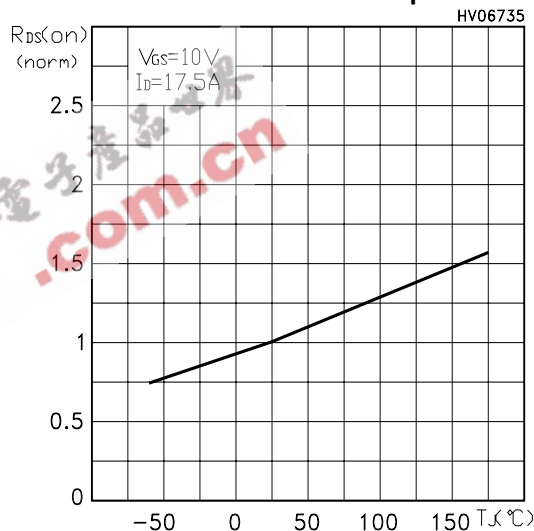
Capacitance Variations



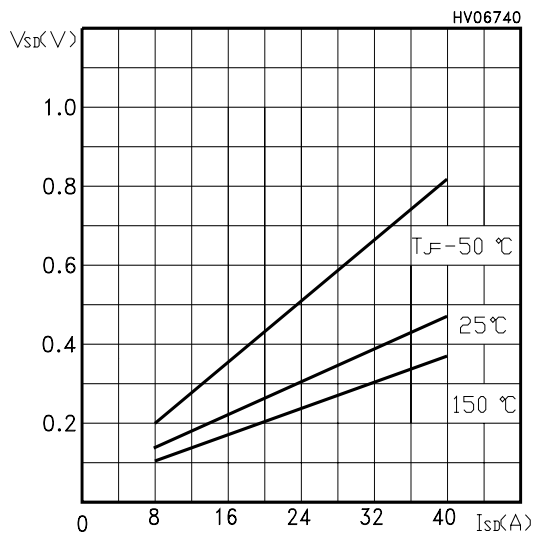
Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Tj

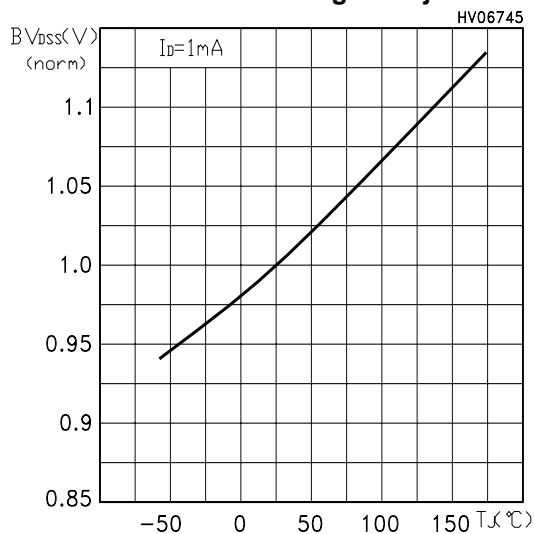


Fig. 1: Unclamped Inductive Load Test Circuit

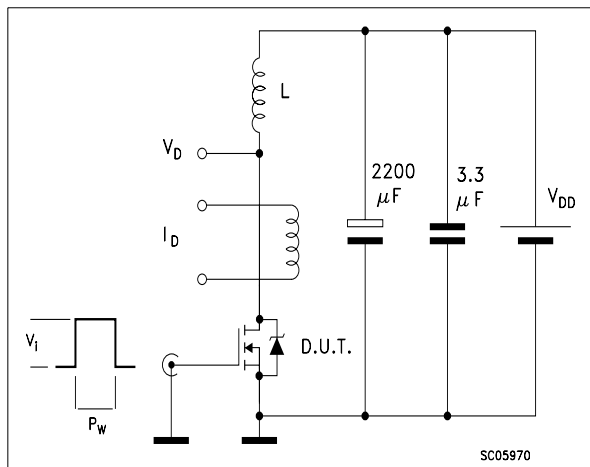


Fig. 2: Unclamped Inductive Waveform

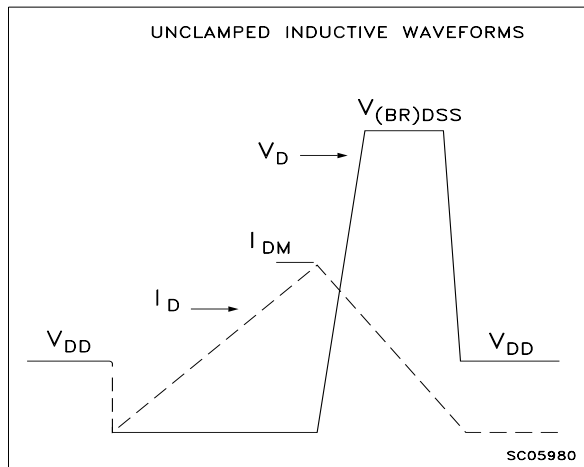


Fig. 3: Switching Times Test Circuit For Resistive Load

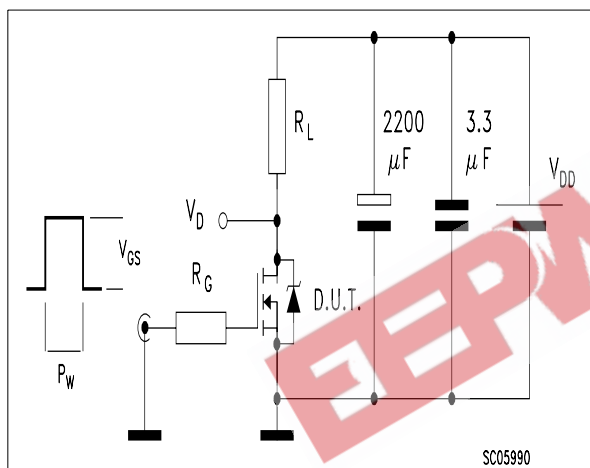


Fig. 4: Gate Charge test Circuit

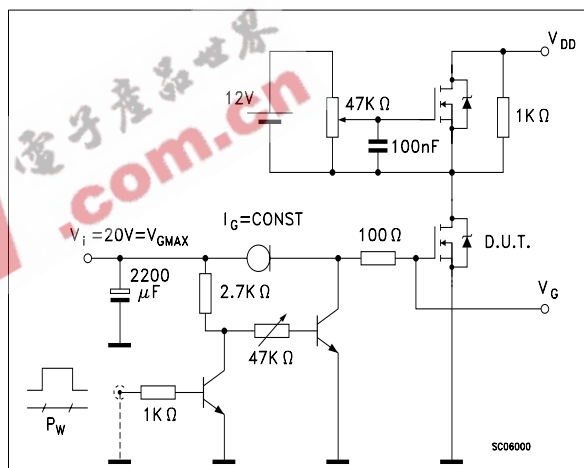
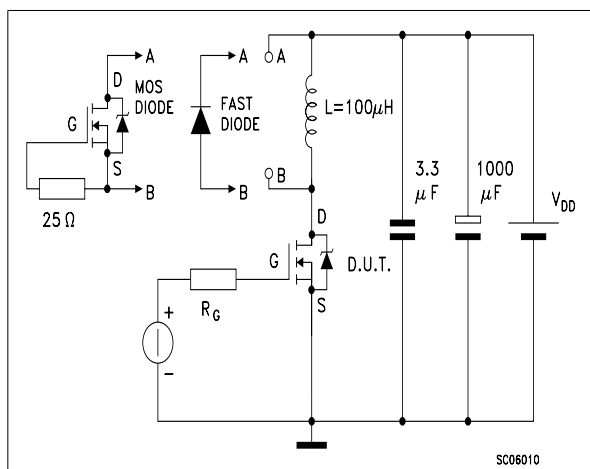
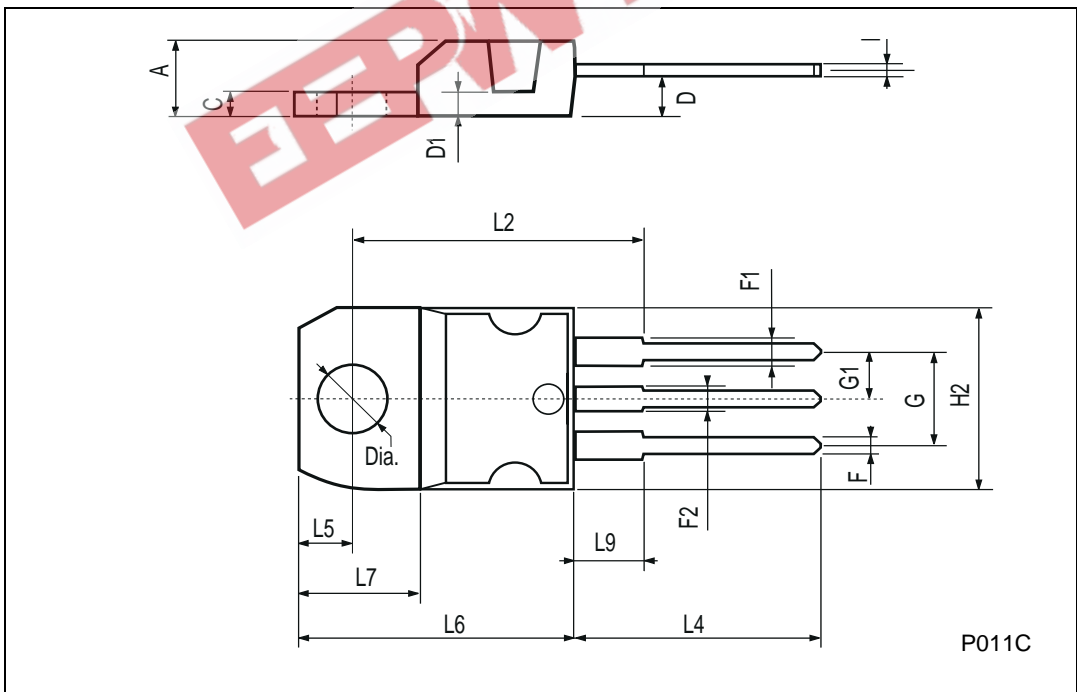


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



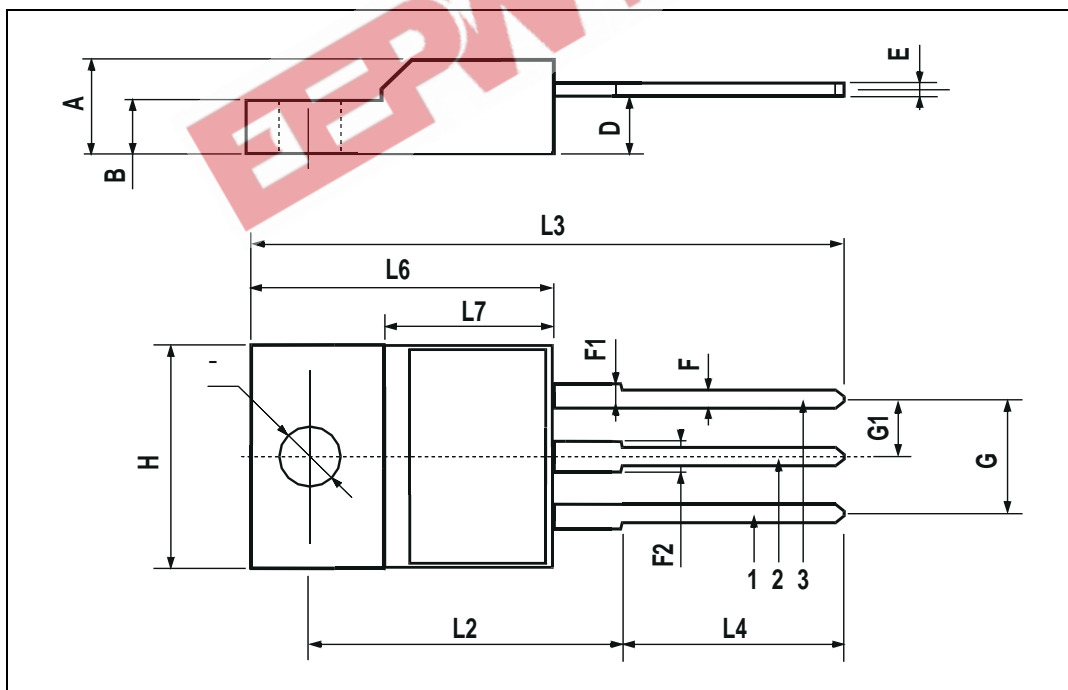
TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



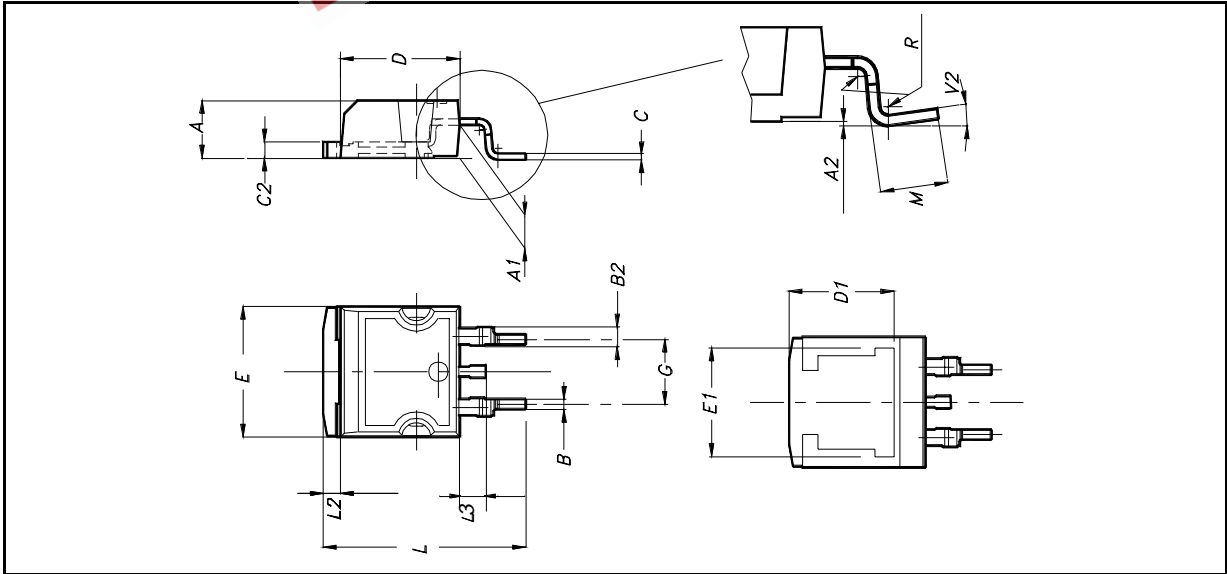
TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



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