



ST1S12xx

Synchronous rectification with enable, 0.7 A, 1.7 MHz fixed or adjustable step-down switching regulator in TSOT23-5L

Features

- Step-down current mode PWM (1.7 MHz) DC-DC converter
- 3% DC output voltage tolerance
- Synchronous rectification
- Fixed output voltage 1.2 V, 1.8 V, and ADJ (available on request 1.5 V, 2.5 V and 3.3 V)
- Enable function
- Internal soft start
- Typical efficiency: > 90%
- 0.7 A output current capability
- Not switching quiescent current: max 600 μ A over temperature range
- $R_{DS(ON)}$ typ. 250 m Ω and 400 m Ω
- Uses tiny capacitors and inductors
- Operative junction temp. -40°C to 125°C
- Available in TSOT23-5L package



required. Moreover, a low output ripple is guaranteed by the current mode PWM topology and by the use of low ESR SMD ceramic capacitors. The device is thermally protected and the current is limited to prevent damage due to accidental short-circuit. The ST1S12Gxx is available in the TSOT23-5L package.

Description

The ST1S12Gxx is a step down DC-DC converter optimized for powering low-voltage digital cores in HDD applications and, generally, to replace the high current linear solution when the power dissipation may cause high heating of the application environment. It provides up to 0.7 A over an input voltage range of 2.5 V to 5.5 V. A high switching frequency (1.7 MHz) allows the use of tiny surface-mount components. In addition to the resistor divider to set the output voltage value, only an inductor and two capacitors are

Table 1. Device summary

Part numbers	Order codes	Package
ST1S12XX	ST1S12GR	TSOT23-5L
ST1S12XX12	ST1S12G12R	TSOT23-5L
ST1S12XX18	ST1S12G18R ⁽¹⁾	TSOT23-5L

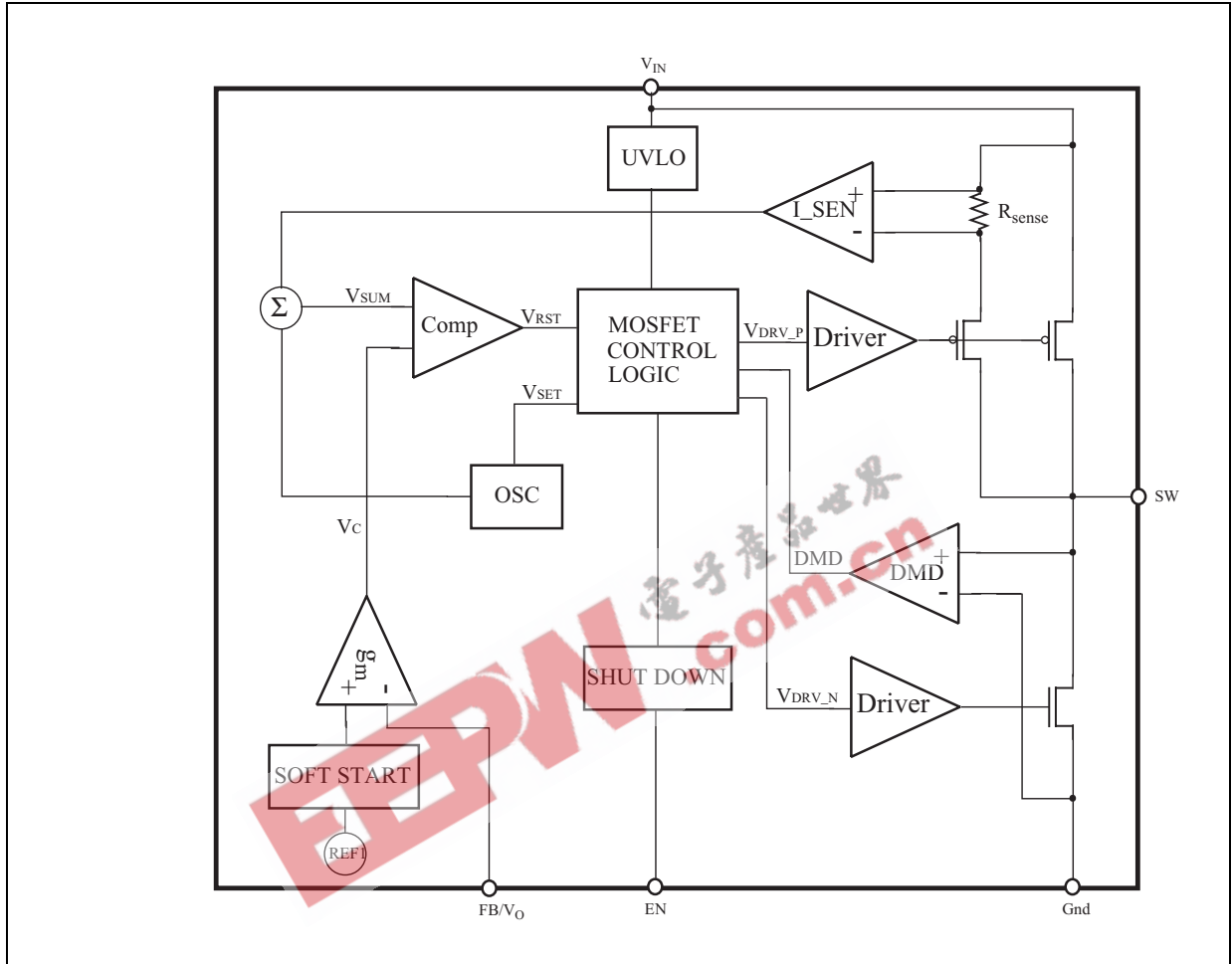
1. Available on request.

Contents

1	Schematic	3
2	Pin configuration	4
3	Maximum ratings	5
4	Electrical characteristics	6
5	Typical application	9
6	Application notes	10
7	Typical performance characteristics	11
8	Package mechanical data	15
9	Revision history	19

1 Schematic

Figure 1. Schematic diagram



2 Pin configuration

Figure 2. Pin connections (top view)

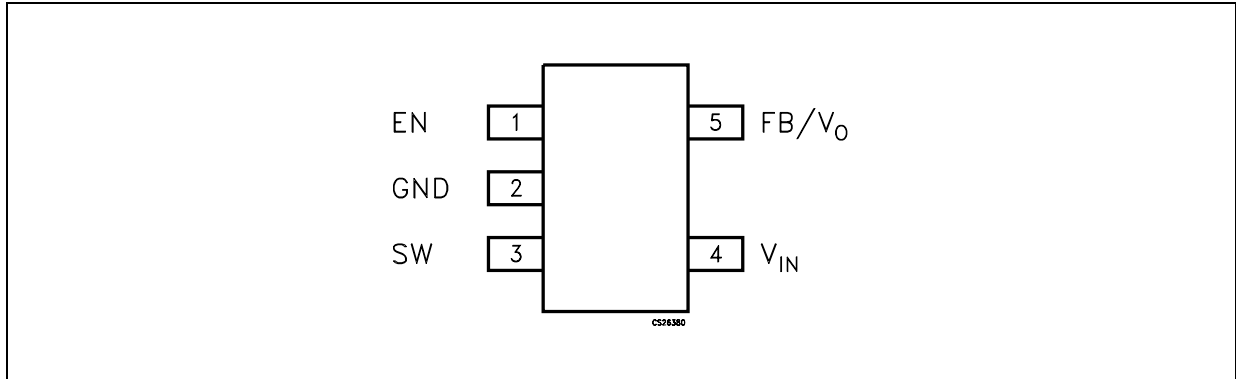


Table 2. Pin description

Pin n°	Symbol	Name and function
1	EN	Enable pin
2	GND	System ground
3	SW	Switching pin
4	V _{IN}	Input supply pin
5	FB/V _O	Feedback voltage / or output voltage

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Positive power supply voltage	-0.3 to 7	V
V_{EN}	Enable voltage	-0.3 to $V_{IN} + 0.3$	V
SWITCH Voltage	Max. voltage of output pin	-0.3 to $V_{IN} + 0.3$	V
V_{FB}/V_O	Feedback voltage	-0.3 to 3	V
V_O	Output voltage (for $V_O > 1.6V$)	-0.3 to 6	V
T_J	Max junction temperature	-40 to 150	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering) 10 sec	260	°C

Note: Absolute maximum ratings are the values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	220	°C/W
R_{thJC}	Thermal resistance junction-case	110	°C/W

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		MM	0.3	kV

4 Electrical characteristics

Table 6. Electrical characteristics for ST1S12G

$V_{IN}=V_{EN}=3.6\text{ V}$, $C_{IN}=4.7\text{ }\mu\text{F}$, $C_O=10\text{ }\mu\text{F}$, $L=2.2\text{ }\mu\text{H}$, $T_J=-40\text{ to }125\text{ }^\circ\text{C}$ (unless otherwise specified. Typical values are referred to $25\text{ }^\circ\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
FB	Feedback voltage	$T_J=-40\text{ to }125\text{ }^\circ\text{C}$	582	600	618	V
I_{FB}	V_{FB} pin bias current		-50		50	nA
V_{IN}	Minimum input voltage	$I_O=10\text{ mA to }0.7\text{ A}$	2.5			V
I_Q	Quiescent current	$V_{IN}=V_{EN}$, $V_{FB}=0.65\text{ V}$		500	600	μA
		$V_{EN}=0$, $T=-40\text{ }^\circ\text{C to }85\text{ }^\circ\text{C}$			1	μA
I_O	Output current	$V_{IN}=2.5\text{ to }5.5\text{ V}$ <i>Note 1</i>	0.7			A
V_{EN}	Enable threshold	Device ON, $V_{IN}=2.5\text{ to }5.5\text{ V}$	1.5			V
		Device OFF			0.5	
I_{EN}	Enable pin current				1	μA
$\%V_O/\Delta V_{IN}$	Reference line regulation	$V_{IN}=2.5\text{ V to }5.5\text{ V}$ <i>Note 1</i>		0.05	0.1	$\%V_O/\Delta V_{IN}$
$\%V_O/\Delta I_O$	Reference load regulation	$I_O=10\text{ mA to }700\text{ mA}$ <i>Note 1</i>		0.0025	0.005	$\%V_O/\text{mA}$
$\text{PWM}f_S$	PWM switching frequency		1.16	1.7	2.08	MHz
D_{MAX}	Maximum duty cycle				100	%
R_{DSON-N}	NMOS switch on resistance	$I_{SW}=100\text{ mA}$		0.25	0.4	Ω
R_{DSON-P}	PMOS switch on resistance	$I_{SW}=100\text{ mA}$		0.25	0.45	Ω
I_{SWL}	Switching current limitation	<i>Note 1</i>		1.6		A
ν	Efficiency <i>Note 1</i>	$I_O=10\text{ mA to }100\text{ mA}$, $V_O=1.8\text{ V}$		80		%
		$I_O=100\text{ mA to }0.7\text{ A}$, $V_O=1.8\text{ V}$		90		
T_{SHDN}	Thermal shutdown		130	150		$^\circ\text{C}$
T_{HYS}	Thermal shutdown hysteresis			15		$^\circ\text{C}$
$\%V_O/\Delta I_O$	Load transient response	$I_O=100\text{ mA to }700\text{ mA}$, $T_A=25\text{ }^\circ\text{C}$ $t_R=t_F \geq 200\text{ ns}$, $C_O=22\text{ }\mu\text{F}$ <i>Note 1</i>	-5		+5	$\%V_O$
$\%V_O/\Delta I_O$	Short circuit removal response	$I_O=10\text{ mA to }I_O=\text{short}$, $T_A=25\text{ }^\circ\text{C}$ <i>Note 1</i>	-10		+10	$\%V_O$

Note: 1 Guaranteed by design, but not tested in production.

Table 7. Electrical characteristics for ST1S12G12

$V_{IN} = V_{EN} = 3\text{ V}$, $C_{IN} = 4.7\text{ }\mu\text{F}$, $C_O = 10\text{ }\mu\text{F}$, $L = 2.2\text{ }\mu\text{H}$, $T_J = -40\text{ to }125\text{ }^\circ\text{C}$ (unless otherwise specified. Typical values are referred to $25\text{ }^\circ\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OUT	Output feedback pin	$T_J = -40\text{ to }125\text{ }^\circ\text{C}$	1.164	1.2	1.236	V
I_O	V_O pin bias current			15	20	μA
V_{IN}	Minimum input voltage	$I_O = 10\text{ mA to }0.7\text{ A}$	2.5			V
I_Q	Quiescent current	$V_{IN} = V_{EN}$, $V_{FB} = 1.5\text{ V}$		500	600	μA
		$V_{EN} = 0$, $T = -40\text{ }^\circ\text{C to }85\text{ }^\circ\text{C}$			1	μA
I_O	Output current	$V_{IN} = 2.5\text{ to }5.5\text{ V}$ <i>Note 1</i>	0.7			A
V_{EN}	Enable threshold	Device ON, $V_{IN} = 2.5\text{ to }5.5\text{ V}$	1.5			V
		Device OFF			0.5	
I_{EN}	Enable pin current				1	μA
$\%V_O/\Delta V_{IN}$	Reference line regulation	$V_{IN} = 2.5\text{ V to }5.5\text{ V}$ <i>Note 1</i>		0.05	0.1	$\%V_O/\Delta V_{IN}$
$\%V_O/\Delta I_O$	Reference load regulation	$I_O = 10\text{ mA to }700\text{ mA}$ <i>Note 1</i>		0.0025	0.005	$\%V_O/\text{mA}$
$\text{PWM}f_S$	PWM switching frequency		1.16	1.7	2.08	MHz
$R_{\text{DSON-N}}$	NMOS switch on resistance	$I_{\text{SW}} = 100\text{ mA}$		0.25	0.4	Ω
$R_{\text{DSON-P}}$	PMOS switch on resistance	$I_{\text{SW}} = 100\text{ mA}$		0.25	0.45	Ω
I_{SWL}	Switching current limitation	<i>Note 1</i>		1.6		A
ν	Efficiency <i>Note 1</i>	$I_O = 10\text{ mA to }100\text{ mA}$		80		%
		$I_O = 100\text{ mA to }0.7\text{ A}$		85		
T_{SHDN}	Thermal shutdown		130	150		$^\circ\text{C}$
T_{HYS}	Thermal shutdown hysteresis			15		$^\circ\text{C}$
$\%V_O/\Delta I_O$	Load transient response	$I_O = 100\text{ mA to }700\text{ mA}$, $T_A = 25\text{ }^\circ\text{C}$ $t_R = t_F \geq 200\text{ ns}$, $C_O = 22\text{ }\mu\text{F}$ <i>Note 1</i>	-5		+5	$\%V_O$
$\%V_O/\Delta I_O$	Short circuit removal response	$I_O = 10\text{ mA to }I_O = \text{short}$, $T_A = 25\text{ }^\circ\text{C}$ <i>Note 1</i>	-10		+10	$\%V_O$

Note: 1 Guaranteed by design, but not tested in production.

Table 8. Electrical characteristics for ST1S12G18

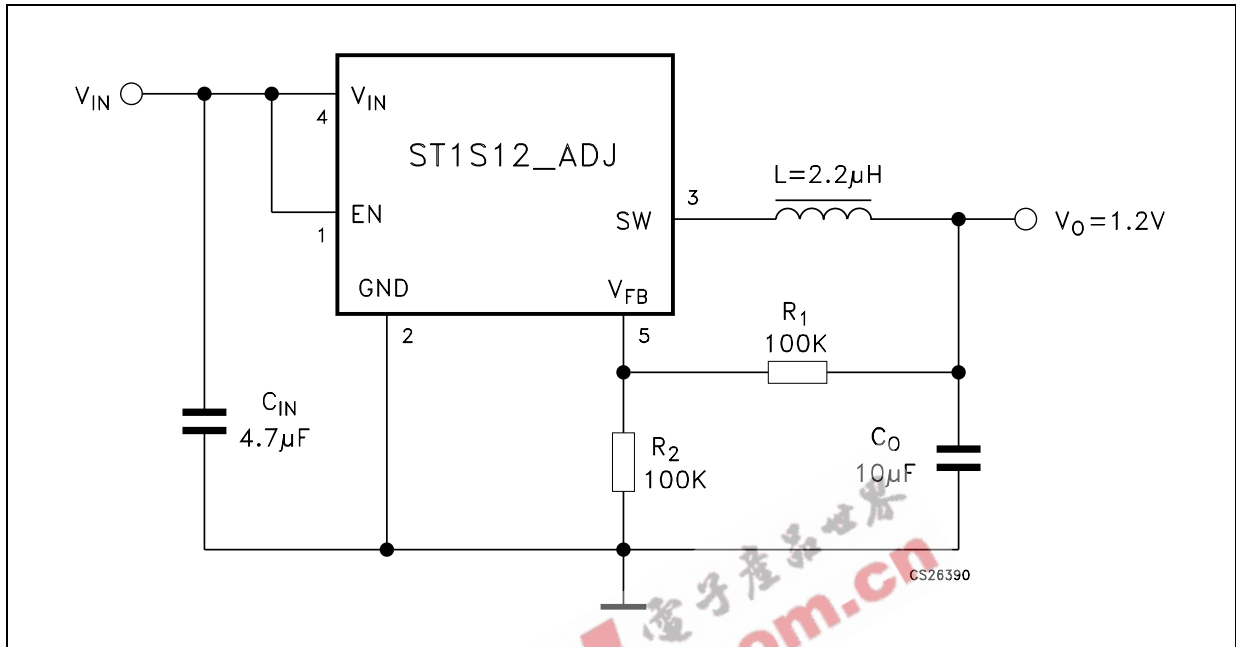
$V_{IN} = V_{EN} = 3.6$ V, $C_{IN} = 4.7$ μ F, $C_O = 10$ μ F, $L = 2.2$ μ H, $T_J = -40$ to 125 $^{\circ}$ C (unless otherwise specified. Typical values are referred to 25 $^{\circ}$ C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OUT	Output feedback pin	$T_J = -40$ to 125°C	1.746	1.8	1.854	V
I_O	V_O pin bias current			15	20	μA
V_{IN}	Minimum input voltage	$I_O = 10\text{mA}$ to 0.7A	2.5			V
I_Q	Quiescent current	$V_{IN} = V_{EN}$, $V_{FB} = 2\text{V}$		500	600	μA
		$V_{EN} = 0$, $T = -40^{\circ}\text{C}$ to 85°C			1	μA
I_O	Output current	$V_{IN} = 2.5$ to 5.5V <i>Note 1</i>	0.7			A
V_{EN}	Enable threshold	Device ON, $V_I = 2.5$ to 5.5V	1.5			V
		Device OFF			0.5	
I_{EN}	Enable pin current				1	μA
$\%V_O/\Delta V_{IN}$	Reference line regulation	$V_{IN} = 2.5\text{V}$ to 5.5V <i>Note 1</i>		0.05	0.1	$\%V_O/\Delta V_{IN}$
$\%V_O/\Delta I_O$	Reference load regulation	$I_O = 10\text{mA}$ to 700mA <i>Note 1</i>		0.0025	0.005	$\%V_O/\text{mA}$
PWMf_S	PWM switching frequency		1.16	1.7	2.08	MHz
$R_{\text{DSON-N}}$	NMOS switch on resistance	$I_{\text{SW}} = 100$ mA		0.25	0.4	Ω
$R_{\text{DSON-P}}$	PMOS switch on resistance	$I_{\text{SW}} = 100$ mA		0.25	0.45	Ω
I_{SWL}	Switching current limitation	<i>Note 1</i>		1.6		A
ν	Efficiency <i>Note 1</i>	$I_O = 10\text{mA}$ to 100mA		80		%
		$I_O = 100\text{mA}$ to 0.7A		90		
T_{SHDN}	Thermal shutdown		130	150		$^{\circ}\text{C}$
T_{HYS}	Thermal shutdown hysteresis			15		$^{\circ}\text{C}$
$\%V_O/\Delta I_O$	Load transient response	$I_O = 100\text{mA}$ to 700mA , $T_A = 25^{\circ}\text{C}$ $t_R = t_F \geq 200\text{ns}$, $C_O = 22\mu\text{F}$ <i>Note 1</i>	-5		+5	$\%V_O$
$\%V_O/\Delta I_O$	Short circuit removal response	$I_O = 10\text{mA}$ to $I_O = \text{short}$, $T_A = 25^{\circ}\text{C}$ <i>Note 1</i>	-10		+10	$\%V_O$

Note: 1 Guaranteed by design, but not tested in production.

5 Typical application

Figure 3. Application circuit



6 Application notes

The ST1S12Gxx is an adjustable current mode PWM step-down DC-DC converter with internal 0.7 A power switch, packaged in TSOT23-5L. This device is a complete 0.7 A switching regulator, with its internal compensation eliminating the need for additional components.

Because the ST1S12Gxx an adjustable regulator, the output voltage is determined by an external resistor divider. The desired value is derived by the following equation:

$$V_O = V_{FB}[1+R_1/R_2]$$

For the device to function only a few component are required: an inductor, two capacitors and the resistor divider. The inductor selected must be capable of non saturation at peak current level. Moreover, its value can be selected taking into account that a large inductor value increases efficiency at low output current and reduces output voltage ripple, while a smaller inductor can be used when it is important to reduce package size and the total cost of the application. Finally, the ST1S12Gxx has been designed to work properly with X5R or X7R SMD ceramic capacitors both at the input and at the output. These types of capacitors, due to their very low series resistance (ESR), minimize the output voltage ripple. Other low ESR capacitors can be used according to the need of the application without compromising the correct functioning of the device.

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7 Typical performance characteristics

Unless otherwise specified, refer to the typical application circuit under the following conditions: $C_{IN} = 4.7 \mu\text{F}$, $C_{OUT} = 10 \mu\text{F}$, $L = 2.2 \mu\text{H}$

Figure 4. Voltage feedback vs temperature

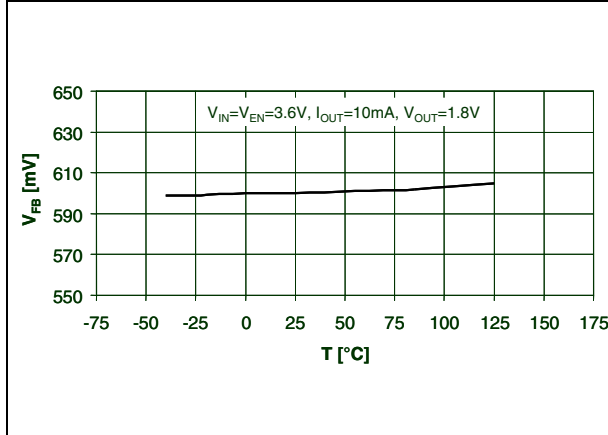


Figure 5. Drop vs temperature

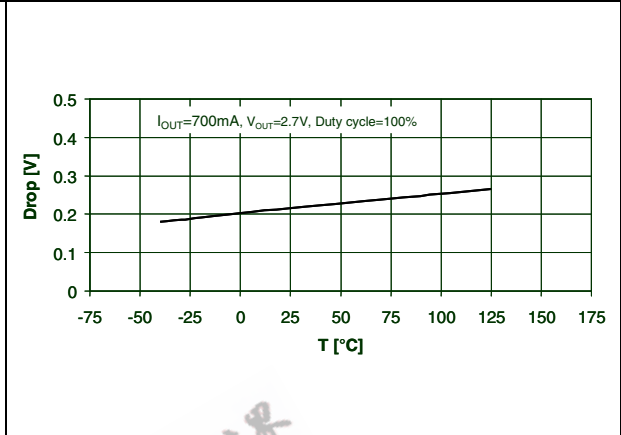


Figure 6. Oscillator frequency vs temperature

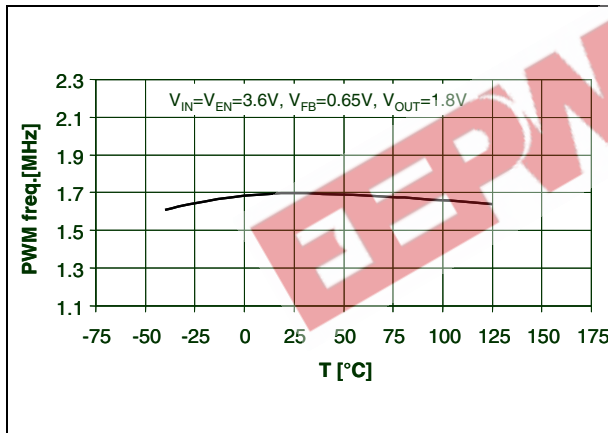


Figure 7. Efficiency vs output current

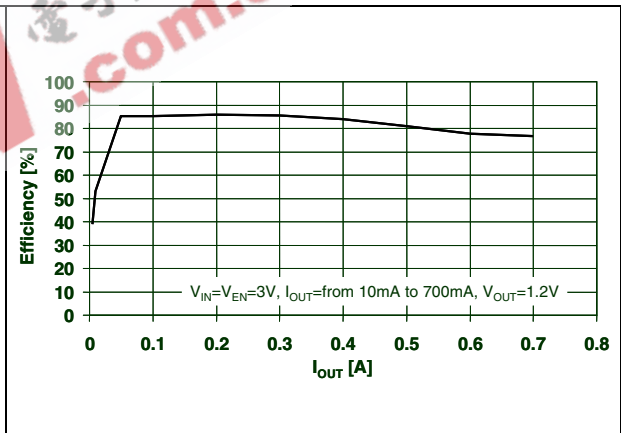


Figure 8. Efficiency vs output current

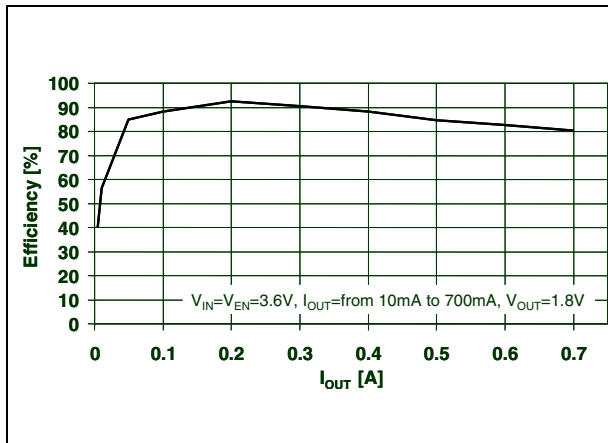


Figure 9. Efficiency vs temperature

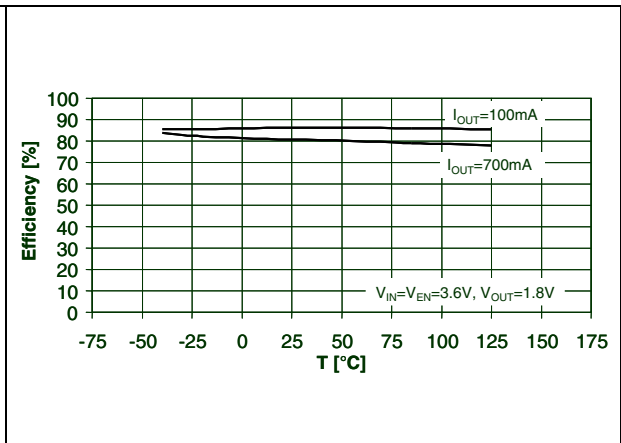


Figure 10. Efficiency vs temperature

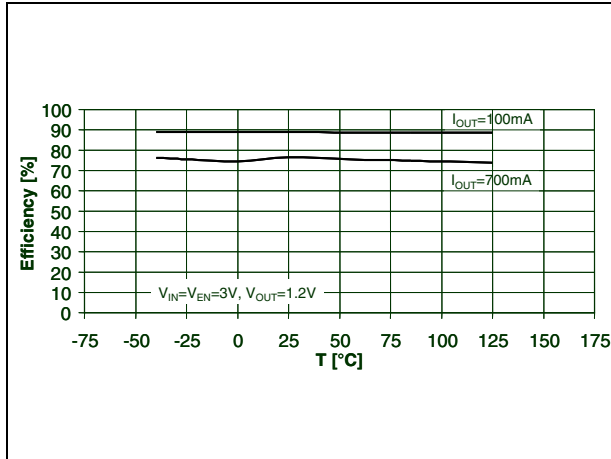


Figure 11. Supply current vs temperature

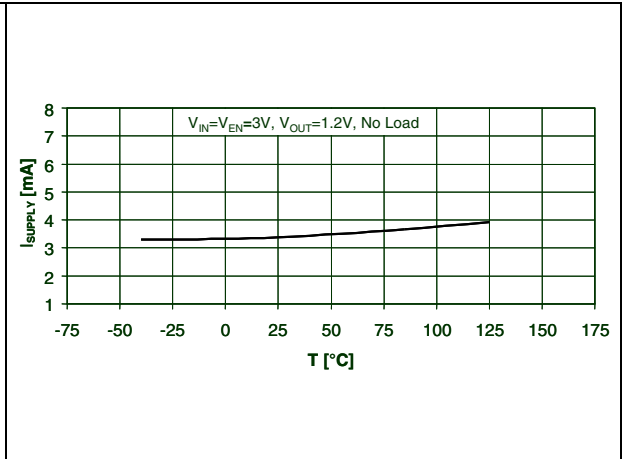


Figure 12. Quiescent current vs temperature

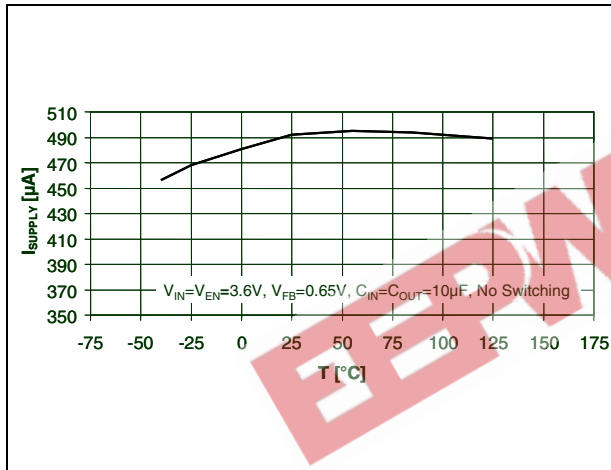


Figure 13. Enable voltage vs temperature

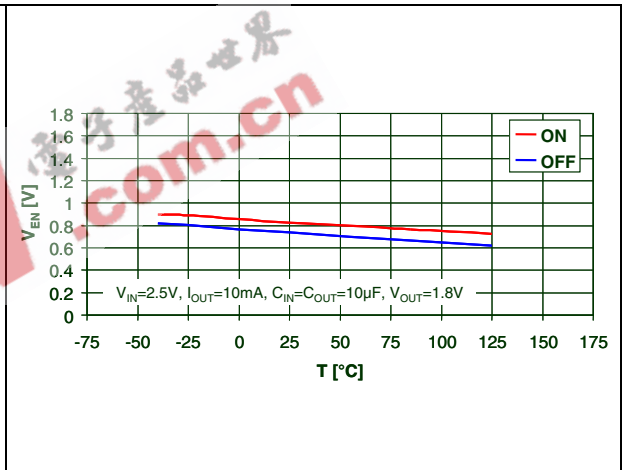


Figure 14. Enable voltage vs temperature

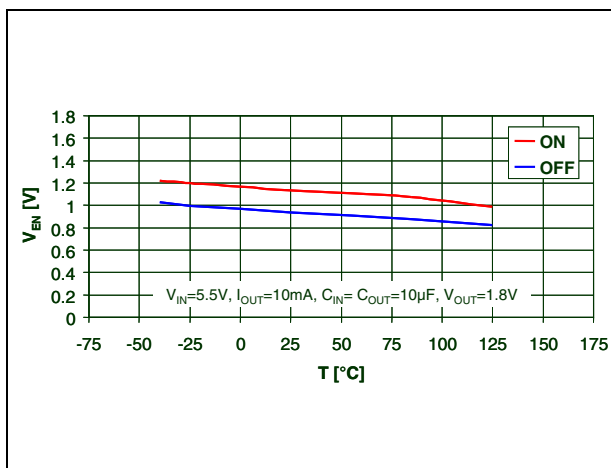


Figure 15. Reference line regulation vs temperature

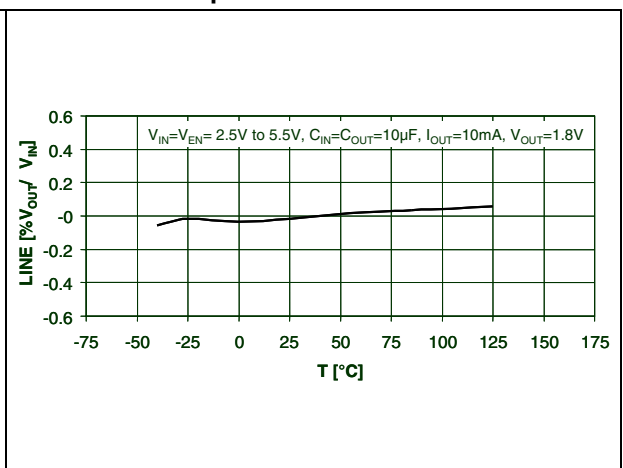


Figure 16. Reference load regulation vs temperature

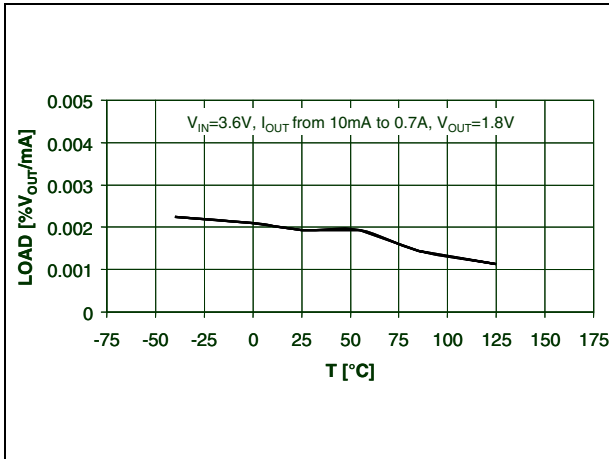


Figure 17. NMOS switch on resistance vs temperature

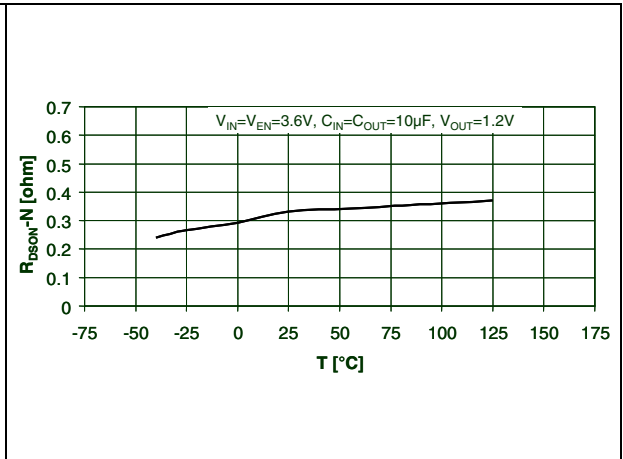


Figure 18. PMOS switch on resistance vs temperature

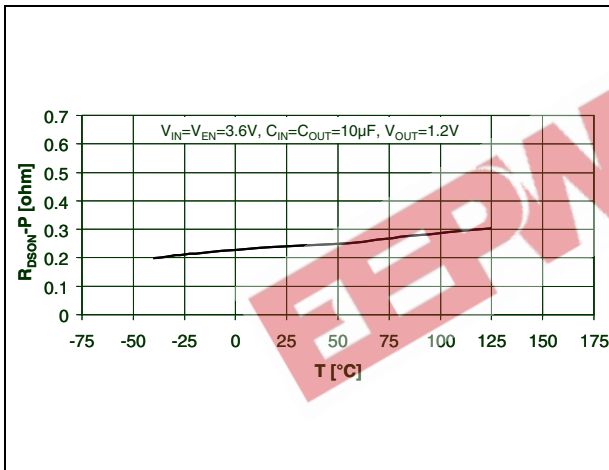


Figure 19. Switching current limitation vs temperature

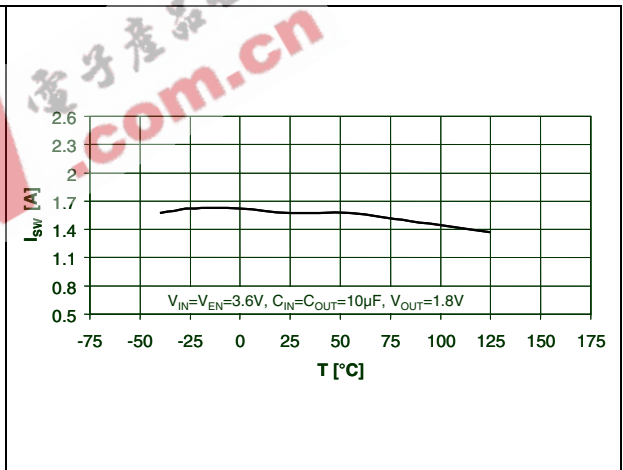


Figure 20. Switching current limitation vs input voltage

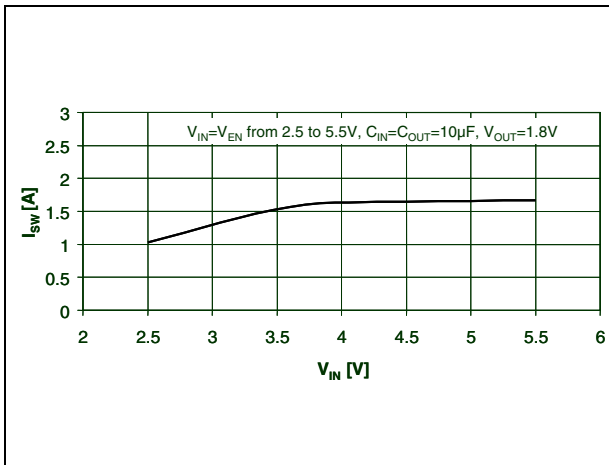


Figure 21. Output voltage vs input voltage

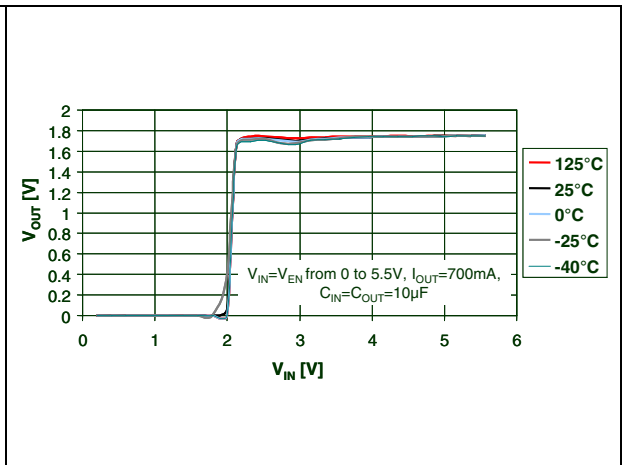


Figure 22. Line transient

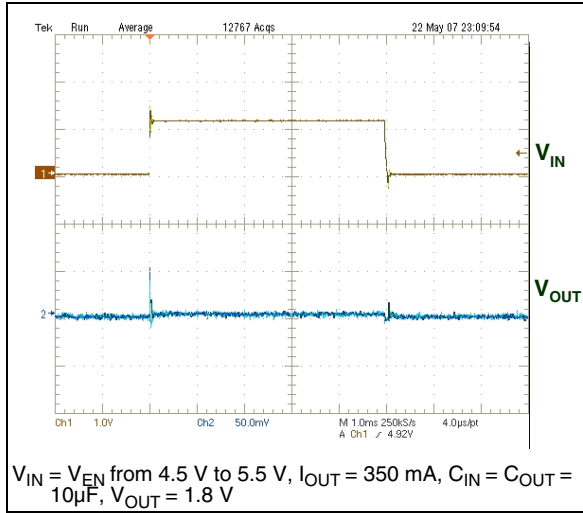


Figure 23. Load transient

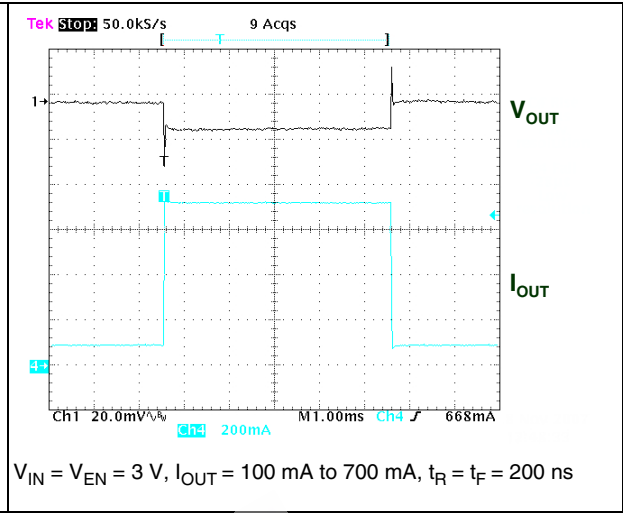


Figure 24. Start-up transient

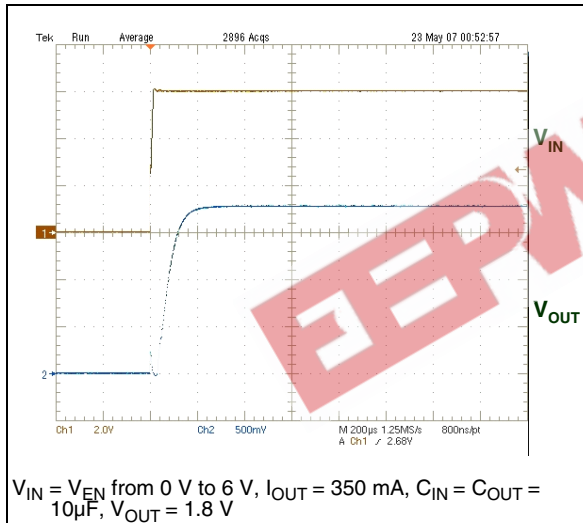
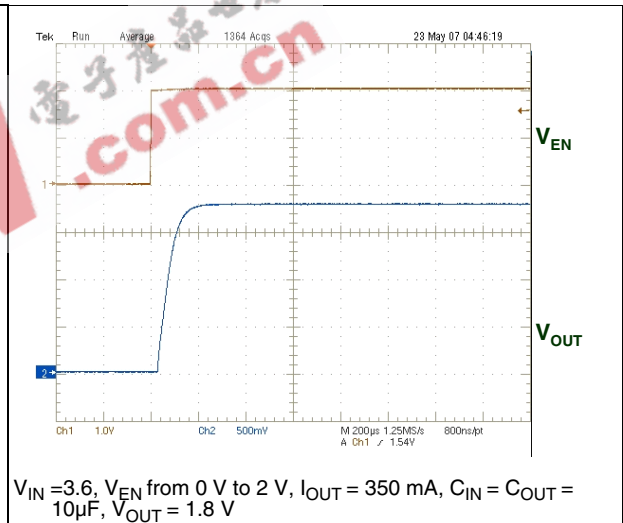


Figure 25. Enable transient



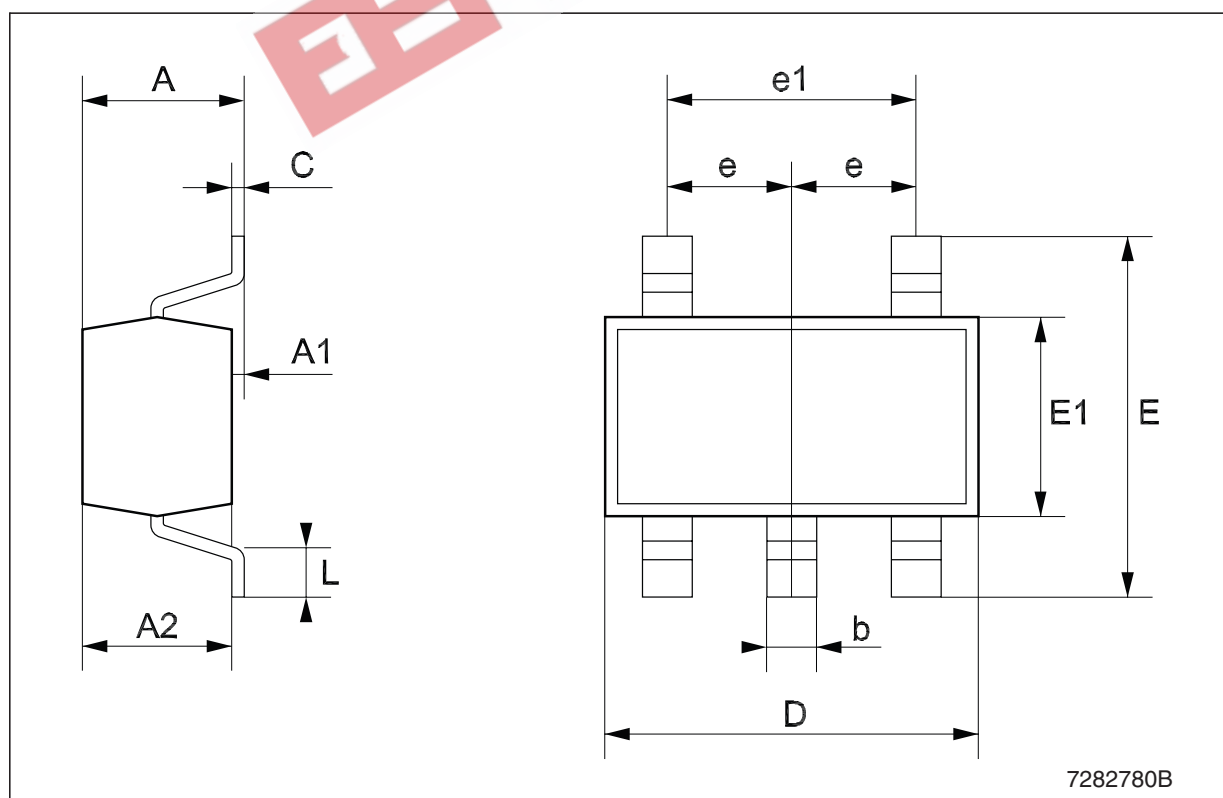
8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

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TSOT23-5L mechanical data

Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			43.3
A1	0		0.1			3.9
A2	0.7		1.0	27.6		39.4
b	0.3		0.5	11.8		19.7
C	0.08		0.2	3.1		7.9
D		2.9			114.2	
E		2.8			110.2	
E1		1.6			63.0	
e		0.95			37.4	
e1		1.9			74.8	
L	0.3		0.6	11.8		23.6



7282780B

Tape & reel TSOT23-5L mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.058
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161

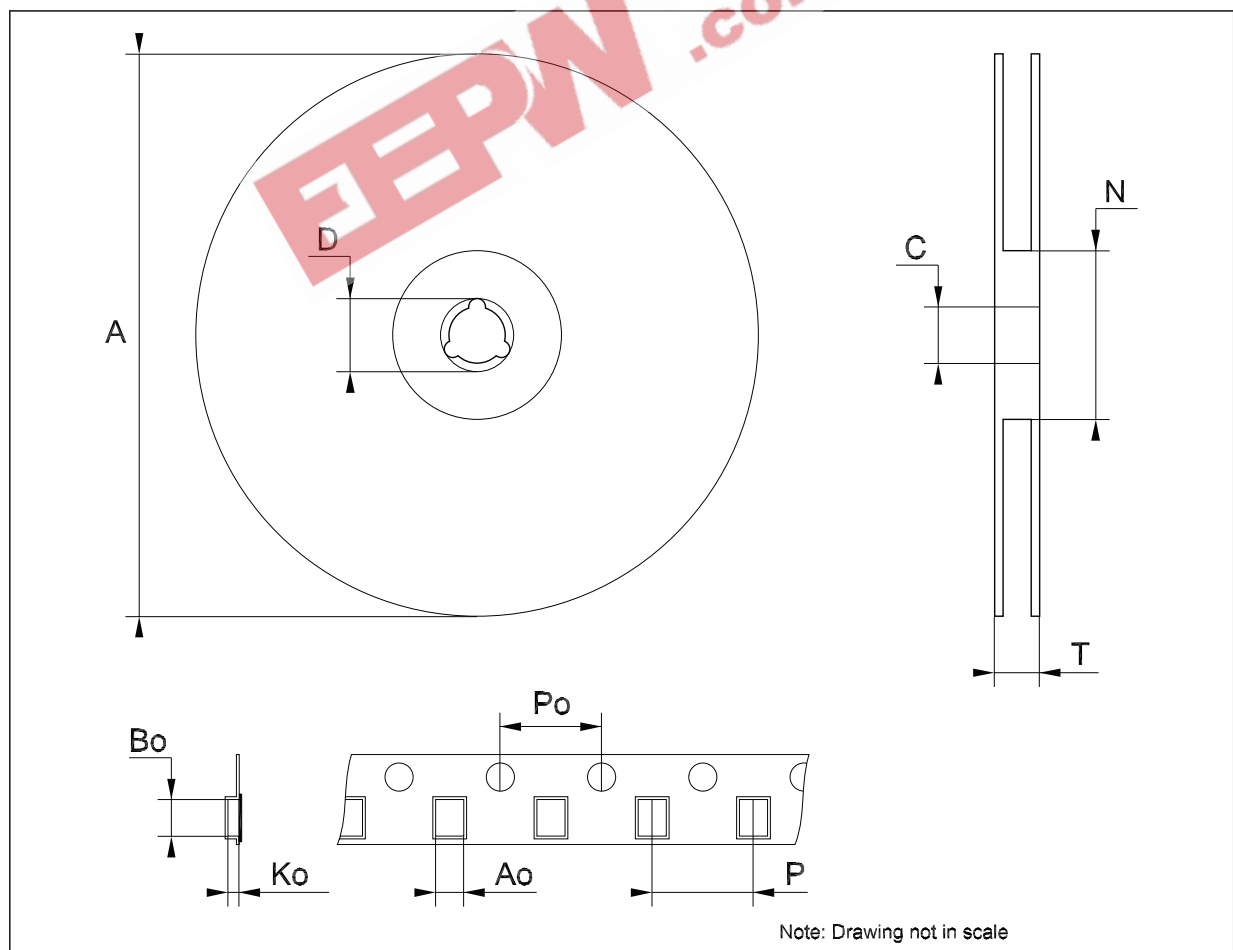


Figure 26. TSOT23-5L footprint recommended data

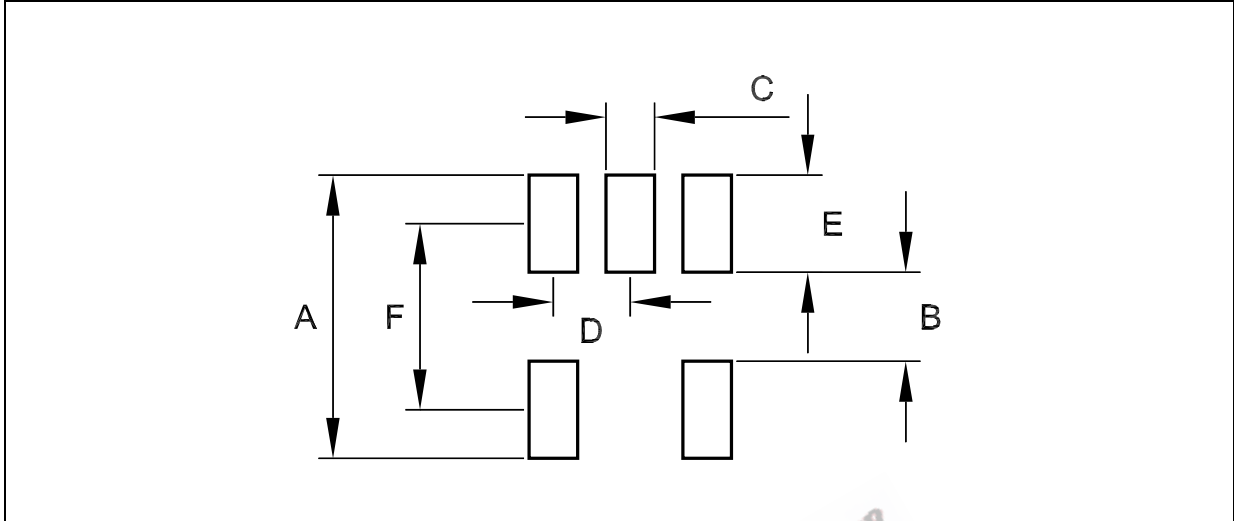


Table 9. Footprint data

	Values	
	mm.	inch.
A	3.50	0.138
B	1.10	0.043
C	0.60	0.024
D	0.95	0.037
E	1.20	0.047
F	2.30	0.090

9 Revision history

Table 10. Document revision history

Date	Revision	Changes
10-Jan-2008	1	Initial release.
01-Feb-2008	2	Modified: Figure 3 on page 9 .

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