



STD11NM60N - STD11NM60N-1 STP11NM60N - STF11NM60N

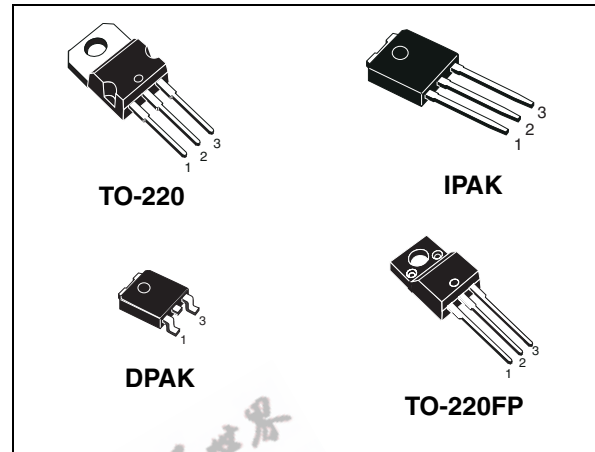
N-channel 600V - 0.37Ω - 10A - TO-220 - TO-220FP- IPAK - DPAK
Second generation MDmesh™ Power MOSFET

General features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)}	I _D
STD11NM60N	650V	<0.45Ω	10A
STD11NM60N-1	650V	<0.45Ω	10A
STF11NM60N	650V	<0.45Ω	10A ⁽¹⁾
STP11NM60N	650V	<0.45Ω	10A

1. Limited only by maximum temperature allowed

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



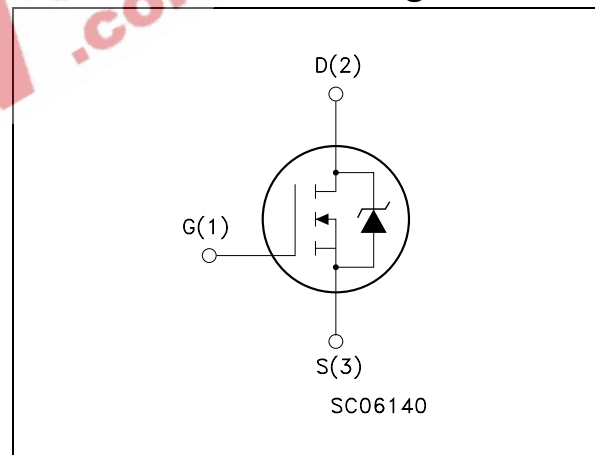
Description

This series of devices is realized with the second generation of MDmesh™ Technology. This revolutionary Power MOSFET associates a new vertical structure to the Company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STD11NM60N-1	D11NM60N	IPAK	Tube
STD11NM60N	D11NM60N	DPAK	Tape & reel
STP11NM60N	P11NM60N	TO-220	Tube
STF11NM60N	F11NM60N	TO-220FP	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/ DPAK/IPAK	TO-220FP	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	600		V
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	10	$10^{(1)}$	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	6.3	$6.3^{(1)}$	A
$I_{DM}^{(2)}$	Drain current (pulsed)	40	$40^{(1)}$	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	100	25	W
	Derating factor	0.8	0.2	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{s}; T_C=25^\circ\text{C}$)	--	2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150		$^\circ\text{C}$

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 10\text{A}$, $di/dt \leq 400\text{A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 2. Thermal data

		TO-220	DPAK/IPAK	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	1.25		5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb Max	62.5	100	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300			$^\circ\text{C}$

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	3.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$, $I_D=I_{AS}$, $V_{DD}=50\text{V}$)	200	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}$, $V_{GS} = 0$	600			V
$dv/dt^{(1)}$	Drain-source voltage slope	$V_{DD}=400\text{V}$, $I_D=5\text{A}$, $V_{GS}=10\text{V}$	45			V/ns
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS}=\text{Max rating}$, $V_{DS}=\text{Max rating}$, $T_c=125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 5\text{A}$		0.37	0.45	Ω

1. Characteristics value at turn off on inductive load

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$, $I_D = 5\text{A}$ $I_D = 10\text{A}$		7.5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		850 44 5		pF pF pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{V}$ to 480V		130		pF
R_g	Gate input resistance	$f = 1\text{MHz}$ Gate DC Bias = 0 Test signal level = 20mV open drain		3.7		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 480\text{V}$, $I_D = 5\text{A}$ $V_{GS} = 10\text{V}$ (see Figure 18)		31 4.2 15.9		nC nC nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=300V$, $I_D=5A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 17)		22		ns
t_r	Rise time			18.5		ns
$t_{d(off)}$	Turn-off delay time			50		ns
t_f	Fall time			12		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{SD}	Source-drain current				10	A
I_{SDM}	Source-drain current (pulsed)				40	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 10A$, $V_{GS}=0$			1.3	V
t_{rr}	Reverse recovery time	$I_{SD}=10A$, $di/dt = 100A/\mu s$, $V_{DD}=100V$, $T_j=25^\circ C$ (see Figure 22)		340		ns
Q_{rr}	Reverse recovery charge			3.26		μC
I_{RRM}	Reverse recovery current			19.2		A
t_{rr}	Reverse recovery time	$V_{DD}=100V$ $di/dt = 100A/\mu s$, $I_{SD}=10A$ $T_j=150^\circ C$ (see Figure 22)		460		ns
Q_{rr}	Reverse recovery charge			4.42		μC
I_{RRM}	Reverse recovery current			19.2		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

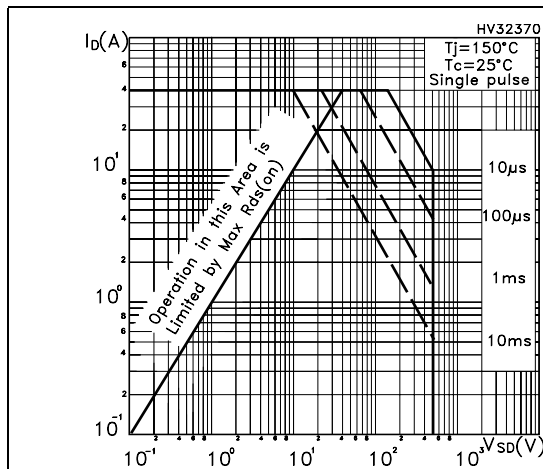


Figure 2. Thermal impedance for TO-220

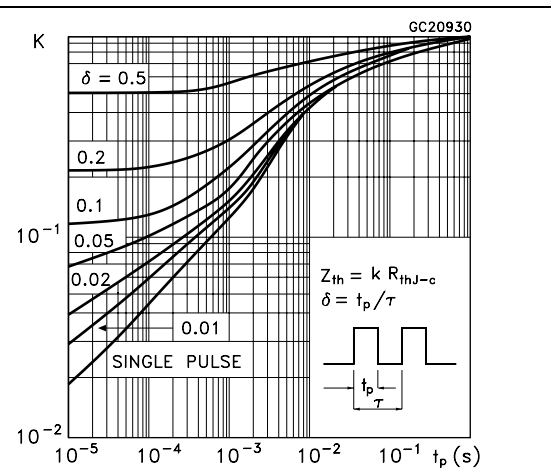


Figure 3. Safe operating area for TO-220FP

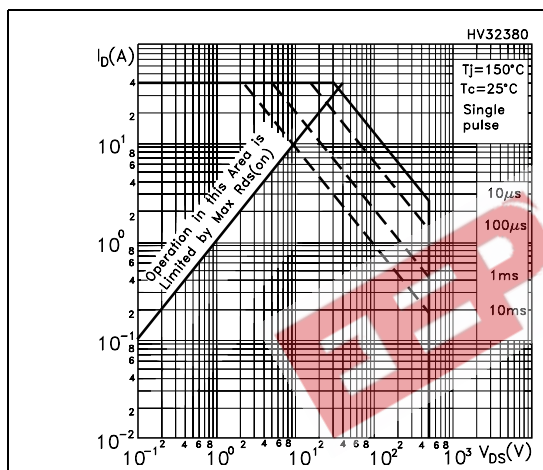


Figure 4. Thermal impedance for TO-220FP

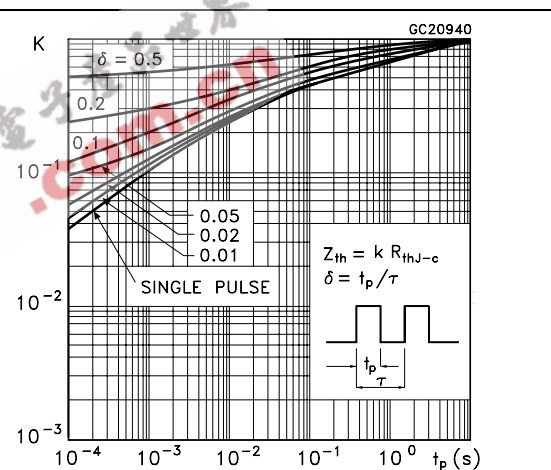


Figure 5. Safe operating area for DPAK / IPAK

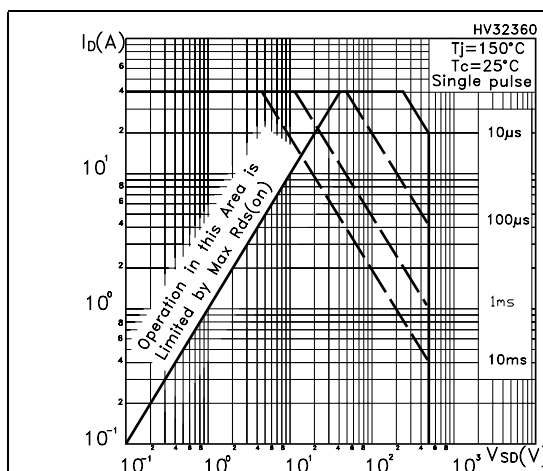


Figure 6. Thermal impedance for DPAK / IPAK

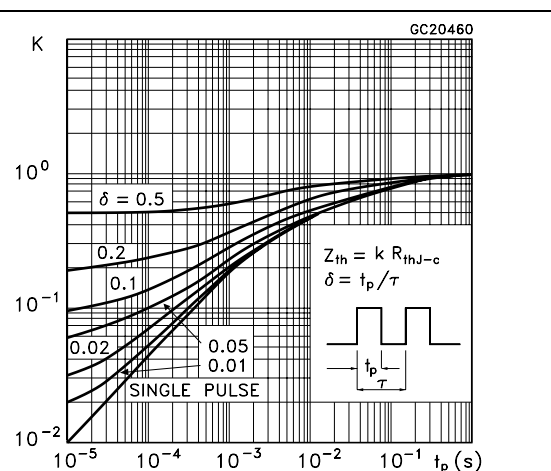


Figure 7. Output characteristics

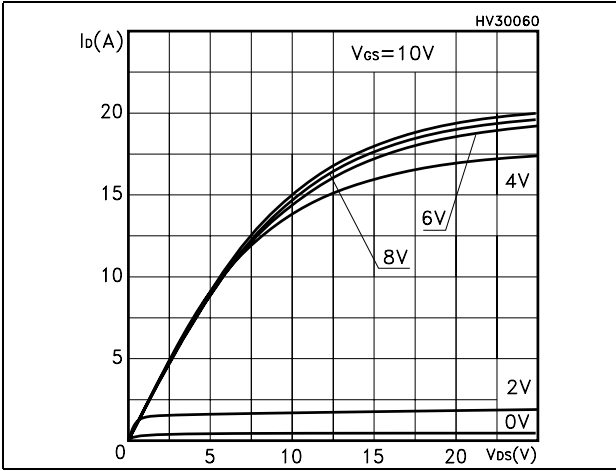


Figure 8. Transfer characteristics

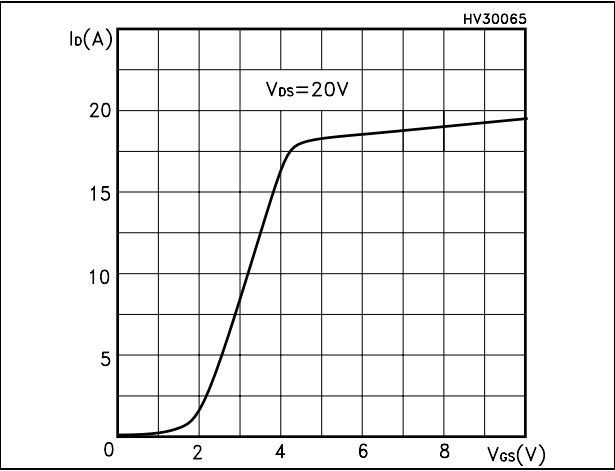


Figure 9. Transconductance

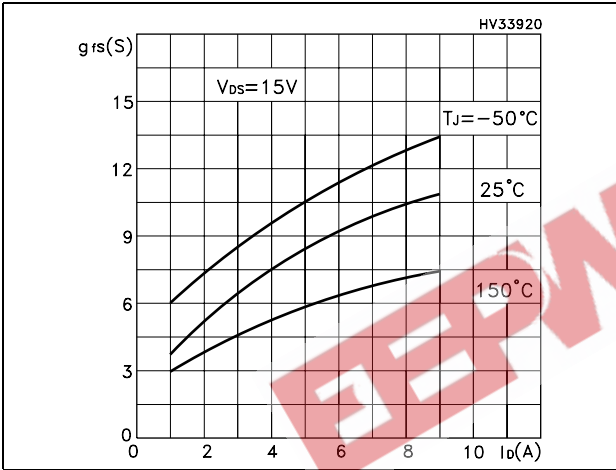


Figure 10. Static drain-source on resistance

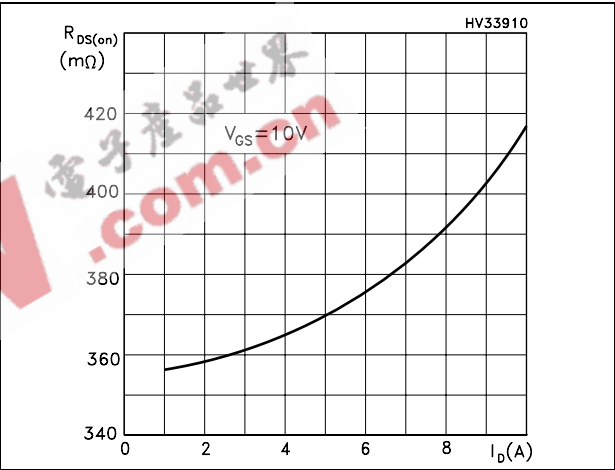


Figure 11. Gate charge vs gate-source voltage

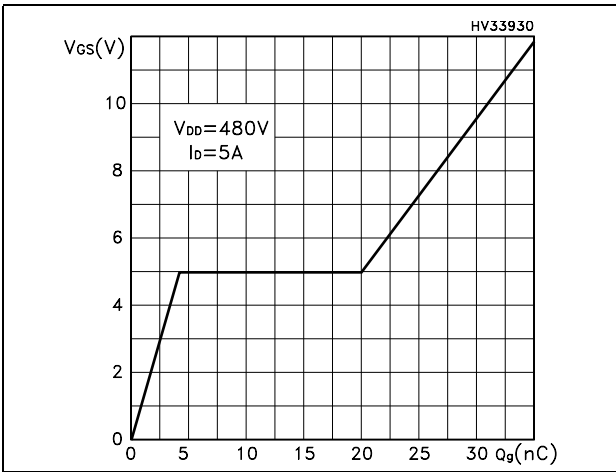


Figure 12. Capacitance variations

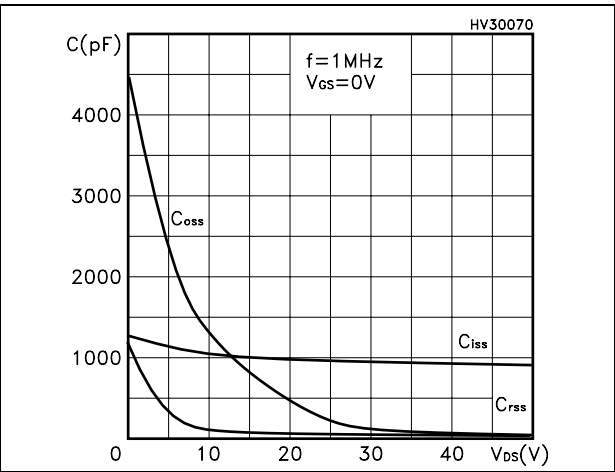


Figure 13. Normalized gate threshold voltage vs temperature

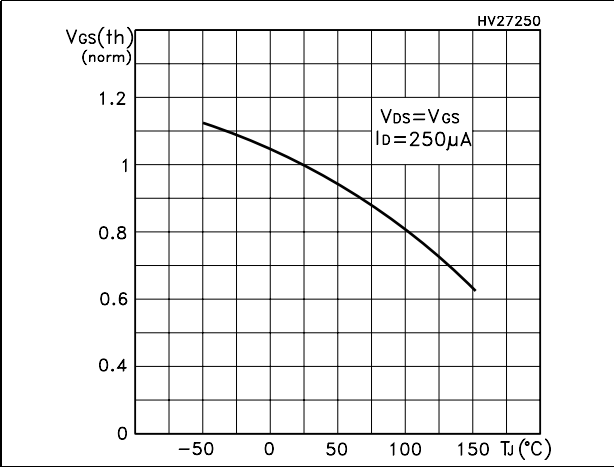


Figure 14. Normalized on resistance vs temperature

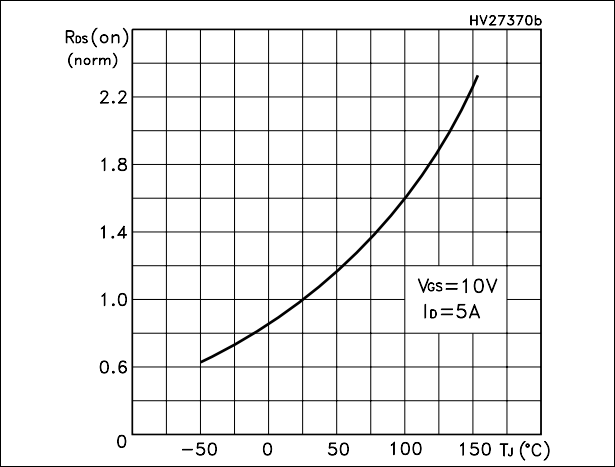


Figure 15. Source-drain diode forward characteristics

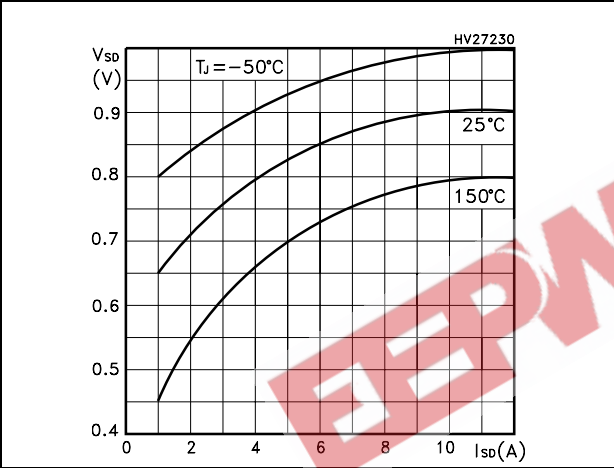
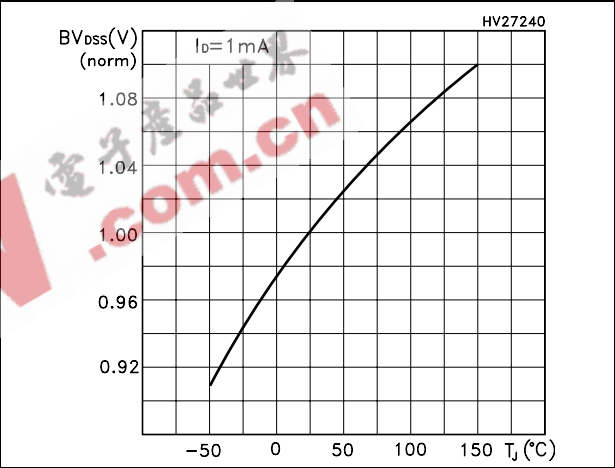


Figure 16. Normalized $B_{V_{DS}}$ vs temperature



3 Test circuit

Figure 17. Switching times test circuit for resistive load

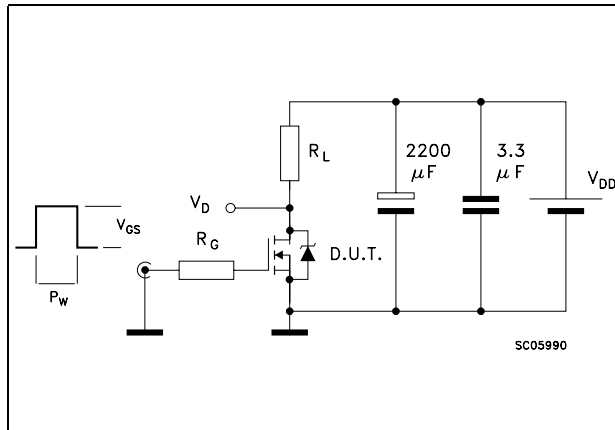


Figure 18. Gate charge test circuit

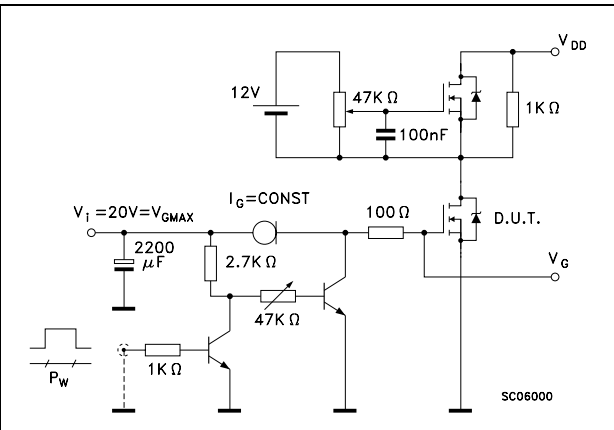


Figure 19. Test circuit for inductive load switching and diode recovery times

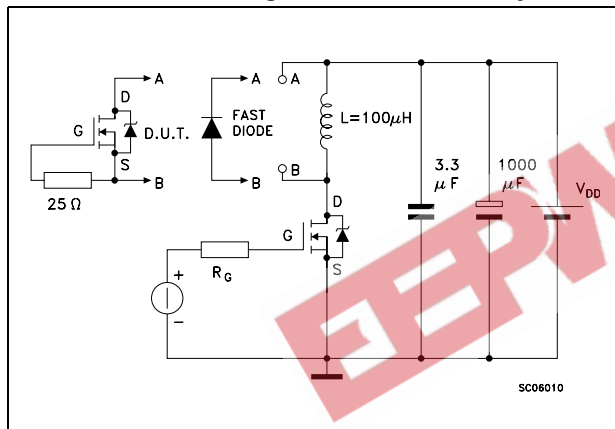


Figure 20. Unclamped Inductive load test circuit

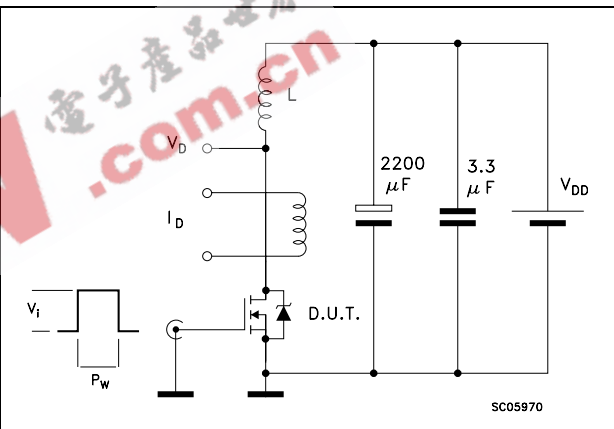


Figure 21. Unclamped inductive waveform

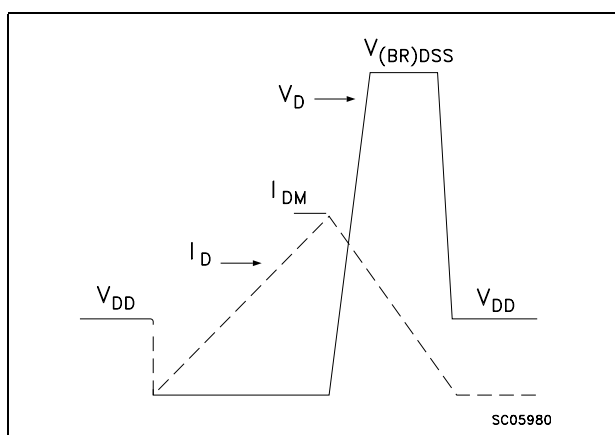
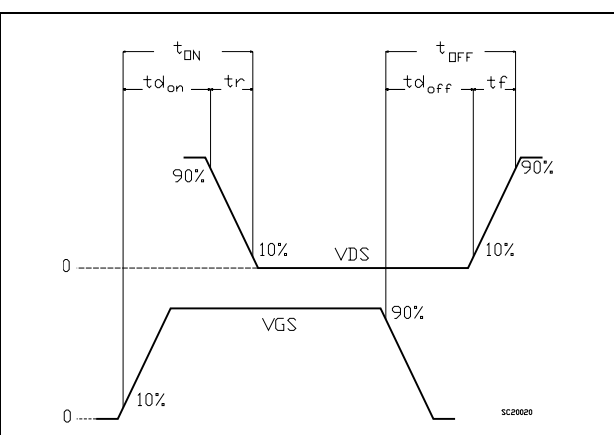


Figure 22. Switching time waveform



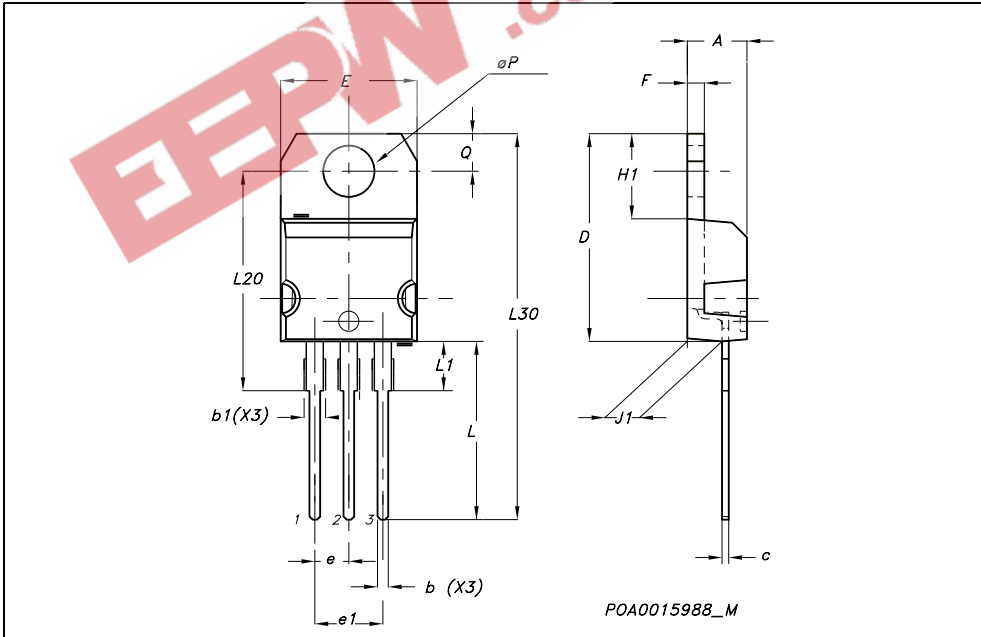
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

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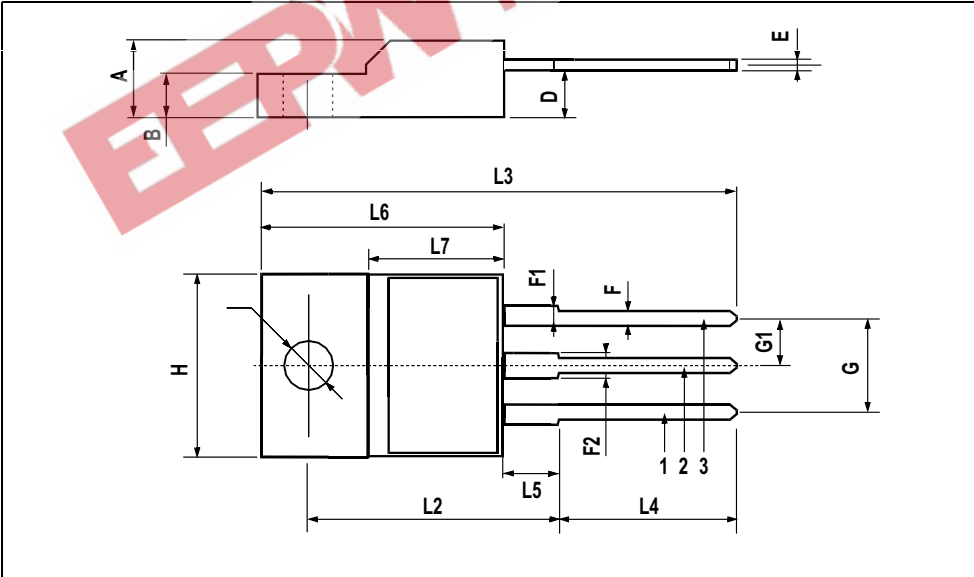
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



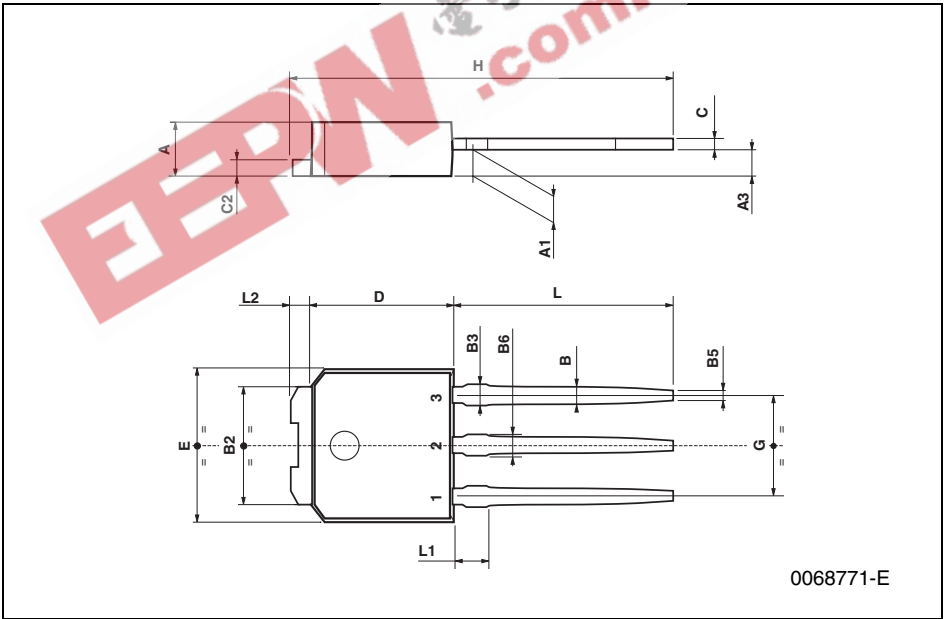
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-251 (IPAK) MECHANICAL DATA

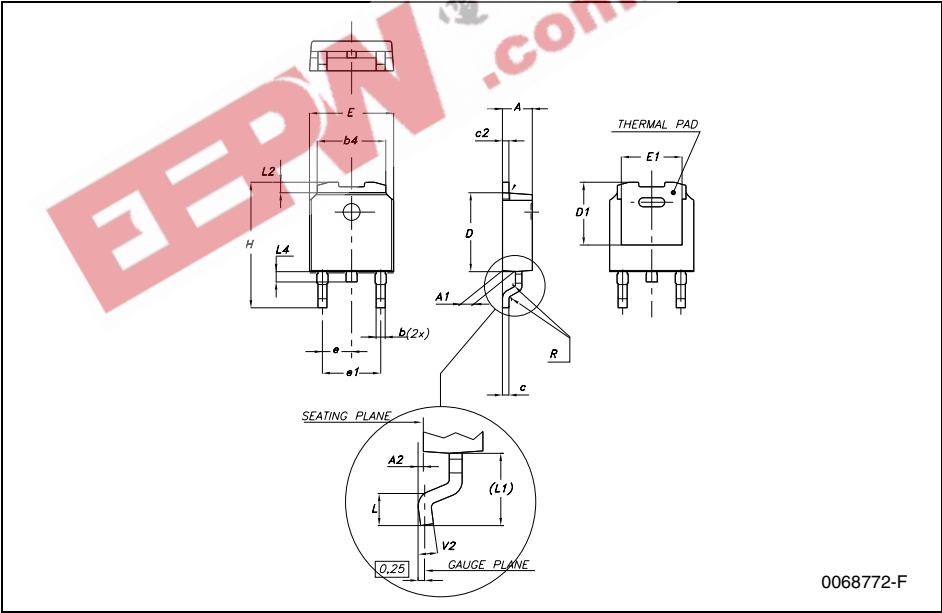
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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DPAK MECHANICAL DATA

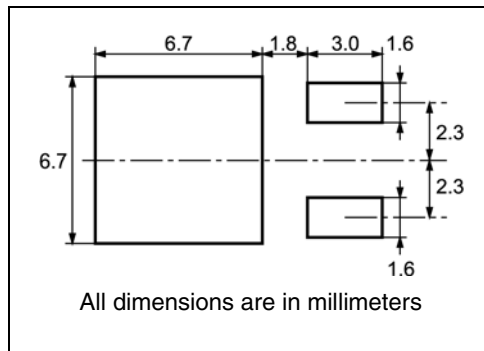
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



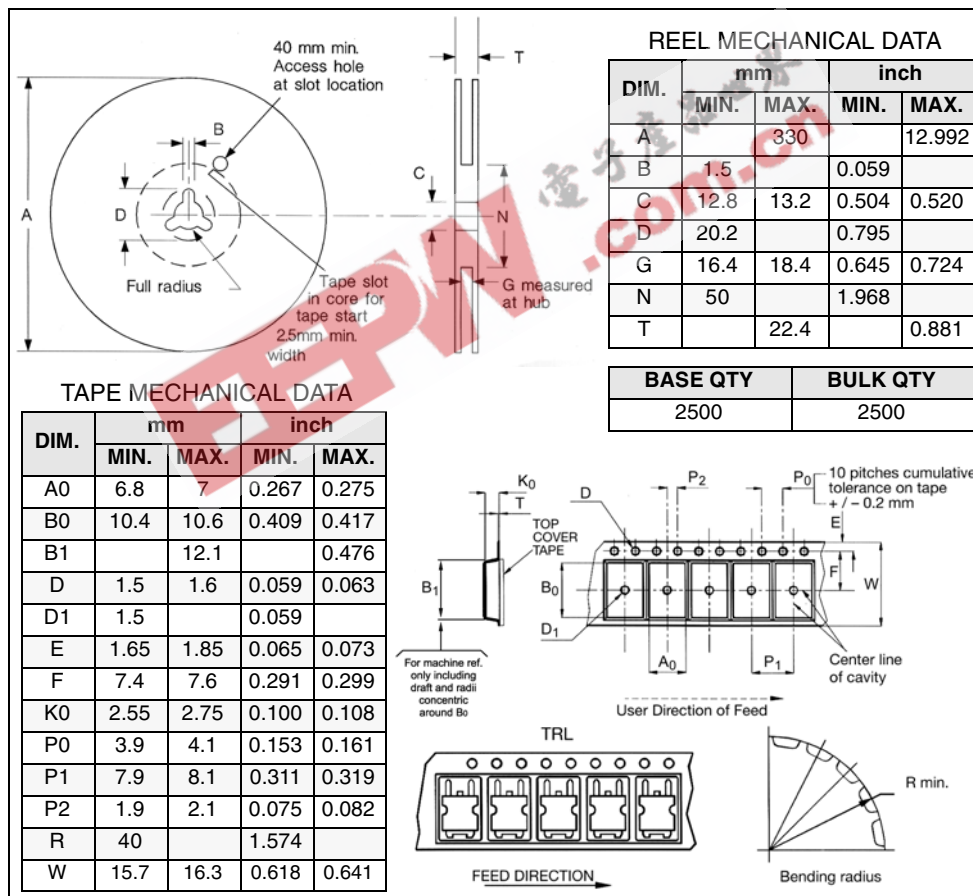
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5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 8. Revision history

Date	Revision	Changes
03-Aug-2006	1	First release
14-Nov-2006	2	Complete version

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