



## STD95NH02L

N-channel 24V - 0.005239Ω - 80A - DPAK  
Ultra low gate charge STripFET™ Power MOSFET

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD95NH02L	24V	<0.005Ω	80A <sup>(1)</sup>

1. Value limited by wire bonding

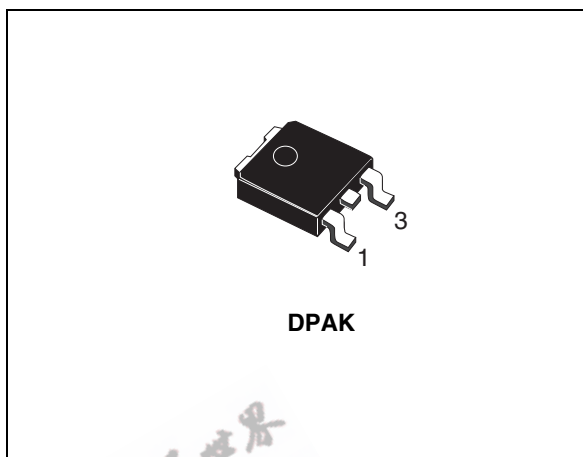
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

### Description

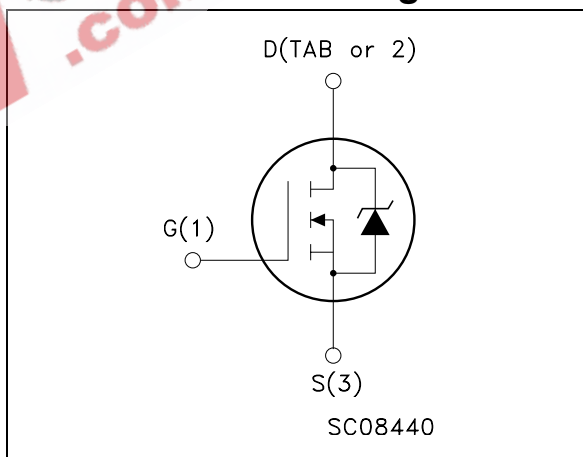
The device is based on the latest generation of ST's proprietary STripFET™ technology. An innovative layout enables the device to also exhibit extremely low gate charge for the most demanding requirements in high-frequency DC-DC converters. It's therefore ideal for high-density converters in Telecom and Computer applications.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STD95NH02LT4	D95NH02L	DPAK	Tape & reel

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{\text{spike}}^{(1)}$	Drain-source voltage rating	30	V
$V_{\text{DS}}$	Drain-source voltage ( $V_{\text{GS}} = 0$ )	24	V
$V_{\text{DGR}}$	Drain-gate voltage ( $R_{\text{GS}} = 20\text{k}\Omega$ )	24	V
$V_{\text{GS}}$	Gate-source voltage	$\pm 20$	V
$I_{\text{D}}^{(2)}$	Drain current (continuous) at $T_{\text{C}} = 25^{\circ}\text{C}$	80	A
$I_{\text{D}}^{(2)}$	Drain current (continuous) at $T_{\text{C}} = 100^{\circ}\text{C}$	68	A
$I_{\text{DM}}^{(3)}$	Drain current (pulsed)	320	A
$P_{\text{TOT}}$	Total dissipation at $T_{\text{C}} = 25^{\circ}\text{C}$	100	W
	Derating factor	0.67	W/ $^{\circ}\text{C}$
$E_{\text{AS}}^{(4)}$	Single pulse avalanche energy	600	mJ
$T_{\text{j}}$	Operating junction temperature	-55 to 175	$^{\circ}\text{C}$
$T_{\text{stg}}$	Storage temperature		

1. Guaranteed when external  $R_{\text{g}} = 4.7\Omega$  and  $T_{\text{f}} < T_{\text{fmax}}$

2. Value limited by wire bonding

3. Pulse width limited by safe operating area

4. Starting  $T_{\text{j}} = 25^{\circ}\text{C}$ ,  $I_{\text{d}} = 40\text{A}$ ,  $V_{\text{dd}} = 22\text{V}$

**Table 2. Thermal data**

$R_{\text{thj-case}}$	Thermal resistance junction-case max	1.5	$^{\circ}\text{C}/\text{W}$
$R_{\text{thj-amb}}$	Thermal resistance junction-to ambient max	100	$^{\circ}\text{C}/\text{W}$
$T_{\text{j}}$	Maximum lead temperature for soldering purpose	275	$^{\circ}\text{C}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	24			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 20V$ $V_{DS} = 20V, T_C = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 40A$ $V_{GS} = 5V, I_D = 40A$		0.0039 0.0055	0.005 0.009	$\Omega$ $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10V, I_D = 10A$		30		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 15V, f = 1MHz,$ $V_{GS} = 0$		2070 990 90		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 12V, I_D = 40A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see <a href="#">Figure 13</a> )		20 110 47 20		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 12V, I_D = 80A,$ $V_{GS} = 5V, R_G = 4.7\Omega$ (see <a href="#">Figure 14</a> )		17 7.6 6.8		nC nC nC
$Q_{oss}^{(2)}$	Output charge	$V_{DS} = 19V, V_{GS} = 0V$		22.6		nC
$Q_{gls}^{(3)}$	Third-quadrant gate charge	$V_{DS} < 0V, V_{GS} = 5V$		15		nC
$R_G$	Gate Input Resistance	f=1MHz Gate DC Bias =0 Test Signal Level =20mV Open Drain		1.8		$\Omega$

1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

2.  $Q_{oss} = C_{oss} * \Delta V_{in}$ ,  $C_{oss} = C_{gd} + C_{gd}$ . See [Chapter 4: Appendix A](#)

3. Gate charge for synchronous operation

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				80 320	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 40A, V_{GS} = 0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 80A, di/dt = 100A/\mu s,$ $V_{DD} = 20V, T_j = 150^\circ C$ (see <a href="#">Figure 15</a> )		42 50.4 2.4		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %

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## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

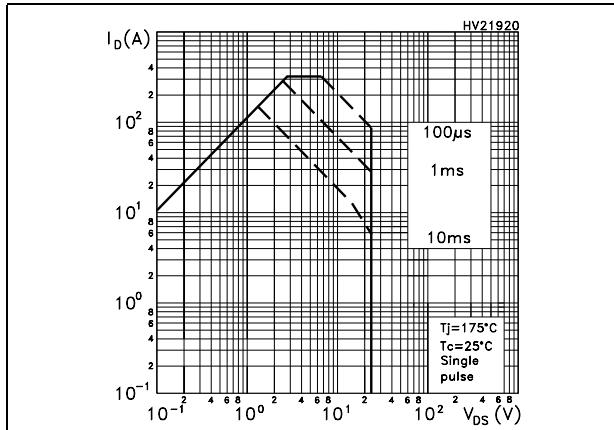


Figure 2. Thermal impedance

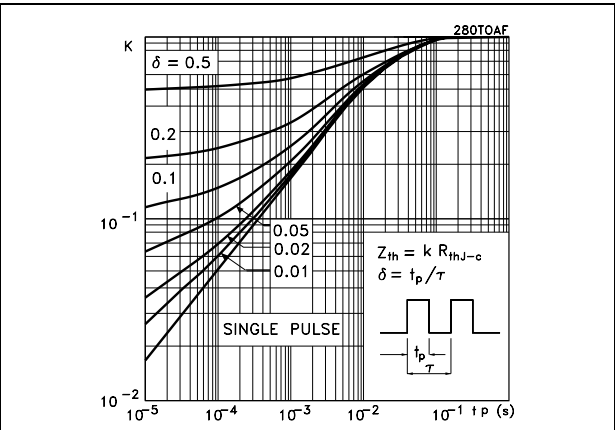


Figure 3. Output characteristics

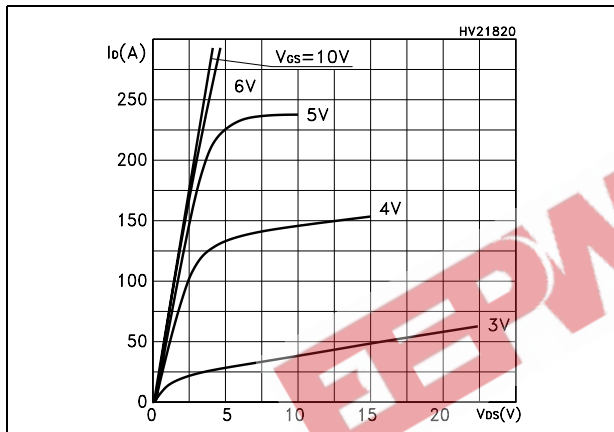


Figure 4. Transfer characteristics

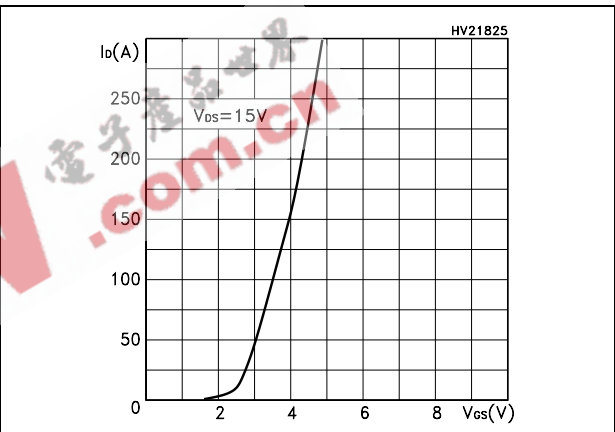


Figure 5. Transconductance

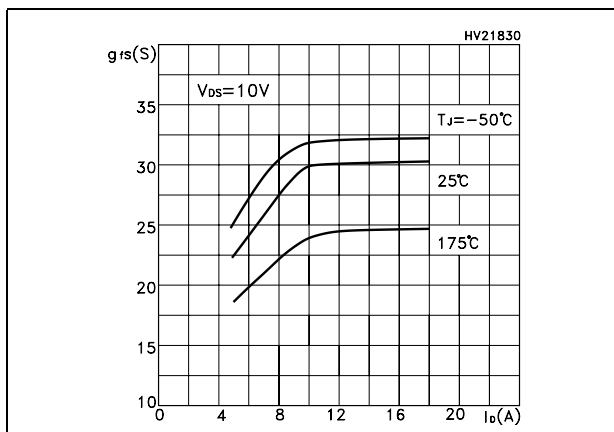


Figure 6. Static drain-source on resistance

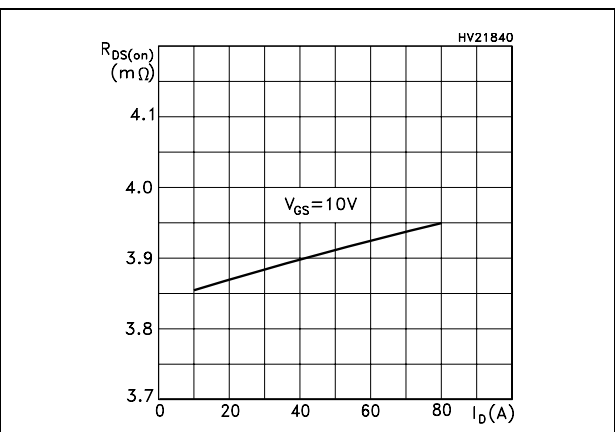


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

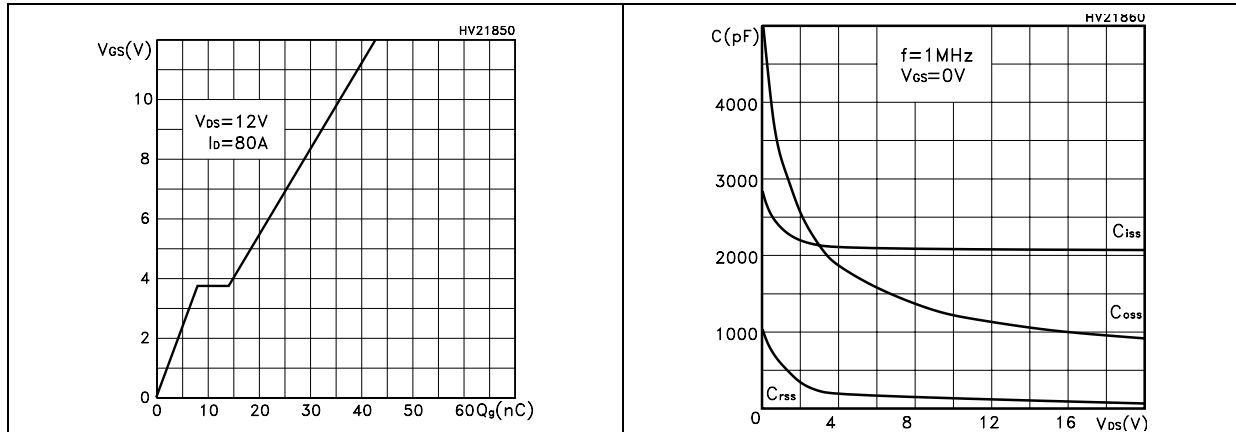


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

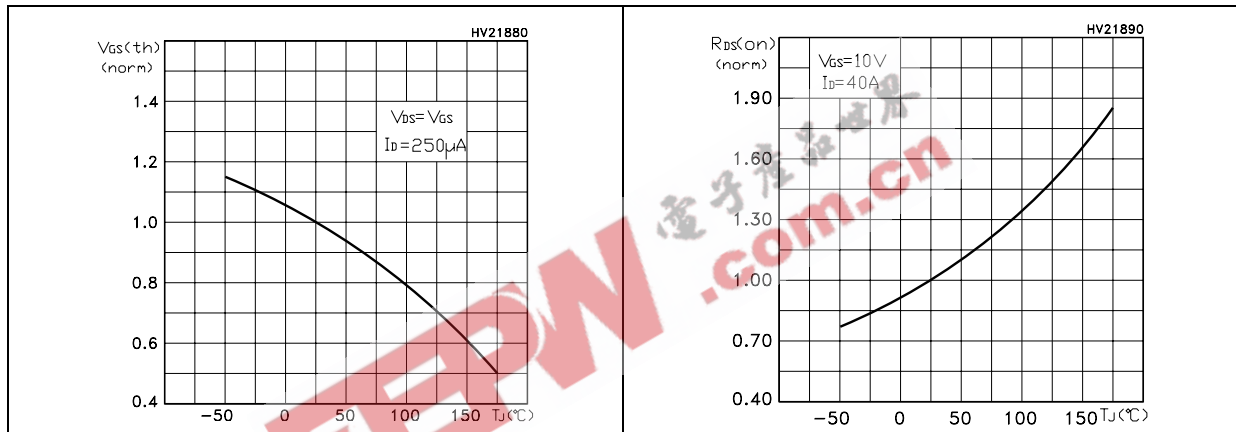
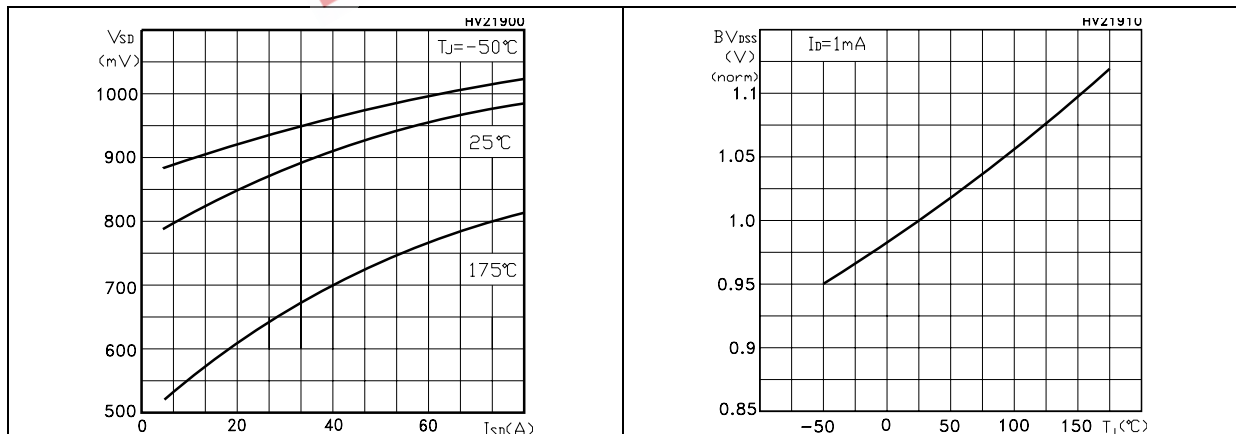


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized  $BV_{DSS}$  vs temperature



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load



Figure 14. Gate charge test circuit

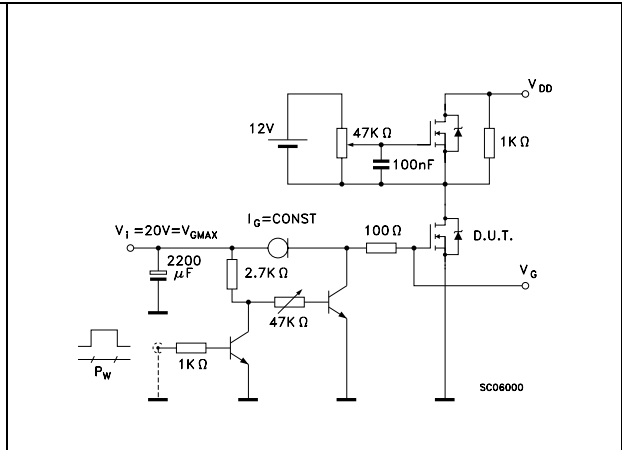


Figure 15. Test circuit for inductive load switching and diode recovery times

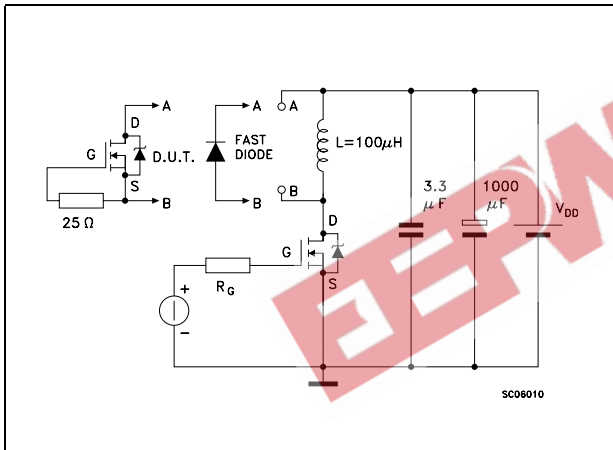


Figure 16. Unclamped Inductive load test circuit

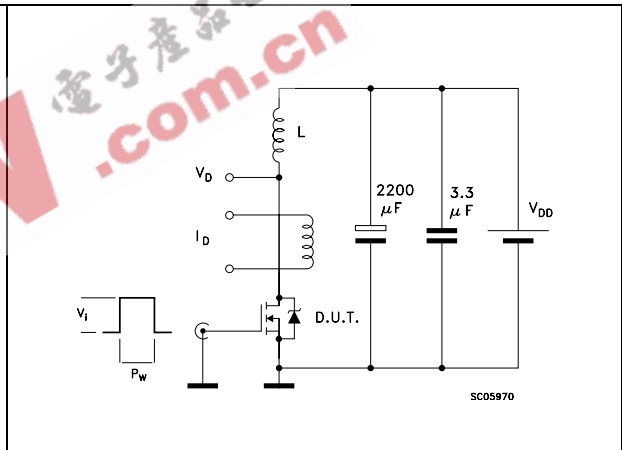
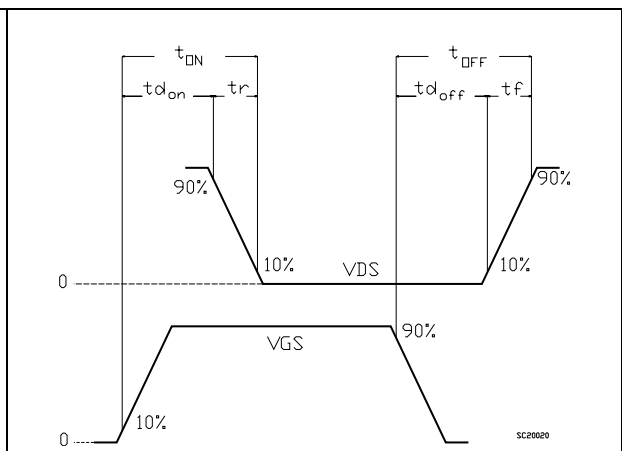


Figure 17. Unclamped inductive waveform



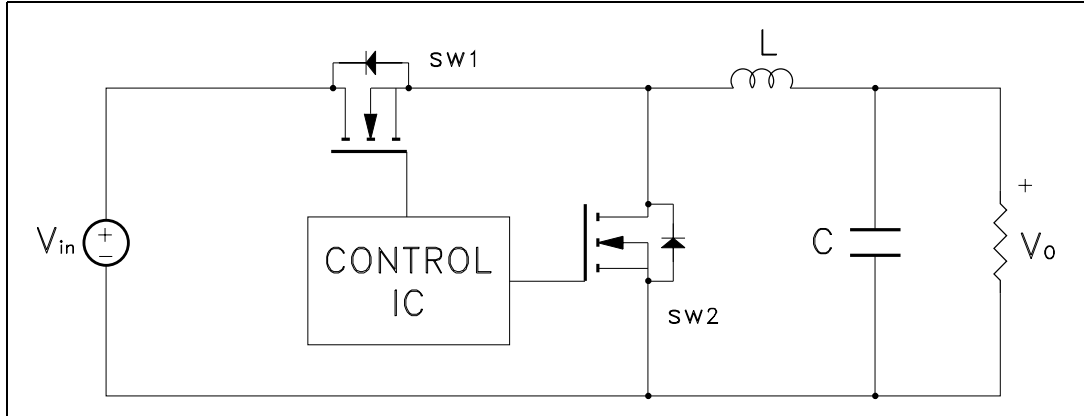
Figure 18. Switching time waveform





# 4 Appendix A

**Figure 19. Buck converter: power losses estimation**



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

- The low side (SW2) device requires:
- Very low  $R_{DS(on)}$  to reduce conduction losses
- Small  $Q_{gl}$  to reduce the gate charge losses
- Small  $C_{oss}$  to reduce losses due to output capacitance
- Small  $Q_{rr}$  to reduce losses on SW1 during its turn-on
- The  $C_{gd}/C_{gs}$  ratio lower than  $V_{th}/V_{gg}$  ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;
- The high side (SW1) device requires:
- Small  $R_g$  and  $L_s$  to allow higher gate current peak and to limit the voltage feedback on the gate
- Small  $Q_g$  to have a faster commutation and to reduce gate charge losses
- Low  $R_{DS(on)}$  to reduce the conduction losses.

**Table 6. Power losses calculation**

	High side switching (SW1)	Low side switch (SW2)
Pconduction	$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1 - \delta)$
Pswitching	$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching

**Table 6. Power losses calculation**

		High side switching (SW1)	Low side switch (SW2)
P <sub>diode</sub>	Recovery <sup>(1)</sup>	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
P <sub>gate</sub> (Q <sub>G</sub> )		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P <sub>Qoss</sub>		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

1. Dissipated by SW1 during turn-on

**Table 7. Parameters meaning**

Parameter	Meaning
d	Duty-cycle
Q <sub>gsth</sub>	Post threshold gate charge
Q <sub>gls</sub>	Third quadrant gate charge
P <sub>conduction</sub>	On state losses
P <sub>switching</sub>	On-off transition losses
P <sub>diode</sub>	Conduction and reverse recovery diode losses
P <sub>gate</sub>	Gate drive losses
P <sub>Qoss</sub>	Output capacitance losses

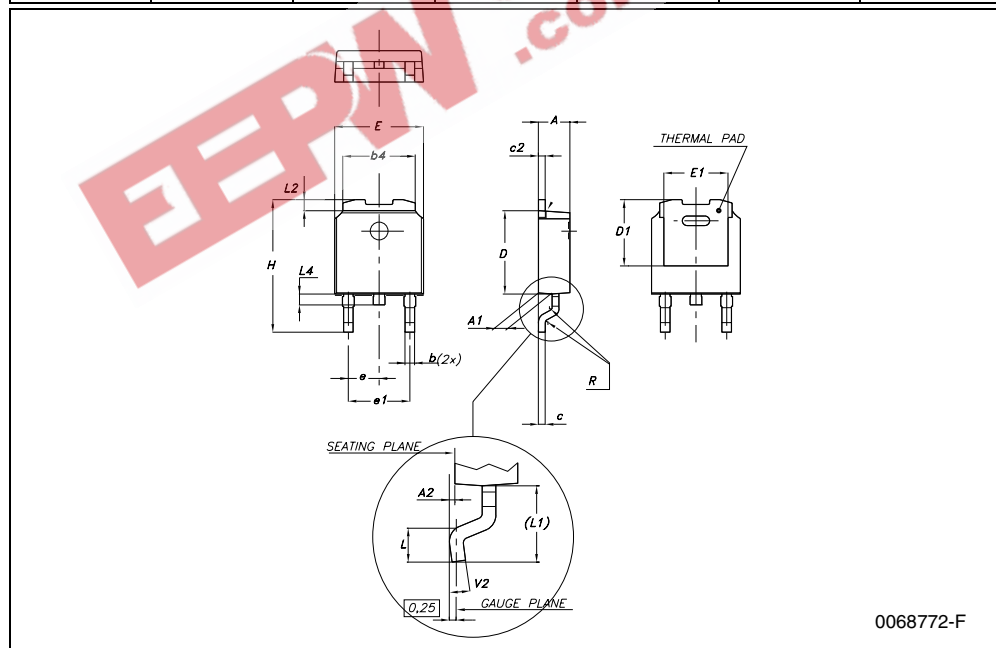
## 5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

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**DPAK MECHANICAL DATA**

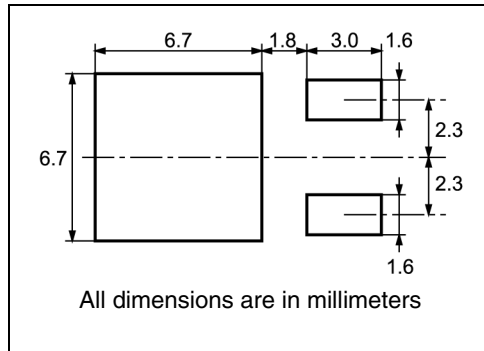
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



0068772-F

## 6 Packing mechanical data

### DPAK FOOTPRINT



### TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start  
2.5mm min. width

40 mm min. Access hole at slot location

T

#### REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

#### TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

#### BASE QTY

2500
------

#### BULK QTY

2500
------

TOP COVER TAPE

User Direction of Feed

FEED DIRECTION

Bending radius R min.

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

For machine ref. only including draft and radii concentric around B0

## 7 Revision history

**Table 8. Revision history**

Date	Revision	Changes
13-Sep-2004	1	First release
27-May-2005	2	Some values changed in <a href="#">Table 4: Dynamic</a> .
09-Aug-2006	3	New template, no content change

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