

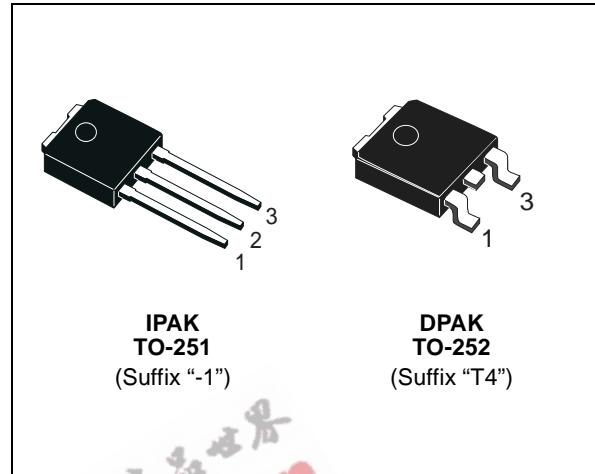


# STD55NH2LL

## N-CHANNEL 24V - 0.010 $\Omega$ - 40A DPAK/IPAK ULTRA LOW GATE CHARGE STripFET™ POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD55NH2LL	24 V	< 0.011 $\Omega$	40 A(*)

- TYPICAL R<sub>DS(on)</sub> = 0.01  $\Omega$  @ 10 V
- TYPICAL R<sub>DS(on)</sub> = 0.012  $\Omega$  @ 4.5 V
- R<sub>DS(ON)</sub> \* Q<sub>g</sub> INDUSTRY'S BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- THROUGH-HOLE IPAK (TO-251) POWER PACKAGE IN TUBE (SUFFIX "-1")
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")



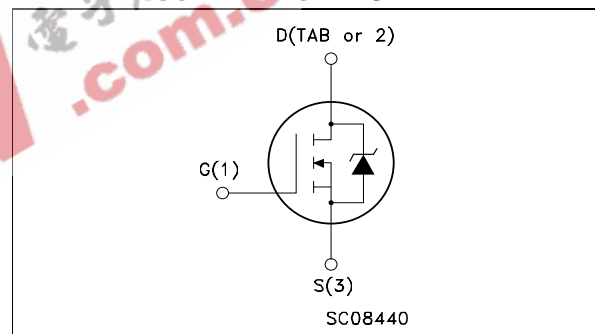
### DESCRIPTION

The STD55NH2LL is based on the latest generation of ST's proprietary STripFET™ technology. An innovative layout enables the device to also exhibit extremely low gate charge for the most demanding requirements as high-side switch in high-frequency DC-DC converters. It's therefore ideal for high-density converters in Telecom and Computer applications.

### APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS

### INTERNAL SCHEMATIC DIAGRAM



### Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD55NH2LLT4	D55NH2LL	TO-252	TAPE & REEL
STD55NH2LL-1	D55NH2LL	TO-251	TUBE

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>spike</sub> (1)	Drain-source Voltage Rating	30	V
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	24	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	24	V
V <sub>GS</sub>	Gate- source Voltage	$\pm 18$	V
I <sub>D</sub> (*)	Drain Current (continuous) at T <sub>C</sub> = 25°C	40	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	28	A
I <sub>DM</sub> (2)	Drain Current (pulsed)	160	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	60	W
	Derating Factor	0.4	W/°C
E <sub>AS</sub> (3)	Single Pulse Avalanche Energy	600	mJ
T <sub>stg</sub>	Storage Temperature	-55 to 175	°C
T <sub>j</sub>	Operating Junction Temperature		

# STD55NH2LL

## THERMAL DATA

R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max	2.5	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient	Max	100	°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose		275	°C

## ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	24			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>C</sub> = 125°C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 18V			±100	nA

ON (4)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	1			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 20 A V <sub>GS</sub> = 4.5 V I <sub>D</sub> = 20 A		0.010 0.012	0.011 0.0135	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (4)	Forward Transconductance	V <sub>DS</sub> = 10 V I <sub>D</sub> = 10 A		18		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 10V f = 1 MHz V <sub>GS</sub> = 0		990		pF
C <sub>oss</sub>	Output Capacitance			385		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			40		pF
R <sub>G</sub>	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		1.3		Ω

# STD55NH2LL

## ELECTRICAL CHARACTERISTICS (continued)

### SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 10\text{ V}$ $I_D = 20\text{ A}$		15		ns
$t_r$	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 3)		56		ns
$Q_g$	Total Gate Charge	$0.44\text{ V} \leq V_{DD} \leq 10\text{ V}$ , $I_D = 40\text{ A}$		8.7	11	nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 4.5\text{ V}$		4.2		nC
$Q_{gd}$	Gate-Drain Charge			2.4		nC
$Q_{oss}^{(5)}$	Output Charge	$V_{DS} = 16\text{ V}$ $V_{GS} = 0\text{ V}$		7.6		nC

### SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 10\text{ V}$ $I_D = 20\text{ A}$		13		ns
$t_f$	Fall Time	$R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		10		ns

### SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				40	A
$I_{SDM}$	Source-drain Current (pulsed)				160	A
$V_{SD}^{(4)}$	Forward On Voltage	$I_{SD} = 20\text{ A}$ $V_{GS} = 0$			1.3	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 40\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$		32.5		ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 15\text{ V}$ $T_j = 150^\circ\text{C}$		28		nC
$I_{RRM}$	Reverse Recovery Current	(see test circuit, Figure 5)		1.7		A

(1) Guaranteed when external  $R_G = 4.7\ \Omega$  and  $t_r < t_{rmax}$ .

(2) Pulse width limited by safe operating area

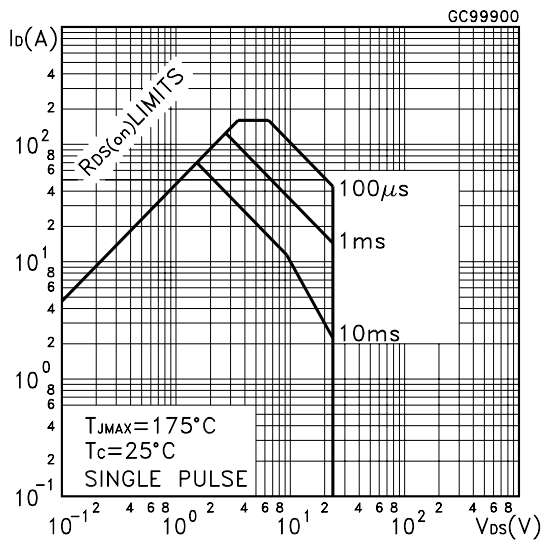
(3) Starting  $T_j = 25^\circ\text{C}$ ,  $I_D = 20\text{ A}$ ,  $V_{DD} = 15\text{ V}$

(4) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

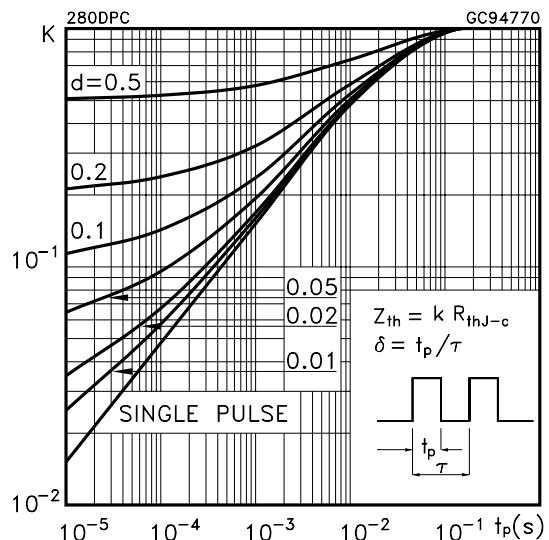
(5)  $Q_{oss} = C_{oss} \cdot \Delta V_{in}$ ,  $C_{oss} = C_{gd} + C_{ds}$ . See Appendix A

(\*) Value limited by wire bonding

### Safe Operating Area

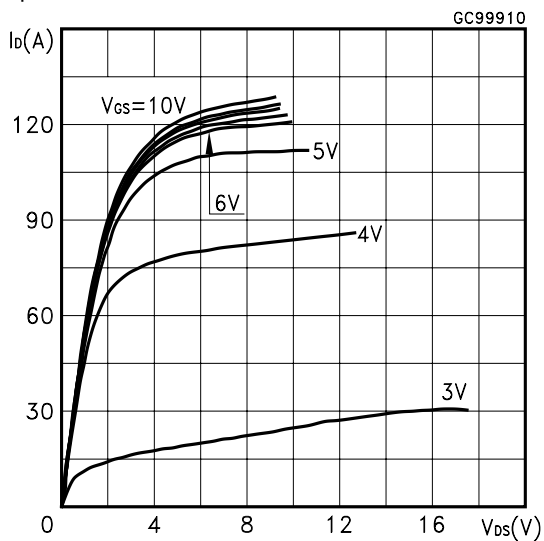


### Thermal Impedance

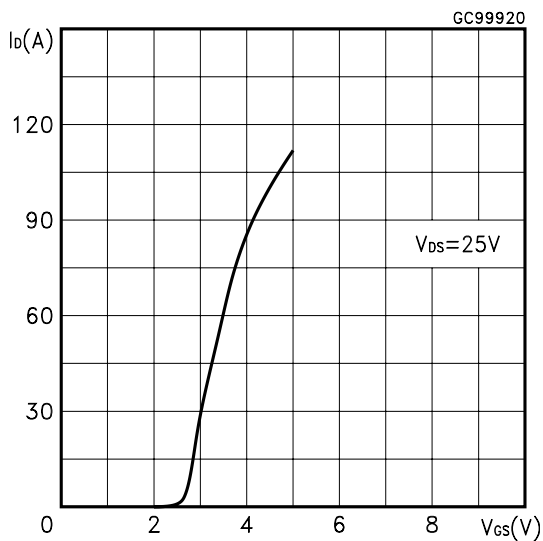


# STD55NH2LL

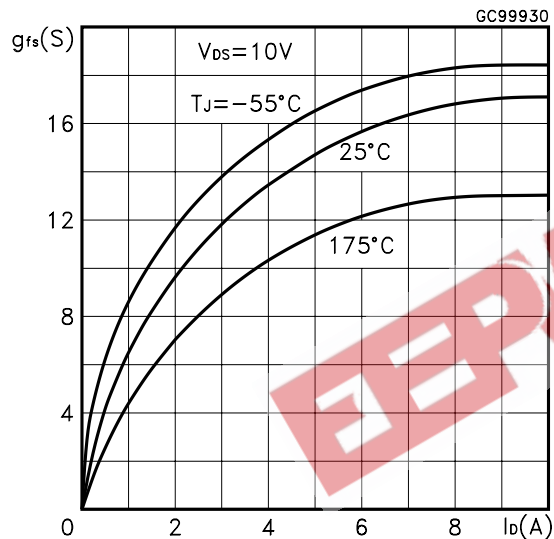
Output Characteristics



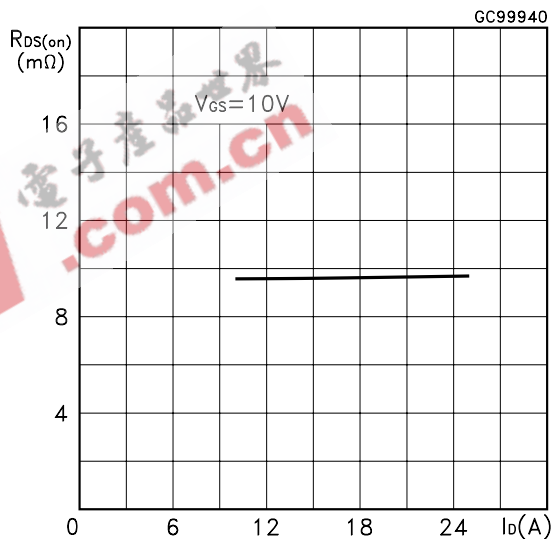
Transfer Characteristics



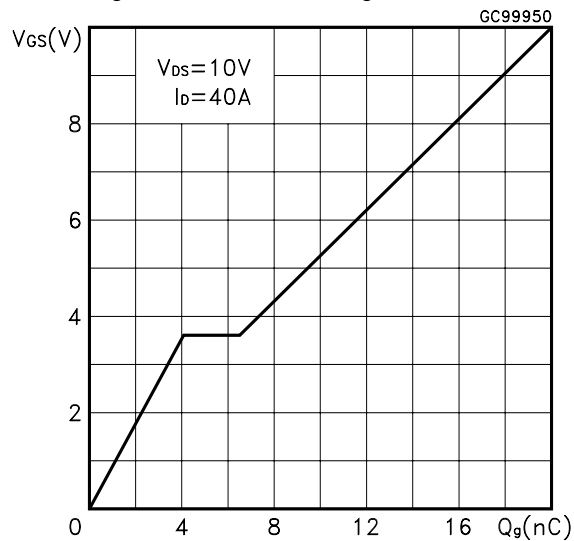
Transconductance



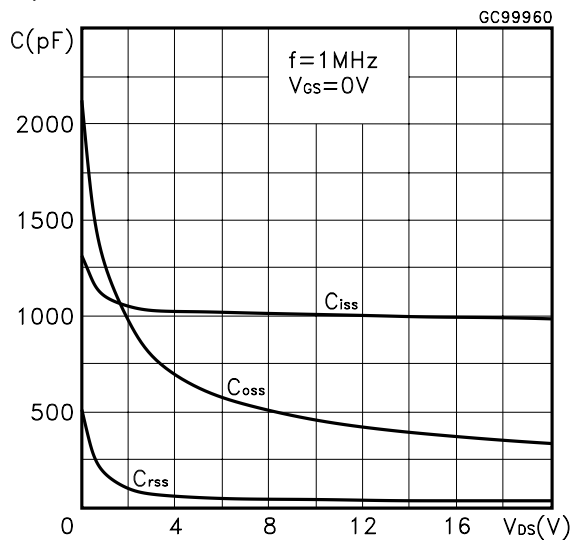
Static Drain-source On Resistance



Gate Charge vs Gate-source Voltage

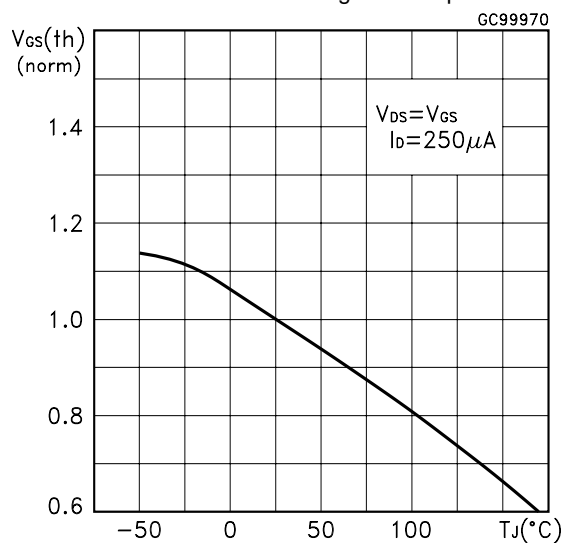


Capacitance Variations

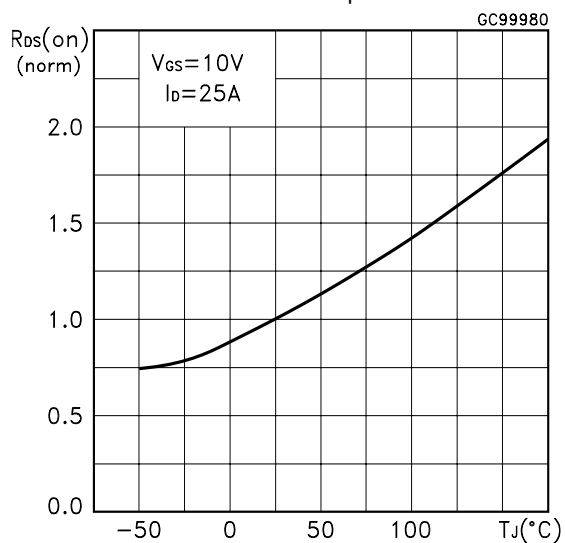


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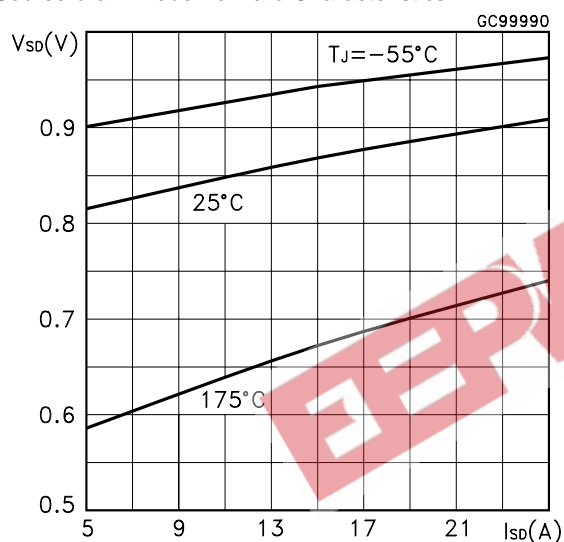
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature

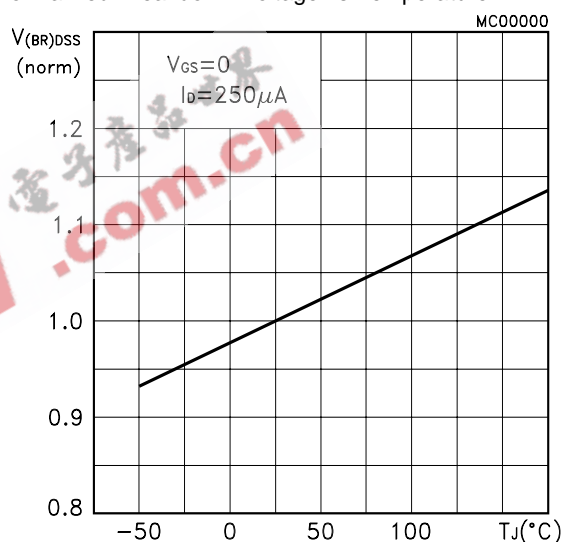


Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuits For Resistive Load

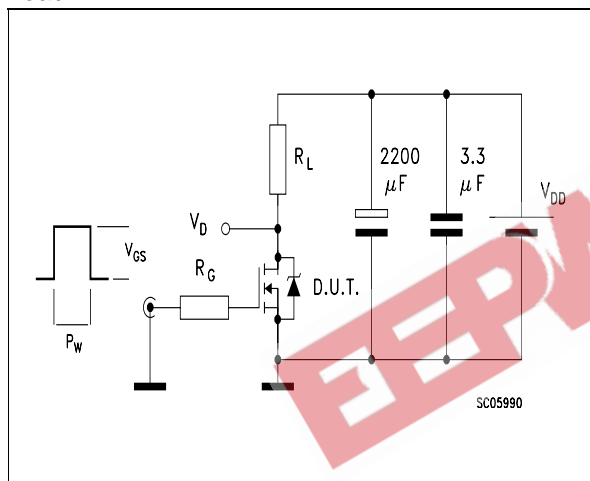


Fig. 4: Gate Charge test Circuit

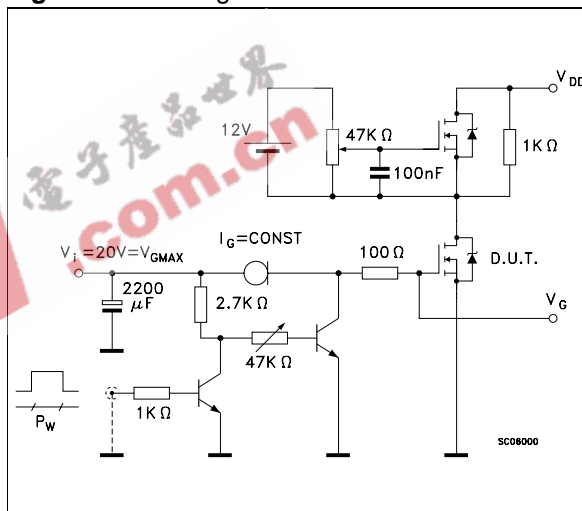
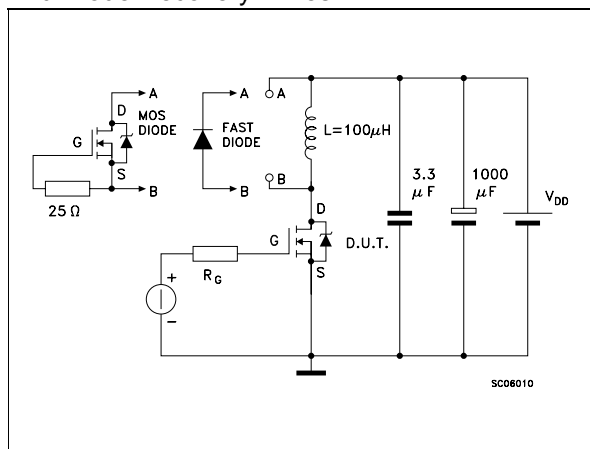
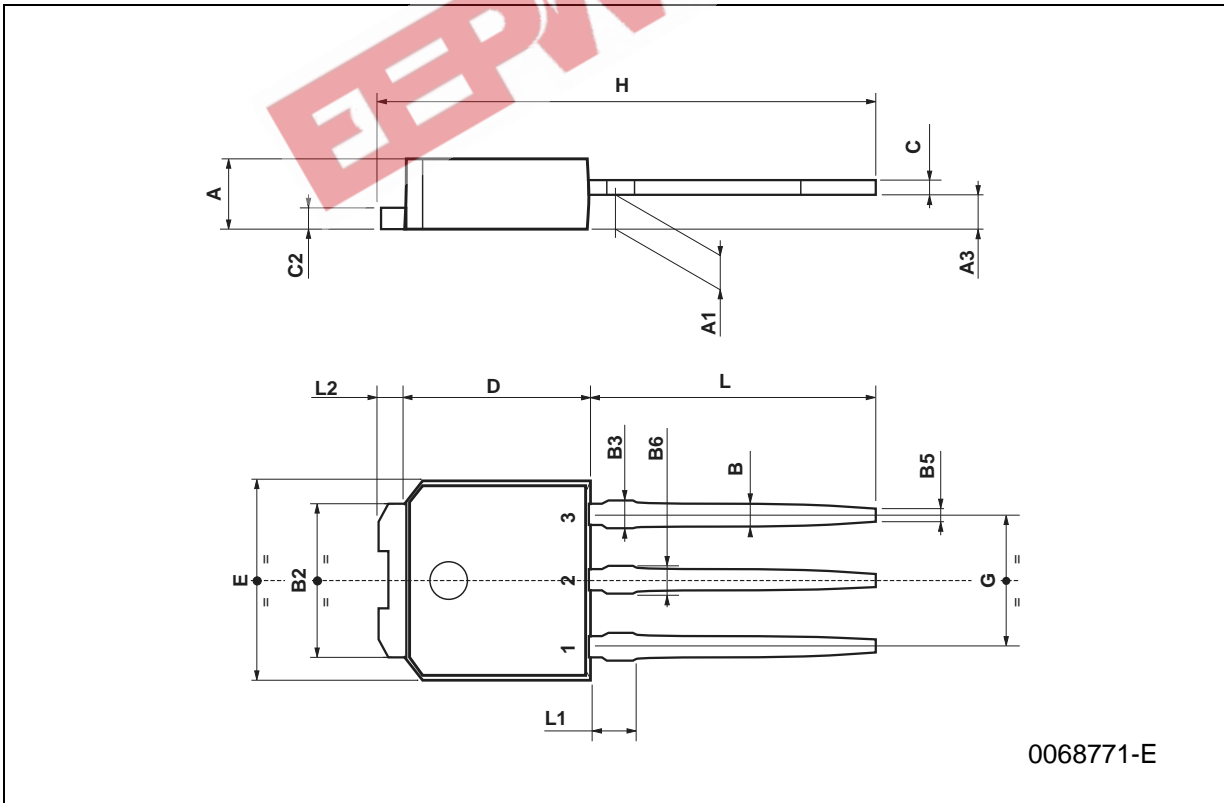


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



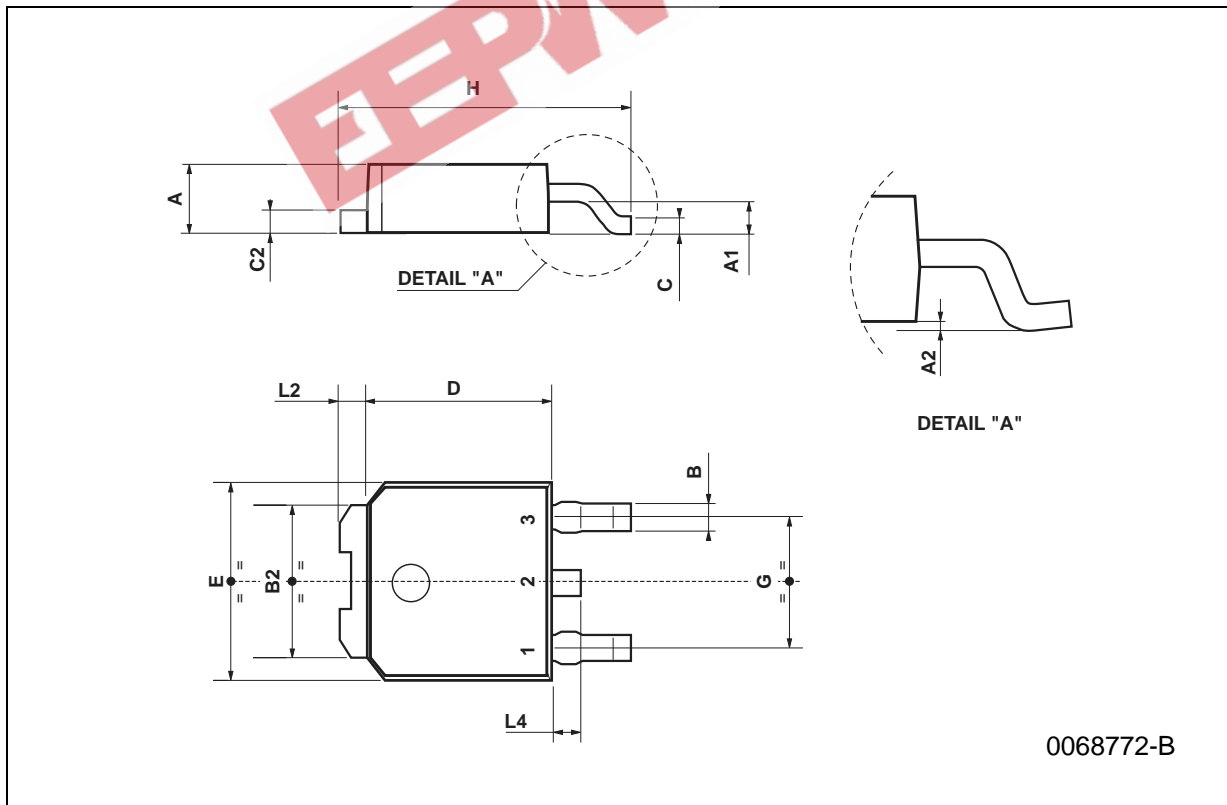
**TO-251 (IPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



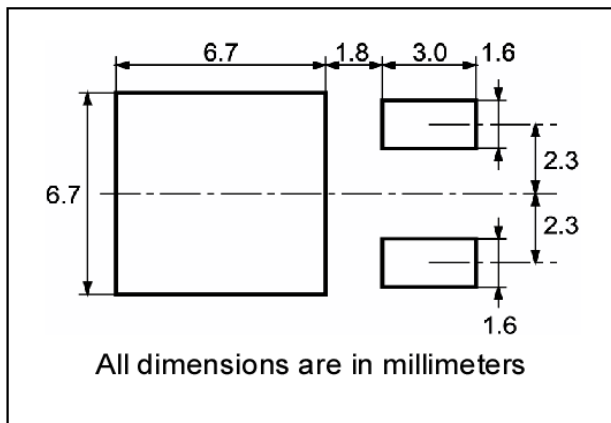
**TO-252 (DPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039

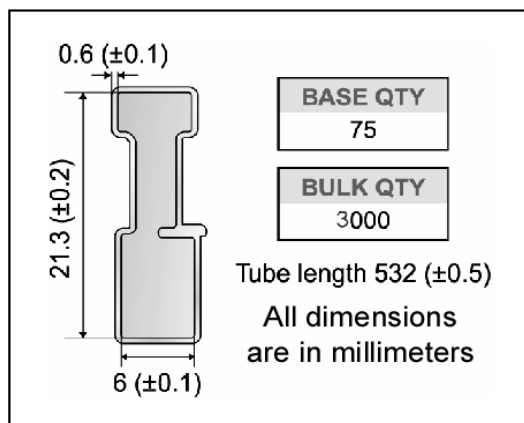




**DPAK FOOTPRINT**



**TUBE SHIPMENT (no suffix)\***



**TAPE AND REEL SHIPMENT (suffix "T4")\***

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

**BASE QTY** 1000      **BULK QTY** 1000

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

For machine ref. only including draft and radii concentric around B0

TOP COVER TAPE

10 pitches cumulative tolerance on tape +/- 0.2 mm

User Direction of Feed

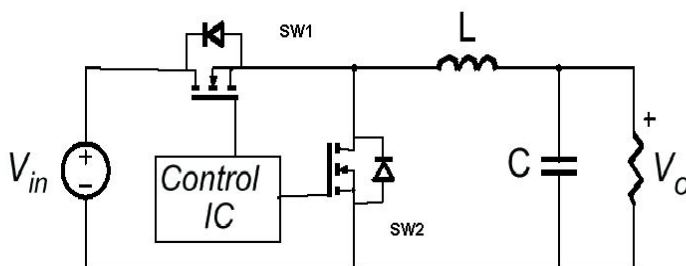
Center line of cavity

FEED DIRECTION

Bending radius R min.

## APPENDIX A

### Buck Converter: Power Losses Estimation



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

- Very low  $R_{DS(on)}$  to reduce conduction losses
- Small  $Q_{gs}$  to reduce the gate charge losses
- Small  $C_{oss}$  to reduce losses due to output capacitance
- Small  $Q_{rr}$  to reduce losses on SW<sub>1</sub> during its turn-on
- The  $C_{gd}/C_{gs}$  ratio lower than  $V_{th}/V_{gg}$  ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;

The high side (SW1) device requires:

- Small  $R_g$  and  $L_s$  to allow higher gate current peak and to limit the voltage feedback on the gate
- Small  $Q_g$  to have a faster commutation and to reduce gate charge losses
- Low  $R_{DS(on)}$  to reduce the conduction losses.

		High Side Switch (SW1)	Low Side Switch (SW2)
P <sub>conduction</sub>		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1 - \delta)$
P <sub>switching</sub>		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
P <sub>diode</sub>	Recovery	Not Applicable	$^1 V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not Applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
P <sub>gate(Q<sub>g</sub>)</sub>		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P <sub>Qoss</sub>		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

Parameter	Meaning
<b>δ</b>	Duty-cycle
<b>Q<sub>gsth</sub></b>	Post threshold gate charge
<b>Q<sub>gls</sub></b>	Third quadrant gate charge
<b>P<sub>conduction</sub></b>	On state losses
<b>P<sub>switching</sub></b>	On-off transition losses
<b>P<sub>diode</sub></b>	Conduction and reverse recovery diode losses
<b>P<sub>gate</sub></b>	Gate drive losses
<b>P<sub>Qoss</sub></b>	Output capacitance losses

<sup>1</sup> Dissipated by SW1 during turn-on



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