

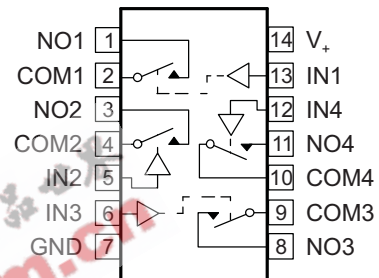
FEATURES

- **Low ON-State Resistance (r_{on})**
 - 0.9 Ω Max (3-V Supply)
 - 1.5 Ω Max (1.8-V Supply)
- **r_{on} Flatness: 0.4 Ω Max (3-V)**
- **r_{on} Matching**
 - 0.05 Ω Max (3-V Supply)
 - 0.25 Ω Max (1.8-V Supply)
- **1.6-V to 3.6-V Single-Supply Operation**
- **1.8-V CMOS Logic Compatible (3-V Supply)**
- **High Current-Handling Capacity (100 mA Continuous)**
- **Fast Switching: $t_{ON} = 14$ ns, $t_{OFF} = 9$ ns**
- **ESD Protection Exceeds JESD-22**
 - 4000-V Human Body Model (A114-A)
 - 300-V Machine Model (A115-A)
 - 1000-V Charged Device Model (C101)

APPLICATIONS

- Power Routing
- Battery Powered Systems
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communications Circuits
- PCMCIA Cards
- Cellular Phones
- Modems
- Hard Drives

TSSOP PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TS3A4751 is a low ON-state resistance (r_{on}), low-voltage, quad, single-pole/single-throw (SPST) analog switch that operates from a single 1.6-V to 3.6-V supply. This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V CMOS compatible when using a single 3-V supply.

The TS3A4751 has four normally open (NO) switches. The TS3A4751 is available in a 14-pin thin shrink small-outline package (TSSOP).

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PWR	Reel of 2000	TS3A4751PWR	YC751

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

IN	NO TO COM, COM TO NO
L	OFF
H	ON



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TS3A4751
0.9-Ω LOW-VOLTAGE SINGLE-SUPPLY QUAD SPST ANALOG SWITCH



SCDS227C–JULY 2006–REVISED SEPTEMBER 2006

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_+	Supply voltage range referenced to GND ⁽²⁾	−0.3	4	V
V_{NO} V_{COM} V_{IN}	Analog and digital voltage range	−0.3	$V_+ + 0.3$	V
I_{NO} I_{COM}	On-state switch current	$V_{NO}, V_{COM} = 0 \text{ to } V_+$		mA
I_+ I_{GND}	Continuous current through V_+ or GND		±100	mA
	Peak current pulsed at 1 ms, 10% duty cycle		±200	mA
θ_{JA}	Package thermal impedance ⁽³⁾		88	°C/W
T_A	Operating temperature range	−40	85	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Signals on COM or NO exceeding V_+ or GND are clamped by internal diodes. Limit forward diode current to maximum current rating.
(3) The package thermal impedance is measured in accordance with JESD 51-7.



Electrical Characteristics for 3-V Supply⁽¹⁾⁽²⁾

$V_+ = 2.7\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$, $V_{IH} = 1.4\text{ V}$, $V_{IL} = 0.5\text{ V}$ (unless otherwise noted).

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	MIN	TYP ⁽³⁾	MAX	UNIT
Analog Switch							
Analog signal range	V_{COM}, V_{NO}			0		V_+	V
ON-state resistance	r_{on}	$V_+ = 2.7\text{ V}$, $I_{COM} = -100\text{ mA}$, $V_{NO} = 1.5\text{ V}$	25°C		0.7	0.9	Ω
			Full			1.1	
ON-state resistance match between channels ⁽⁴⁾	Δr_{on}	$V_+ = 2.7\text{ V}$, $I_{COM} = -100\text{ mA}$, $V_{NO} = 1.5\text{ V}$	25°C		0.03	0.05	Ω
			Full			0.15	
ON-state resistance flatness ⁽⁵⁾	$r_{on(Flat)}$	$V_+ = 2.7\text{ V}$, $I_{COM} = -100\text{ mA}$, $V_{NO} = 1\text{ V}, 1.5\text{ V}, 2\text{ V}$	25°C		0.23	0.4	Ω
			Full			0.5	
NO OFF leakage current ⁽⁶⁾	$I_{NO(OFF)}$	$V_+ = 3.6\text{ V}$, $V_{COM} = 0.3\text{ V}, 3\text{ V}$, $V_{NO} = 3\text{ V}, 0.3\text{ V}$	25°C	-2	1	2	nA
			Full	-18		18	
COM OFF leakage current ⁽⁶⁾	$I_{COM(OFF)}$	$V_+ = 3.6\text{ V}$, $V_{COM} = 0.3\text{ V}, 3\text{ V}$, $V_{NO} = 3\text{ V}, 0.3\text{ V}$	25°C	-2	1	2	nA
			Full	-18		18	
COM ON leakage current ⁽⁶⁾	$I_{COM(ON)}$	$V_+ = 3.6\text{ V}$, $V_{COM} = 0.3\text{ V}, 3\text{ V}$, $V_{NO} = 0.3\text{ V}, 3\text{ V}$, or floating	25°C	-2.5	0.01	2.5	nA
			Full	-5		5	
Dynamic							
Turn-on time	t_{ON}	$V_{NO} = 1.5\text{ V}$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, See Figure 14	25°C		5	14	ns
			Full			15	
Turn-off time	t_{OFF}	$V_{NO} = 1.5\text{ V}$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, See Figure 14	25°C		4	9	ns
			Full			10	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1\text{ nF}$, See Figure 15	25°C		3		pC
NO OFF capacitance	$C_{NO(OFF)}$	$f = 1\text{ MHz}$, See Figure 16	25°C		23		pF
COM OFF capacitance	$C_{COM(OFF)}$	$f = 1\text{ MHz}$, See Figure 16	25°C		20		pF
COM ON capacitance	$C_{COM(ON)}$	$f = 1\text{ MHz}$, See Figure 16	25°C		43		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON	25°C		125		MHz
OFF isolation ⁽⁷⁾	O_{ISO}	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, See Figure 17	$f = 10\text{ MHz}$	25°C		-40	dB
			$f = 1\text{ MHz}$			-62	
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, See Figure 17	$f = 10\text{ MHz}$	25°C		-73	dB
			$f = 1\text{ MHz}$			-95	
Total harmonic distortion	THD	$f = 20\text{ Hz to }20\text{ kHz}$, $V_{COM} = 2\text{ V}_{P-P}$	$R_L = 32\ \Omega$	25°C		0.04	%
			$R_L = 600\ \Omega$			0.003	
Digital Control Inputs (IN1–IN4)							
Input logic high	V_{IH}		Full		1.4		V
Input logic low	V_{IL}		Full			0.5	V
Input leakage current	I_{IN}	$V_I = 0\text{ or }V_+$	25°C		0.5	1	nA
			Full		-20	20	
Supply							
Power-supply range	V_+				1.6	3.6	V
Positive-supply current	I_+	$V_+ = 3.6\text{ V}$, $V_{IN} = 0\text{ or }V_+$	25°C			0.075	μA
			Full			0.75	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.

(3) Typical values are at $V_+ = 3\text{ V}$, $T_A = 25^\circ\text{C}$.

(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$

(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.

(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at $T_A = 25^\circ\text{C}$.

(7) OFF isolation = $20_{\log 10}(V_{COM}/V_{NO})$, V_{COM} = output, V_{NO} = input to OFF switch

TS3A4751

0.9-Ω LOW-VOLTAGE SINGLE-SUPPLY QUAD SPST ANALOG SWITCH



SCDS227C–JULY 2006–REVISED SEPTEMBER 2006

Electrical Characteristics for 1.8-V Supply⁽¹⁾⁽²⁾

$V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$, $V_{IH} = 1\text{ V}$, $V_{IL} = 0.4\text{ V}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	MIN	TYP ⁽³⁾	MAX	UNIT
Analog Switch							
Analog signal range	V_{COM}, V_{NO}			0		V_+	V
ON-state resistance	r_{on}	$V_+ = 1.8\text{ V}$, $I_{COM} = -10\text{ mA}$, $V_{NO} = 0.9\text{ V}$	25°C		1	1.5	Ω
			Full			2	
ON-state resistance match between channels ⁽⁴⁾	Δr_{on}	$V_+ = 1.8\text{ V}$, $I_{COM} = -10\text{ mA}$, $V_{NO} = 0.9\text{ V}$	25°C		0.09	0.15	Ω
			Full			0.25	
ON-state resistance flatness ⁽⁵⁾	$r_{on(Flat)}$	$V_+ = 1.8\text{ V}$, $I_{COM} = -10\text{ mA}$, $0 \leq V_{NO} \leq V_+$	25°C		0.7	0.9	Ω
			Full			1.5	
NO OFF leakage current ⁽⁶⁾	$I_{NO(OFF)}$	$V_+ = 1.95\text{ V}$, $V_{COM} = 0.15\text{ V}$, 1.65 V , $V_{NO} = 1.8\text{ V}$, 0.15 V	25°C	-1	0.5	1	nA
			Full	-10		10	
COM OFF leakage current ⁽⁶⁾	$I_{COM(OFF)}$	$V_+ = 1.95\text{ V}$, $V_{COM} = 0.15\text{ V}$, 1.65 V , $V_{NO} = 1.65\text{ V}$, 0.15 V	25°C	-1	0.5	1	nA
			Full	-10		10	
COM ON leakage current ⁽⁶⁾	$I_{COM(ON)}$	$V_+ = 1.95\text{ V}$, $V_{COM} = 0.15\text{ V}$, 1.65 V , $V_{NO} = 0.15\text{ V}$, 1.65 V , or floating	25°C	-1	0.01	1	nA
			Full	-3		3	
Dynamic							
Turn-on time	t_{ON}	$V_{NO} = 1.5\text{ V}$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, See Figure 14	25°C		6	18	ns
			Full			20	
Turn-off time	t_{OFF}	$V_{NO} = 1.5\text{ V}$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, See Figure 14	25°C		5	10	ns
			Full			12	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1\text{ nF}$, See Figure 15	25°C		3.2		pC
NO OFF capacitance	$C_{NO(OFF)}$	$f = 1\text{ MHz}$, See Figure 16	25°C		23		pF
COM OFF capacitance	$C_{COM(OFF)}$	$f = 1\text{ MHz}$, See Figure 16	25°C		20		pF
COM ON capacitance	$C_{COM(ON)}$	$f = 1\text{ MHz}$, See Figure 16	25°C		43		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON	25°C		123		MHz
OFF isolation ⁽⁷⁾	O_{ISO}	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, See Figure 17	f = 10 MHz	25°C		-61	dB
			f = 100 MHz			-36	
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, See Figure 17	f = 10 MHz	25°C		-95	dB
			f = 100 MHz			-73	
Total harmonic distortion	THD	f = 20 Hz to 20 kHz, V_{COM} = 2 V_{P-P}	$R_L = 32\ \Omega$	25°C		0.14	%
			$R_L = 600\ \Omega$			0.013	
Digital Control Inputs (IN1–IN4)							
Input logic high	V_{IH}		Full		1		V
Input logic low	V_{IL}		Full			0.4	V
Input leakage current	I_{IN}	$V_I = 0\text{ or }V_+$	25°C		0.1	5	nA
			Full	-10		10	
Supply							
Power-supply range	V_+				1.6	3.6	V
Positive-supply current	I_+	$V_I = 0\text{ or }V_+$	25°C			0.05	μA
			Full			0.5	

- (1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.
- (3) Typical values are at $T_A = 25^\circ\text{C}$.
- (4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$
- (5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.
- (6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at $T_A = 25^\circ\text{C}$.
- (7) OFF isolation = $20_{\log 10}(V_{COM}/V_{NO})$, V_{COM} = output, V_{NO} = input to OFF switch

TYPICAL PERFORMANCE

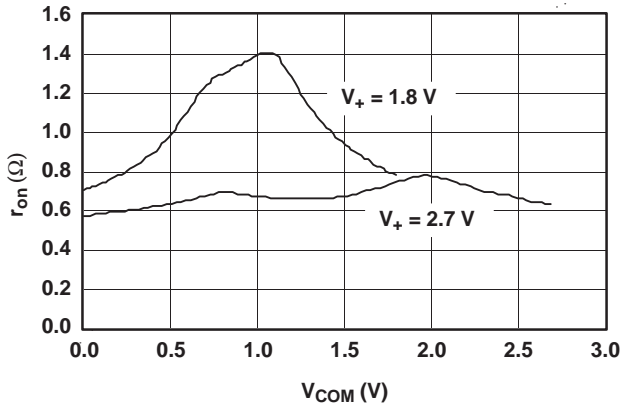


Figure 1. r_{on} vs V_{COM}

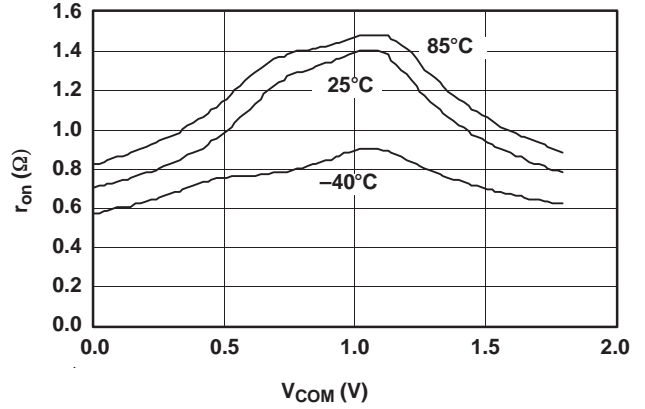


Figure 2. r_{on} vs V_{COM} ($V_+ = 1.8$ V)

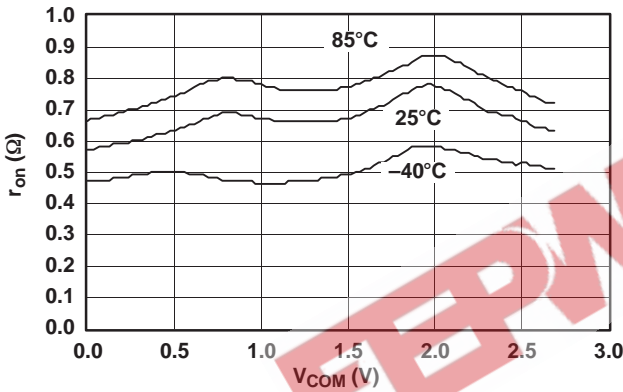


Figure 3. r_{on} vs V_{COM} ($V_+ = 2.7$ V)

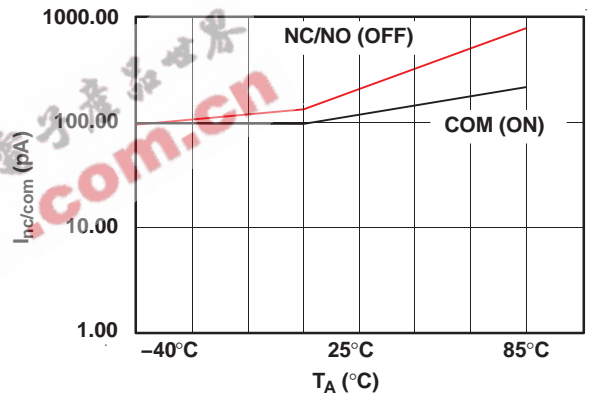


Figure 4. I_{ON} and I_{OFF} vs Temperature ($V_+ = 3.6$ V)

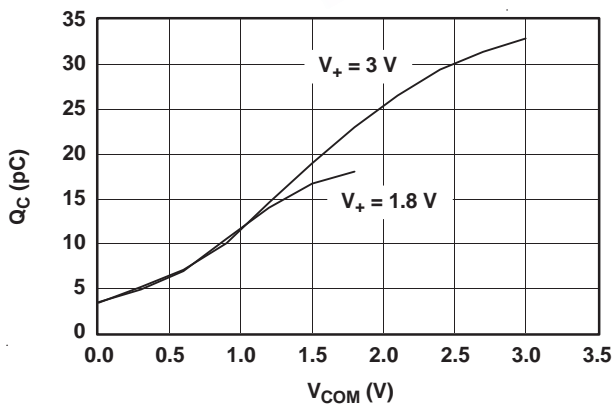


Figure 5. Q_C vs V_{COM}

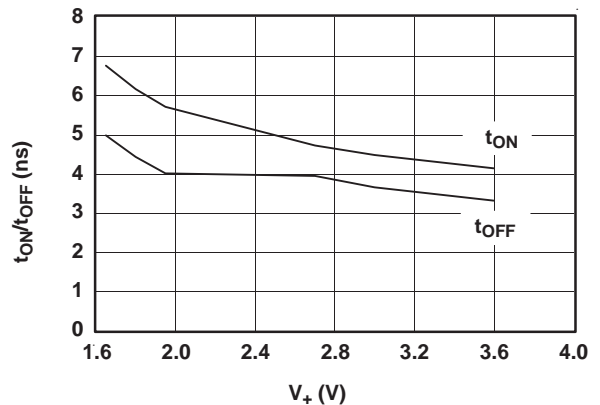


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

TYPICAL PERFORMANCE (continued)

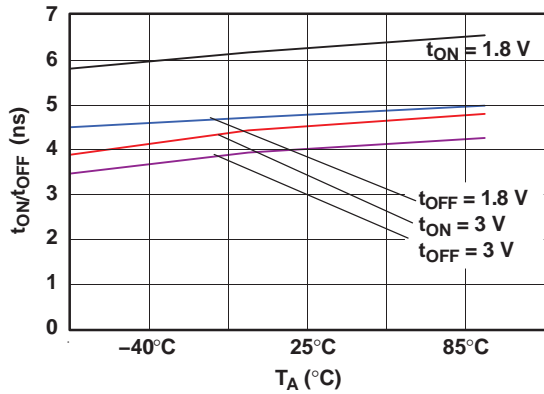


Figure 7. t_{ON} and t_{OFF} vs Temperature

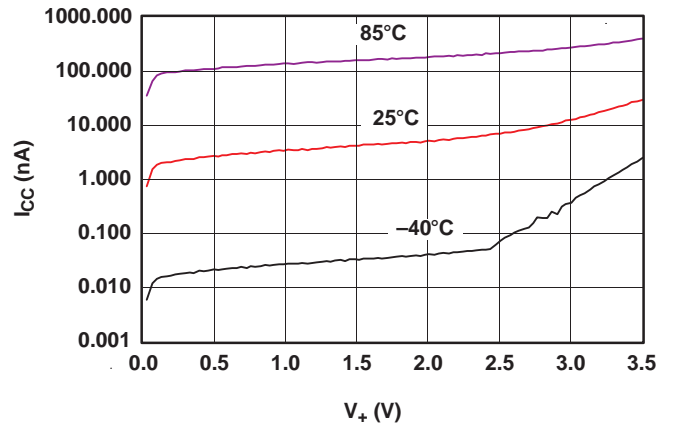


Figure 8. I_{CC} vs V_+

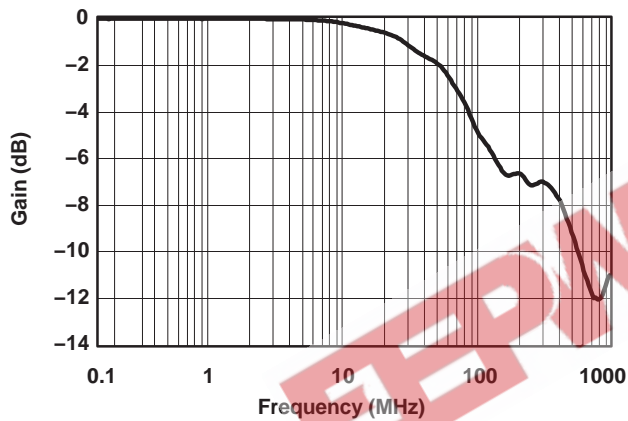


Figure 9. Gain vs Frequency
 ($V_+ = 3\text{ V}$)

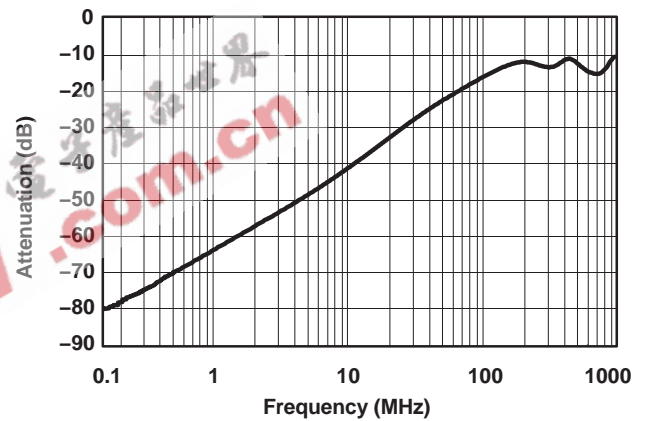


Figure 10. OFF Isolation vs Frequency
 ($V_+ = 3\text{ V}$)

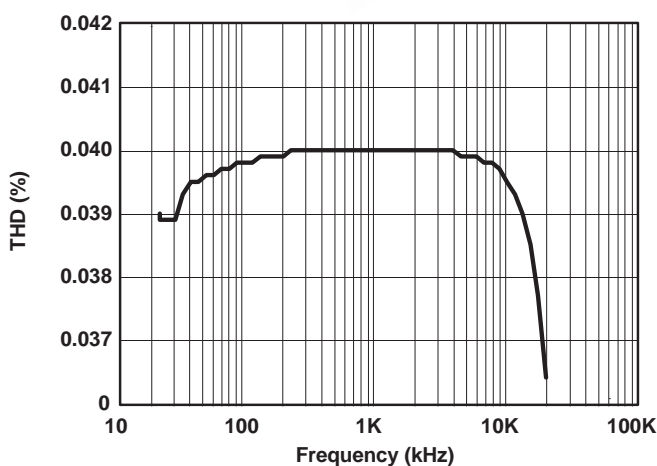


Figure 11. Total Harmonic Distortion vs Frequency
 ($R_L = 32\ \Omega$)

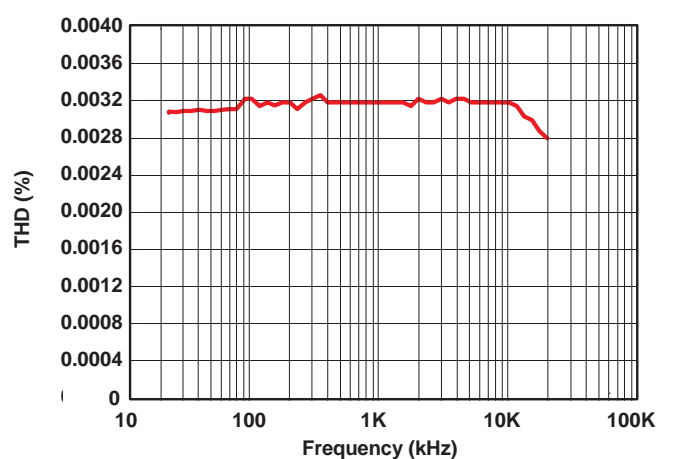


Figure 12. Total Harmonic Distortion vs Frequency
 ($R_L = 600\ \Omega$)

TYPICAL PERFORMANCE (continued)

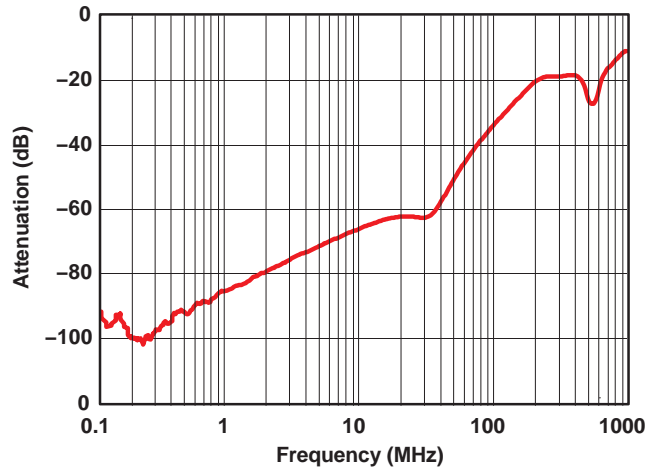


Figure 13. Crosstalk vs Frequency ($V_+ = 3\text{ V}$)

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1, 3, 8, 11	NO1, NO2, NO3, NO4	Normally open
2, 4, 9, 10	COM1, COM2, COM3, COM4	Common
7	GND	Ground
13, 5, 6, 12	IN1, IN2, IN3, IN4	Logic control inputs
14	V_+	Positive supply voltage

APPLICATION INFORMATION

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_+ on first, followed by NO or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_+ supply to other components. A 0.1- μ F capacitor, connected from V_+ to GND, is adequate for most applications.

Logic Inputs

The TS3A4751 logic inputs can be driven up to 3.6 V, regardless of the supply voltage. For example, with a 1.8-V supply, IN may be driven low to GND and high to 3.6 V. Driving IN rail to rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V_+ to GND) can be passed with very little change in r_{on} (see Typical Operating Characteristics). The switches are bidirectional, so NO and COM can be used as either inputs or outputs.

Layout

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

TEST CIRCUITS/TIMING DIAGRAMS

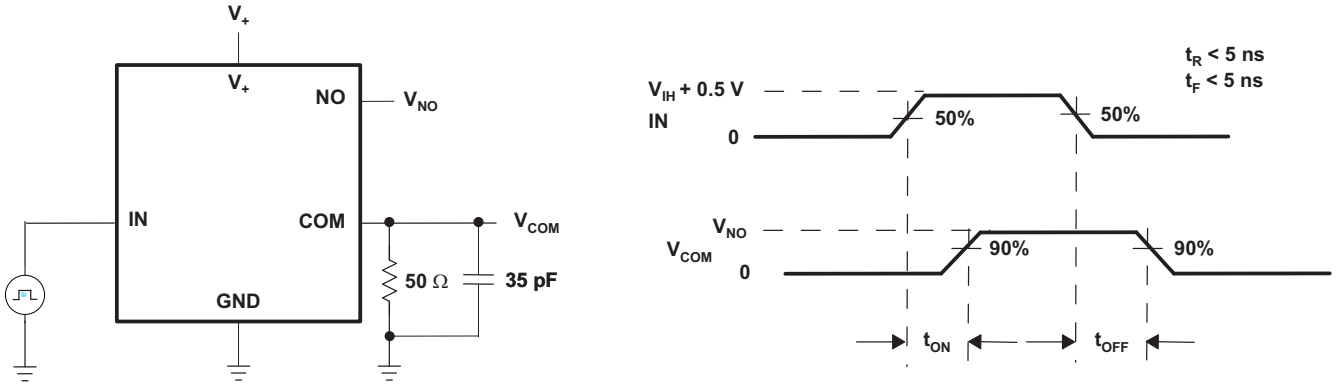


Figure 14. Switching Times

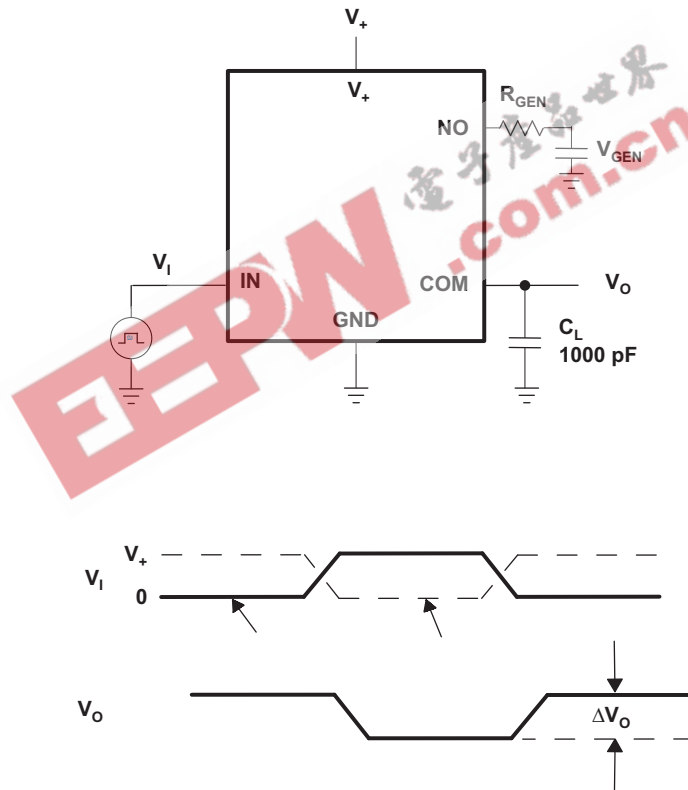


Figure 15. Charge Injection (Q_C)

TEST CIRCUITS/TIMING DIAGRAMS (continued)

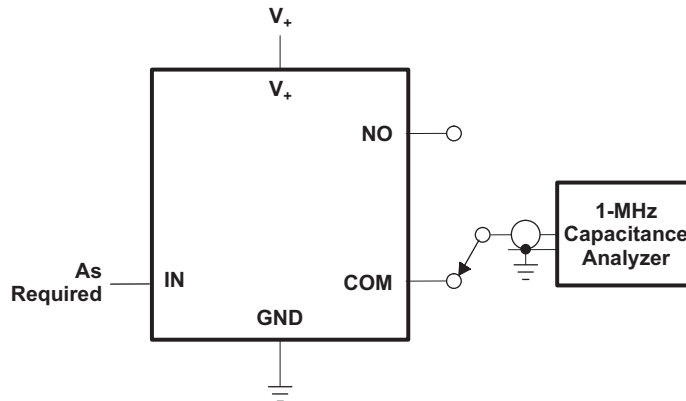


Figure 16. NO and COM Capacitance

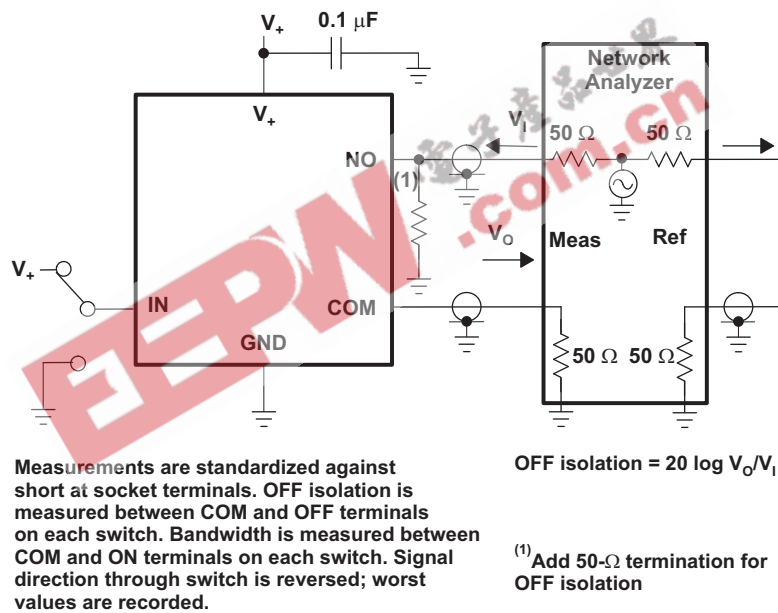
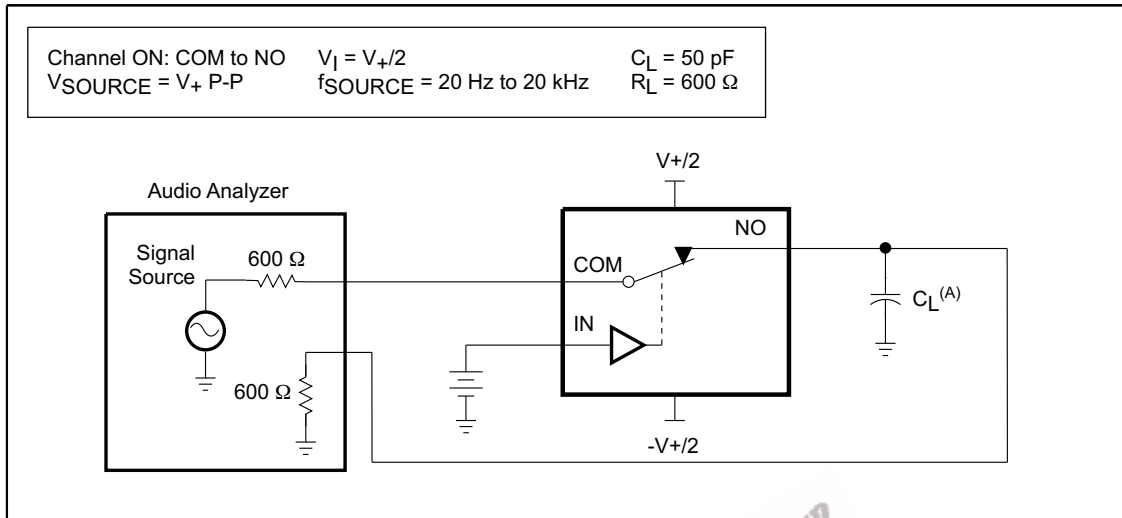


Figure 17. OFF Isolation, Bandwidth, and Crosstalk

TEST CIRCUITS/TIMING DIAGRAMS (continued)



A. C_L includes probe and jig capacitance.

Figure 18. Total Harmonic Distortion (THD)

EEPW.com.cn 电子元件世界

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TS3A4751PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A4751PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

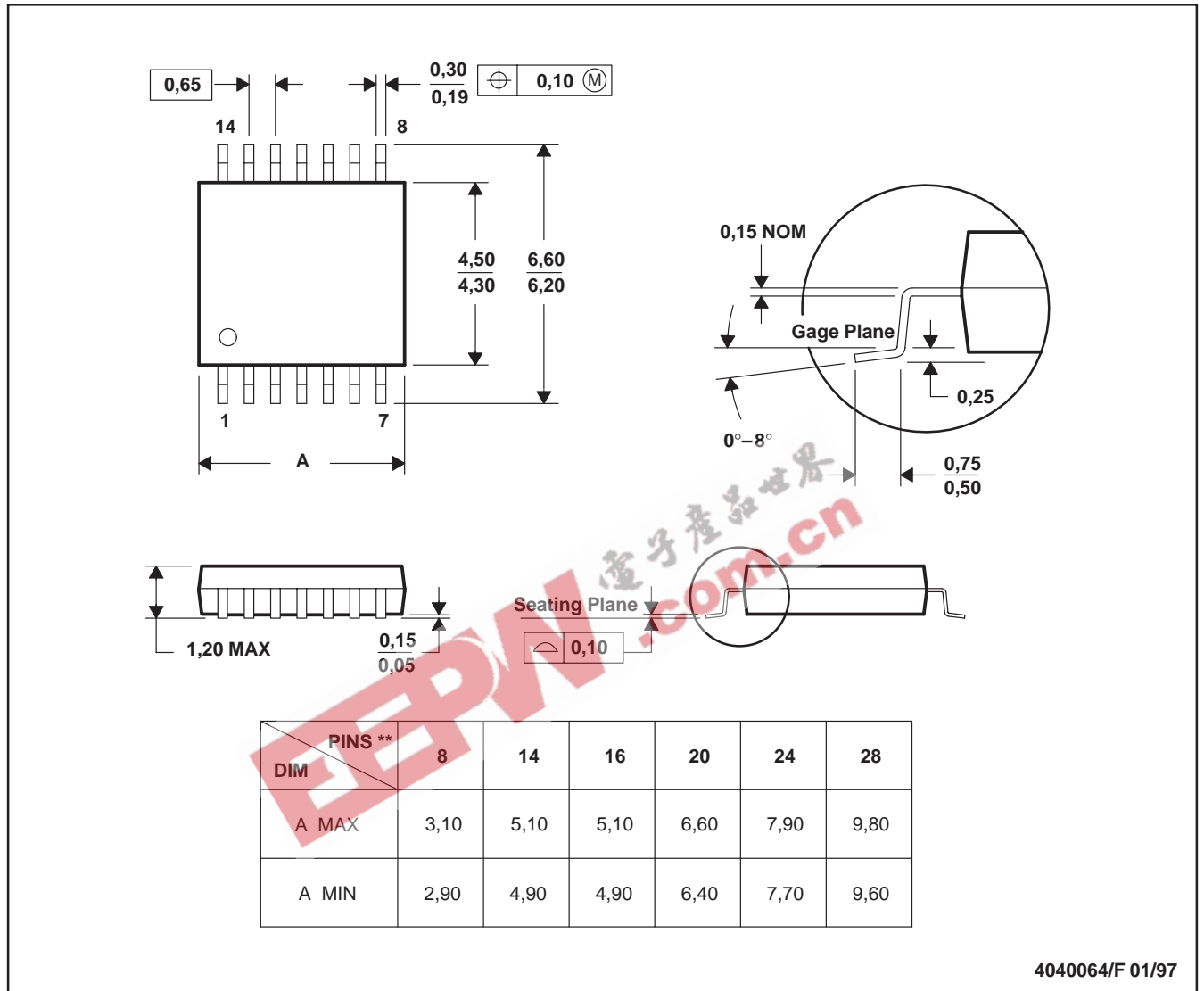
MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265