

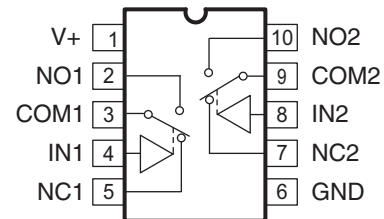
FEATURES

- Specified Break-Before-Make Switching
- Low ON-State Resistance (0.3 Ω Max)
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 3.6-V Single-Supply Operation
- Control Inputs Are 1.8-V Logic Compatible
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

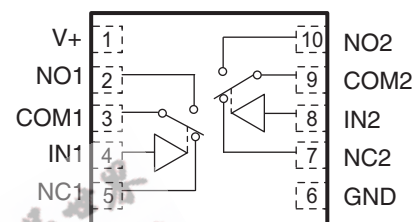
APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals

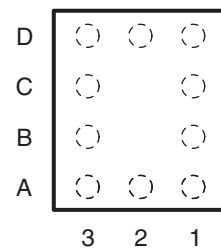
DGS PACKAGE
(TOP VIEW)



DRC PACKAGE
(TOP VIEW)



YZP PACKAGE
(TOP-THROUGH VIEW)



YZP PACKAGE TERMINAL ASSIGNMENTS

D	NO2	V+	NO1
C	COM2		COM1
B	IN2		IN1
A	NC2	GND	NC1
	3	2	1

DESCRIPTION/ORDERING INFORMATION

The TS3A24159 is a dual single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 3.6 V. It offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

TS3A24159
0.3-Ω DUAL SPDT ANALOG SWITCH
DUAL-CHANNEL 2:1 MULTIPLEXER/DEMULPLEXER



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ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	NanoFree™ (DSBGA) – YZP	Reel of 3000	TS3A24159YZPR	L87
	VSSOP – DGS (MSOP)	Reel of 2500	TS3A24159DGSR	L8R
	SON – DRC	Reel of 3000	TS3A24159DRCR	ZWS

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

SUMMARY OF CHARACTERISTICS⁽¹⁾

Configuration	Dual 2:1 Multiplexer/Demultiplexer (2 × SPDT)
Number of channels	2
ON-state resistance (r _{on})	0.3 Ω Max
ON-state resistance match (Δr _{on})	0.05 Ω Max
ON-state resistance flatness (r _{on(flat)})	0.04 Ω Max
Turn-on/turn-off time (t _{ON} /t _{OFF})	20 ns/12 ns
Break-before-make time (t _{BBM})	10 ns
Charge injection (Q _C)	9 pC
Bandwidth (BW)	23 MHz
OFF isolation (O _{ISO})	–72 dB
Crosstalk (X _{TALK})	–96 dB
Total harmonic distortion (THD)	0.003%
Power-supply current (I ₊)	15 nA
Package options	10-pin MSOP, SON, DSBGA

(1) V₊ = 2.7 V, T_A = 25°C

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V+	Supply voltage range ⁽³⁾	−0.5	3.6	V
V _{NC} V _{NO} V _{COM}	Analog voltage range ⁽³⁾⁽⁴⁾⁽⁵⁾	−0.5	V+ + 0.5	V
I _{I/O}	Analog port diode current	V _{NC} , V _{NO} , V _{COM} < 0		mA
I _{NC} I _{NO} I _{COM}	ON-state switch current	−300	300	mA
	ON-state peak switch current ⁽⁶⁾	−500	500	
V _I	Digital input voltage range	−0.5	3.6	V
I _{IK}	Digital input clamp current ⁽³⁾⁽⁴⁾	−50		mA
I+	Continuous current through V+		100	mA
I _{GND}	Continuous current through GND	−100		mA
θ _{JA}	Package thermal impedance ⁽⁷⁾	DGS package		165
		DRC package		56.5
		YZP package		93
T _{stg}	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration <10% duty cycle
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

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ELECTRICAL CHARACTERISTICS FOR 3-V SUPPLY⁽¹⁾

V₊ = 2.7 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A	V ₊	MIN	TYP	MAX	UNIT	
Analog Switch									
Analog signal range	V _{COM} , V _{NO} , V _{NC}				0		V ₊	V	
Peak ON resistance	r _{peak}	0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V	0.2	0.3	Ω	
				Full		0.35			
ON-state resistance	r _{on}	V _{NO} or V _{NC} = 2 V, I _{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V	0.26	0.3	Ω	
				Full		0.34			
ON-state resistance match between channels	Δr _{on}	V _{NO} or V _{NC} = 2 V, 0.8 V, I _{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V	0.01	0.05	Ω	
				Full		0.05			
ON-state resistance flatness	r _{on(flat)}	0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = –100 mA,	Switch ON, See Figure 10	25°C	2.7 V	0.13		Ω	
				Full		0.01	0.04		Ω
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 1 V, V _{COM} = 3 V, or V _{NC} or V _{NO} = 3 V, V _{COM} = 1 V,	Switch OFF, See Figure 11	25°C	3.6 V	–10	10	nA	
				Full		–50	50		
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 1 V, V _{COM} = Open, or V _{NC} or V _{NO} = 3 V, V _{COM} = Open,	Switch ON, See Figure 12	25°C	3.6 V	–10	10	nA	
				Full		–100	100		
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = Open, V _{COM} = 1 V, or V _{NC} or V _{NO} = Open, V _{COM} = 3 V,	Switch ON, See Figure 12	25°C	3.6 V	–10	10	nA	
				Full		–100	100		
Digital Control Inputs (IN1, IN2)⁽²⁾									
Input logic high	V _{IH}		Full		1.4			V	
Input logic low	V _{IL}		Full			0.5		V	
Input leakage current	I _{IH} , I _{IL}	V _I = 3.6 V or 0		25°C	3.6 V	–40	5	40	nA
				Full		–50	50		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V₊ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 3-V SUPPLY (continued)
 $V_+ = 2.7\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT	
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 14	25°C	3 V	20	35	ns	
				Full	2.7 V to 3.6 V		40		
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 14	25°C	3 V	12	25	ns	
				Full	2.7 V to 3.6 V		30		
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35\text{ pF}$, See Figure 15	25°C	3 V	1	10	25	ns
				Full	2.7 V to 3.6 V	0.5		30	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 1\text{ nF}$, See Figure 19	25°C	3 V	9		pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF,	See Figure 13	25°C	3 V	90		pF	
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON,	See Figure 13	25°C	3 V	224		pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 13	25°C	3 V	250		pF	
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 13	25°C	3 V	2		pF	
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 16	25°C	3 V	23		MHz	
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$,	See Figure 17	25°C	3 V	-72		dB	
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$,	See Figure 18	25°C	3 V	-96		dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$,	$f = 20\text{ Hz to }20\text{ kHz}$, See Figure 20	25°C	3 V	0.00	3	%	
Supply									
Positive supply current	I_+	$V_I = V_+$ or GND	25°C	3.6 V	15	100		nA	
			Full		1			μA	

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ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY⁽¹⁾

V₊ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A	V ₊	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	V _{COM} , V _{NO} , V _{NC}				0		V ₊	V
Peak ON resistance	r _{peak}	0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V			0.35
				Full				0.45
ON-state resistance	r _{on}	V _{NO} or V _{NC} = 1.8 V, I _{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V			
				Full				0.4
ON-state resistance match between channels	Δr _{on}	V _{NO} or V _{NC} = 1.8 V, 0.8 V, I _{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V	0.01	0.05	Ω
				Full		0.05	0.05	
ON-state resistance flatness	r _{on(flat)}	0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = –8 mA,	Switch ON, See Figure 10	25°C	2.3 V			0.05
				Full		25°C	0.03	0.08
						Full		
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 0.5 V, V _{COM} = 2.2 V, or V _{NC} or V _{NO} = 2.2 V, V _{COM} = 0.5 V,	Switch OFF, See Figure 11	25°C	2.7 V	–10	10	nA
				Full		–50	50	
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 0.5 V, V _{COM} = Open, or V _{NC} or V _{NO} = 2.2 V, V _{COM} = Open,	Switch ON, See Figure 12	25°C	2.7 V	–10	10	nA
				Full		–100	100	
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = Open, V _{COM} = 0.5 V, or V _{NC} or V _{NO} = Open, V _{COM} = 2.2 V,	Switch ON, See Figure 12	25°C	2.7 V	–10	10	nA
				Full		–100	100	
Digital Control Inputs (IN1, IN2)⁽²⁾								
Input logic high	V _{IH}		Full		1.25			V
Input logic low	V _{IL}		Full				0.5	V
Input leakage current	I _{IH} , I _{IL}	V _I = 2.7 V or 0		25°C	2.7 V	–40	5	40
				Full		–50	50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) All unused digital inputs of the device must be held at V₊ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY (continued)

V₊ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A	V ₊	MIN	TYP	MAX	UNIT
Dynamic								
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω, C _L = 35 pF, See Figure 14	25°C	2.5 V	23	45	50	ns
			Full	2.3 V to 2.7 V				
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω, C _L = 35 pF, See Figure 14	25°C	2.5 V	17	27	30	ns
			Full	2.3 V to 2.7 V				
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V ₊ , R _L = 50 Ω, C _L = 35 pF, See Figure 15	25°C	2.5 V	2	14	30	ns
			Full	2.3 V to 2.7 V	1		35	
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0, C _L = 1 nF, See Figure 19	25°C	2.5 V		8		pC
NC, NO OFF capacitance	C _{NC(OFF)} , C _{NO(OFF)}	V _{NC} or V _{NO} = V ₊ or GND, Switch OFF, See Figure 13	25°C	2.5 V		90		pF
NC, NO ON capacitance	C _{NC(ON)} , C _{NO(ON)}	V _{NC} or V _{NO} = V ₊ or GND, Switch ON, See Figure 13	25°C	2.5 V		250		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON, See Figure 13	25°C	2.5 V		250		pF
Digital input capacitance	C _I	V _I = V ₊ or GND, See Figure 13	25°C	2.5 V		2		pF
Bandwidth	BW	R _L = 50 Ω, Switch ON, See Figure 16	25°C	2.5 V		23		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz, See Figure 17	25°C	2.5 V		–72		dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 1 MHz, See Figure 18	25°C	2.5 V		–96		dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF, f = 20 Hz to 20 kHz, See Figure 20	25°C	2.5 V		0.00 3		%
Supply								
Positive supply current	I ₊	V _I = V ₊ or GND	25°C	2.7 V	10	100	700	nA
			Full					

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ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY⁽¹⁾

V₊ = 1.65 V to 1.95 V, T_A = -40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A	V ₊	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	V _{COM} , V _{NO} , V _{NC}				0		V ₊	V
Peak ON resistance	r _{peak}	0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = -2 mA,	Switch ON, See Figure 10	25°C Full	1.65 V	0.4	0.9 0.8	Ω
ON-state resistance	r _{on}	V _{NO} or V _{NC} = 1.5 V, I _{COM} = -2 mA,	Switch ON, See Figure 10	25°C Full	1.65 V	0.3	0.45 0.5	Ω
ON-state resistance match between channels	Δr _{on}	V _{NO} or V _{NC} = 0.6 V, 1.5 V, I _{COM} = -2 mA,	Switch ON, See Figure 10	25°C Full	1.65 V	0.02	0.04 0.05	Ω
ON-state resistance flatness	r _{on(flat)}	0 ≤ (V _{NO} or V _{NC}) ≤ V ₊ , I _{COM} = -2 mA, V _{NO} or V _{NC} = 0.6 V, 1.5 V, I _{COM} = -8 mA,	Switch ON, See Figure 10	25°C Full	1.65 V	0.13	0.08 0.15 0.2	Ω
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 0.3 V, V _{COM} = 1.65 V, or V _{NC} or V _{NO} = 1.65 V, V _{COM} = 0.3 V,	Switch OFF, See Figure 11	25°C Full	1.95 V	-10	10 50	nA
NC, NO ON leakage current	I _{NC(ON)} , I _{NO(ON)}	V _{NC} or V _{NO} = 0.3 V, V _{COM} = Open, or V _{NC} or V _{NO} = 1.65 V, V _{COM} = Open,	Switch ON, See Figure 12	25°C Full	1.95 V	-10	10 100	nA
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = Open, V _{COM} = 0.3 V, or V _{NC} or V _{NO} = Open, V _{COM} = 1.65 V,	Switch ON, See Figure 12	25°C Full	1.95 V	-10	10 100	nA
Digital Control Inputs (IN1, IN2)⁽²⁾								
Input logic high	V _{IH}			Full		1		V
Input logic low	V _{IL}			Full			0.4	V
Input leakage current	I _{IH} , I _{IL}	V _I = 1.95 V or 0		25°C Full	1.95 V	-40	5 40 50	nA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V₊ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY (continued)

V+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A	V+	MIN	TYP	MAX	UNIT
Dynamic								
Turn-on time	t _{ON}	V _{COM} = V+, R _L = 50 Ω, C _L = 35 pF, See Figure 14	25°C	1.8 V		53	75	ns
			Full	1.65 V to 1.95 V			30	
Turn-off time	t _{OFF}	V _{COM} = V+, R _L = 50 Ω, C _L = 35 pF, See Figure 14	25°C	1.8 V		24	35	ns
			Full	1.65 V to 1.95 V			40	
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V+, R _L = 50 Ω, C _L = 35 pF, See Figure 15	25°C	1.8 V	2	30	40	ns
			Full	1.65 V to 1.95 V	1		50	
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0, C _L = 1 nF, See Figure 19	25°C	1.8 V		5		pC
NC, NO OFF capacitance	C _{NC(OFF)} , C _{NO(OFF)}	V _{NC} or V _{NO} = V+ or GND, Switch OFF, See Figure 13	25°C	1.8 V		90		pF
NC, NO ON capacitance	C _{NC(ON)} , C _{NO(ON)}	V _{NC} or V _{NO} = V+ or GND, Switch ON, See Figure 13	25°C	1.8 V		250		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V+ or GND, Switch ON, See Figure 13	25°C	1.8 V		250		pF
Digital input capacitance	C _I	V _I = V+ or GND, See Figure 13	25°C	1.8 V		2		pF
Bandwidth	BW	R _L = 50 Ω, Switch ON, See Figure 16	25°C	1.8 V		23		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz, See Figure 17	25°C	1.8 V		–73		dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 1 MHz, See Figure 18	25°C	1.8 V		–97		dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF, f = 20 Hz to 20 kHz, See Figure 20	25°C	1.8 V		0.00 5		%
Supply								
Positive supply current	I+	V _I = V+ or GND	25°C	1.95 V		100	50	nA
			Full				700	

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TYPICAL PERFORMANCE

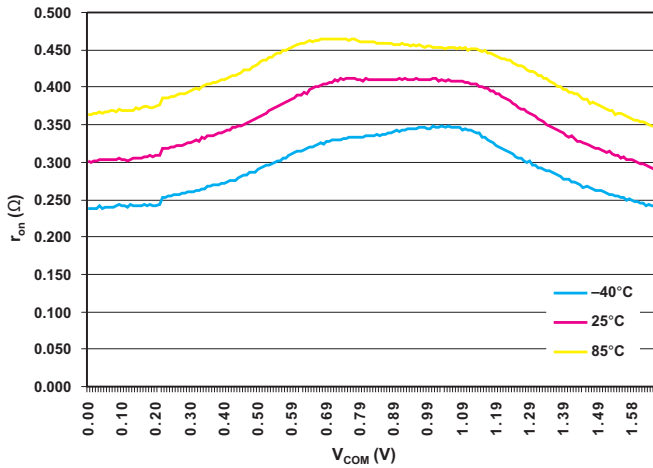


Figure 1. r_{on} vs V_{COM}
($V_+ = 1.65$ V)

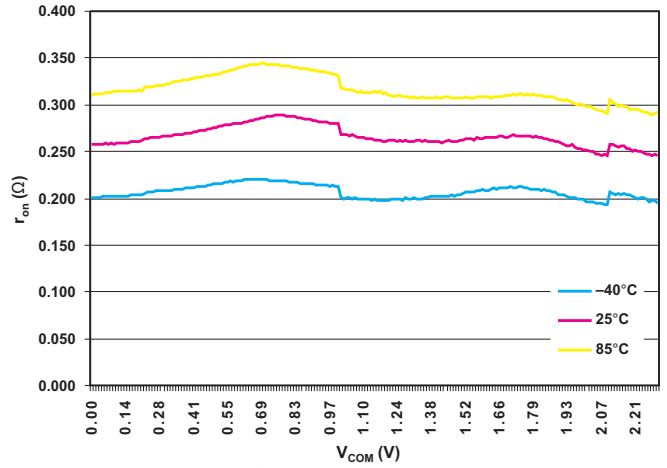


Figure 2. r_{on} vs V_{COM}
($V_+ = 2.3$ V)

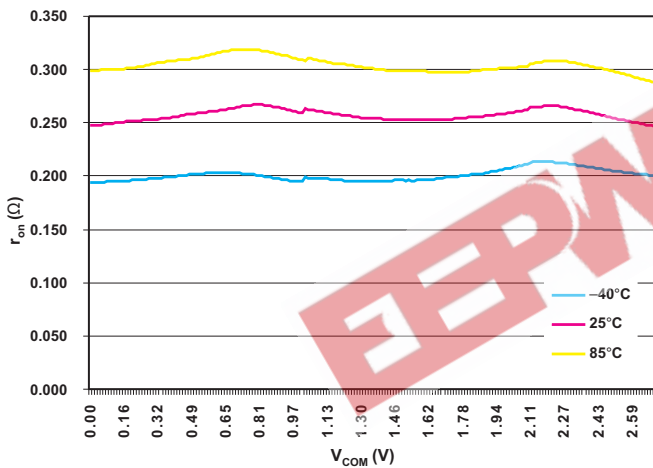


Figure 3. r_{on} vs V_{COM}
($V_+ = 2.7$ V)

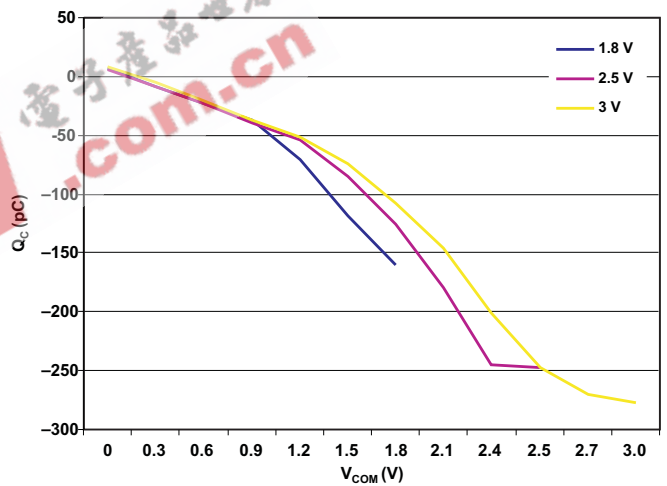


Figure 4. Charge Injection (Q_C) vs V_{COM}
($T_A = 25^\circ\text{C}$)

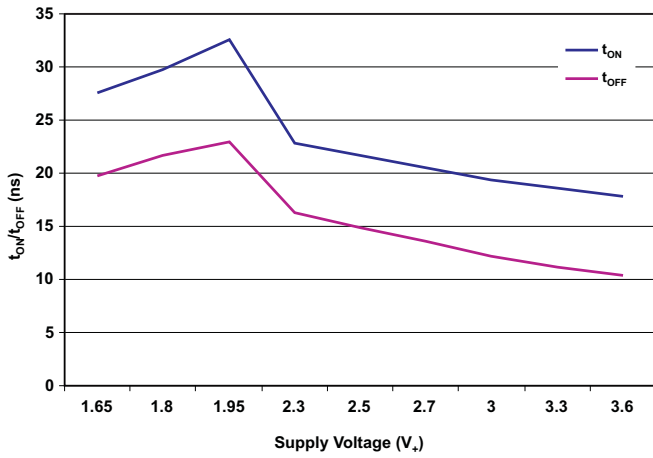


Figure 5. t_{ON} and t_{OFF} vs Supply Voltage (T_A = 25°C)

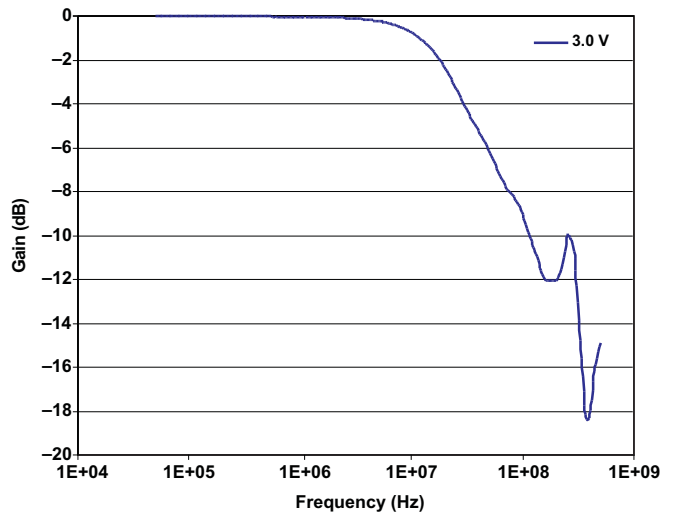


Figure 6. Bandwidth

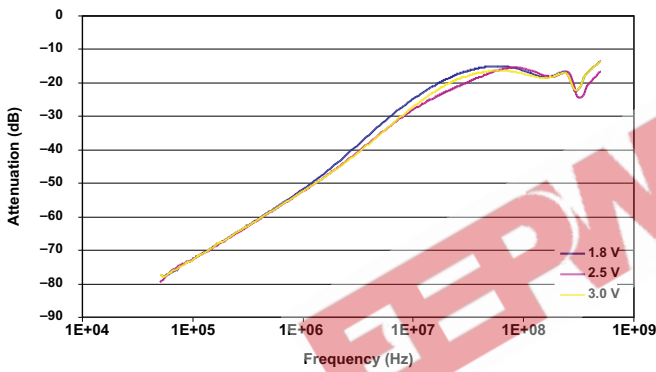


Figure 7. OFF Isolation

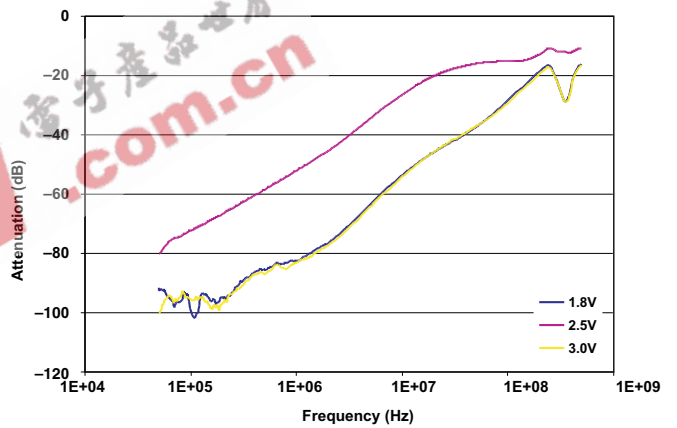


Figure 8. Crosstalk

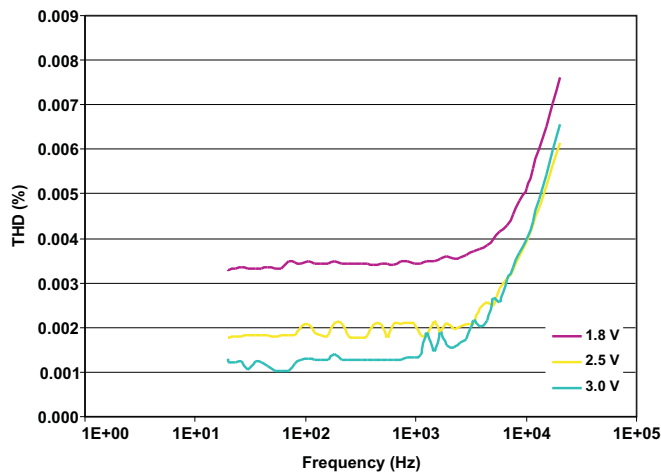


Figure 9. Total Harmonic Distortion vs Frequency

PARAMETER MEASUREMENT INFORMATION

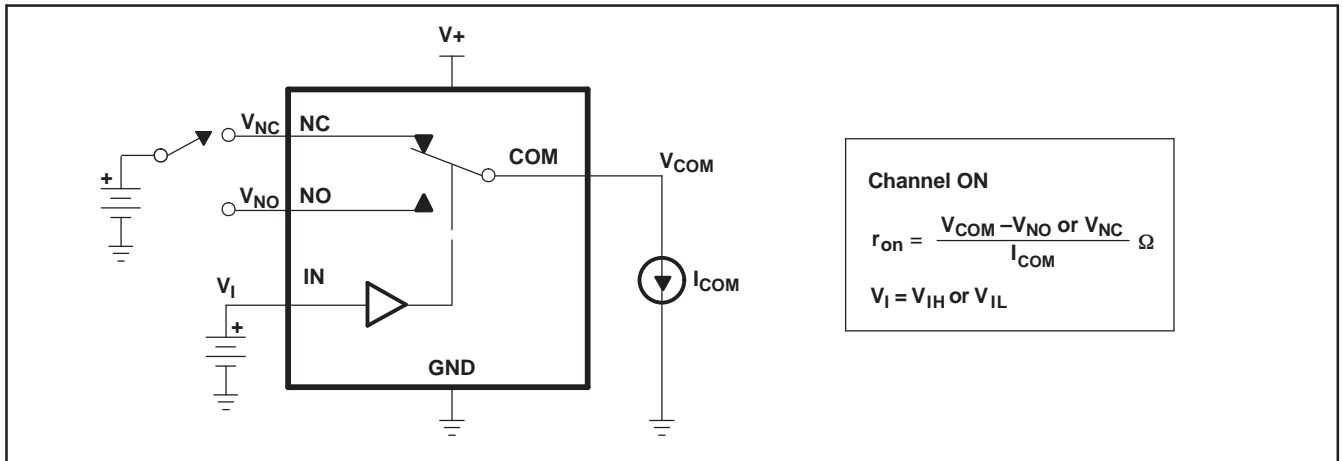


Figure 10. ON-State Resistance

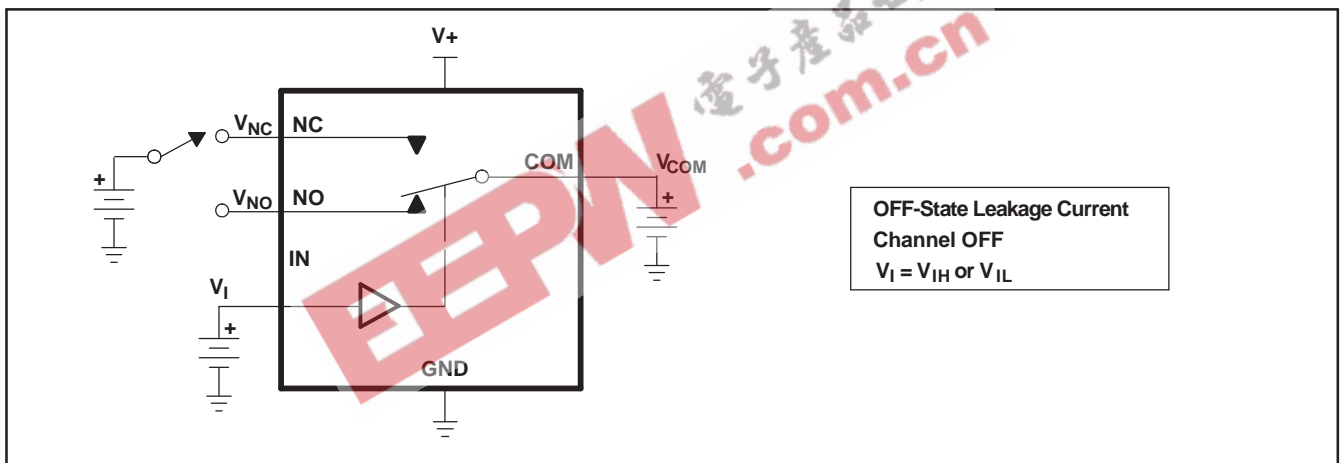


Figure 11. OFF-State Leakage Current
 ($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

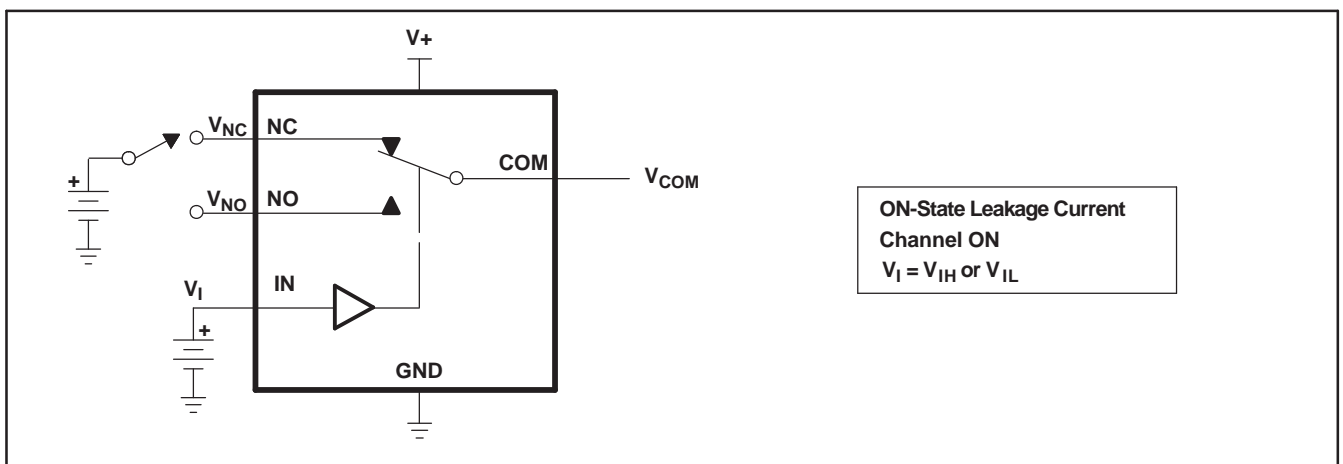


Figure 12. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

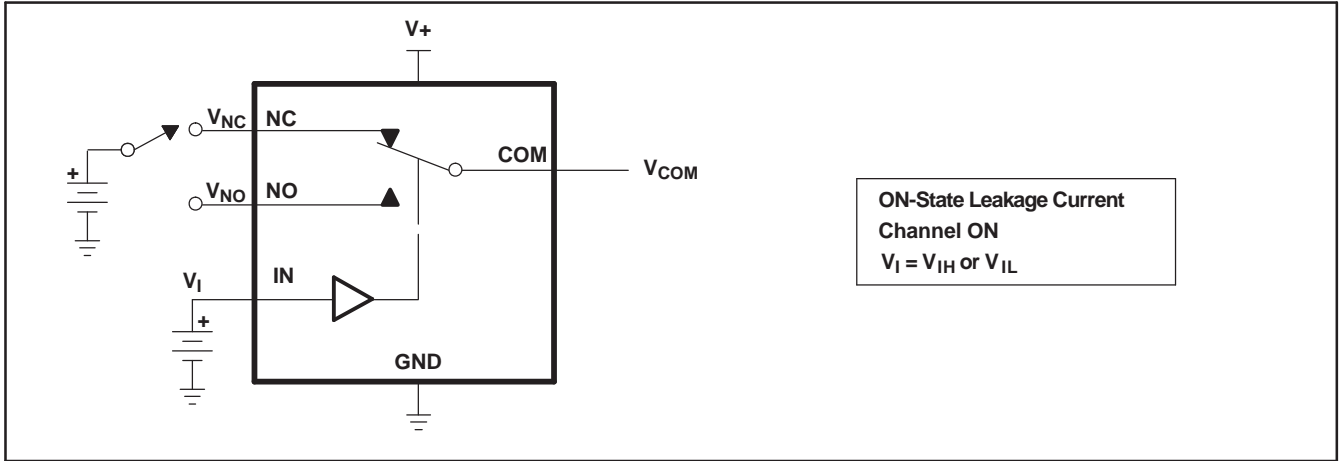
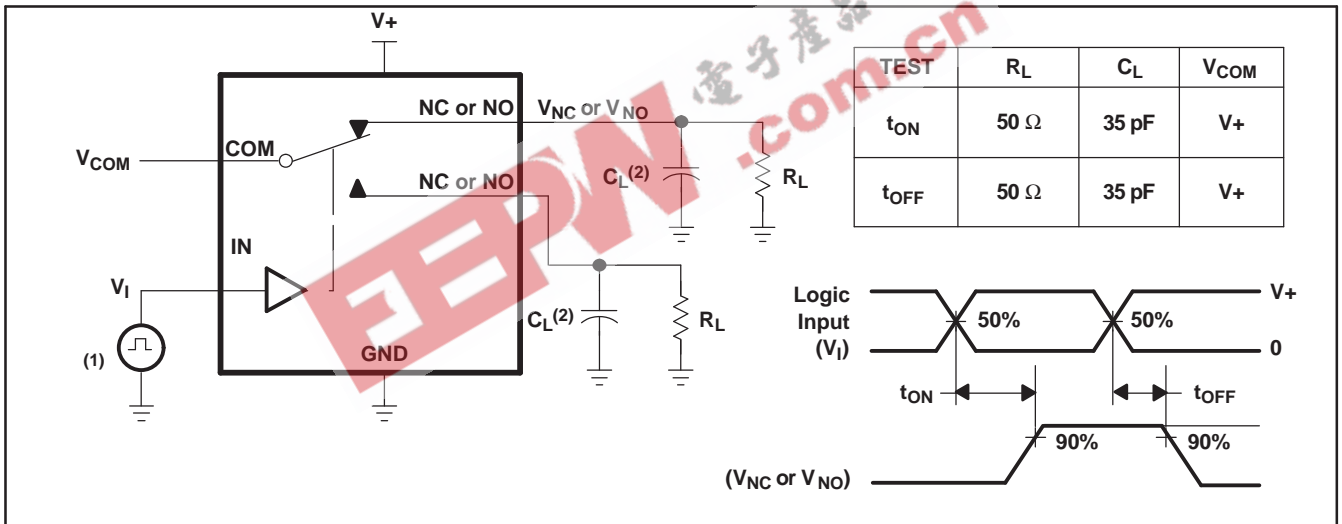


Figure 13. Capacitance (C_I , $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



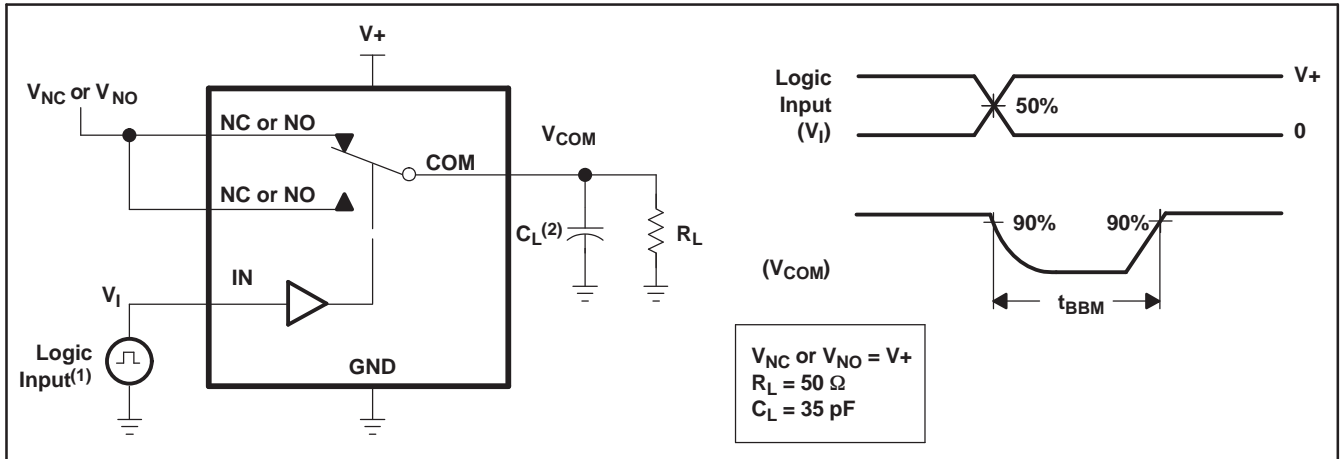
- (1) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
- (2) C_L includes probe and jig capacitance.

Figure 14. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

TS3A24159
0.3-Ω DUAL SPDT ANALOG SWITCH
DUAL-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER

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PARAMETER MEASUREMENT INFORMATION (continued)



- (1) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
- (2) C_L includes probe and jig capacitance.

Figure 15. Break-Before-Make Time (t_{BBM})

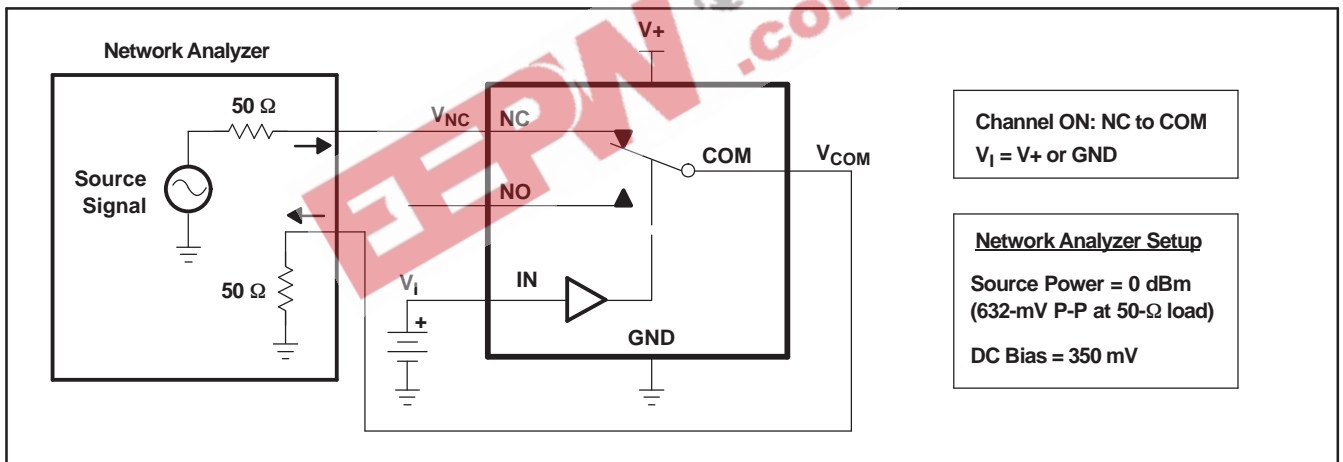


Figure 16. Bandwidth (BW)

PARAMETER MEASUREMENT INFORMATION (continued)

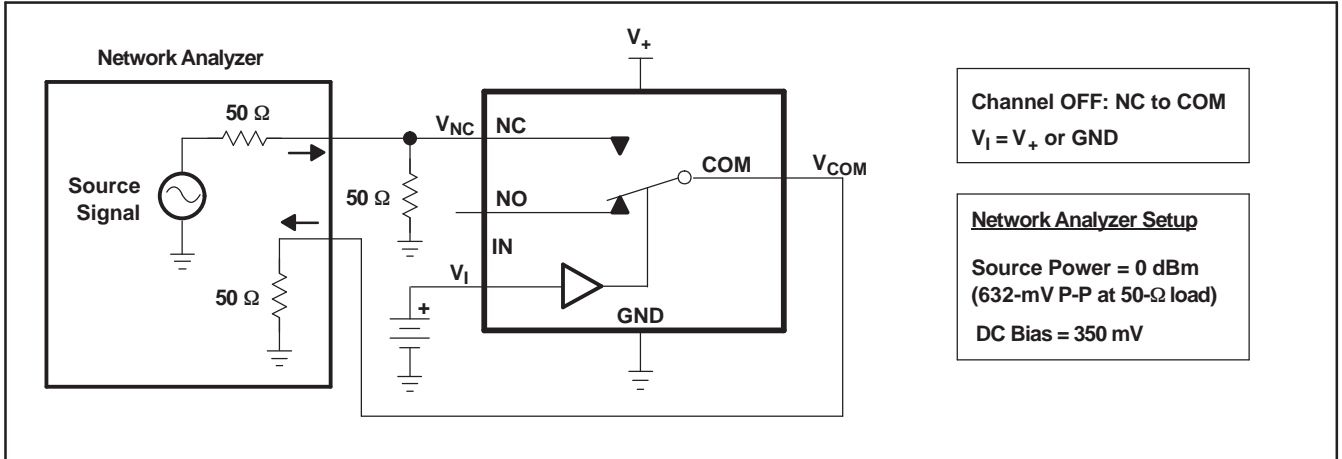


Figure 17. OFF Isolation (O_{ISO})

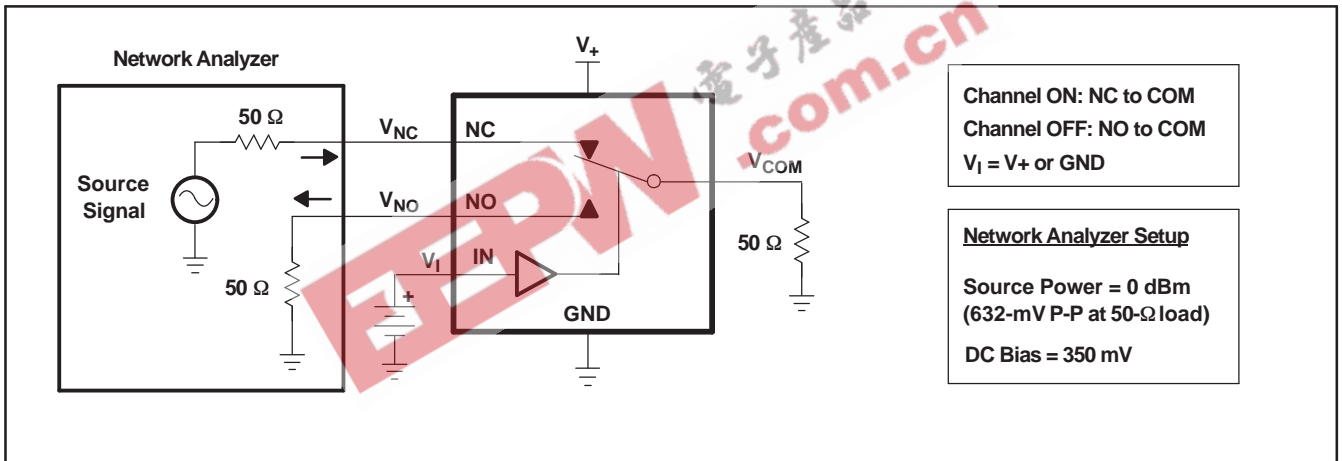
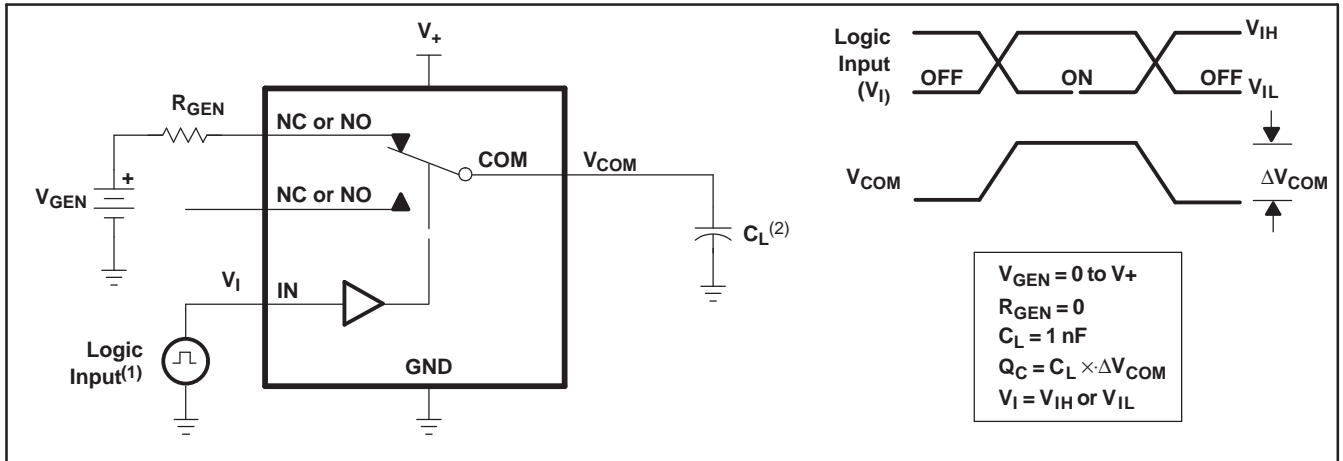


Figure 18. Crosstalk (X_{TALK})

TS3A24159
0.3-Ω DUAL SPDT ANALOG SWITCH
DUAL-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER

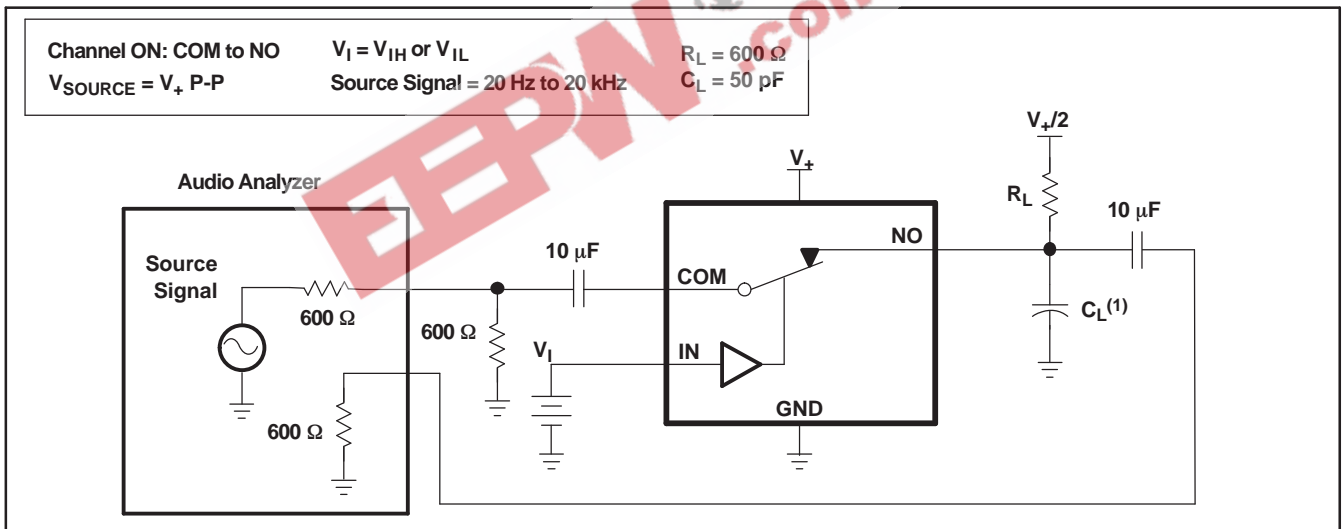
SCDS238C—MARCH 2007—REVISED FEBRUARY 2008

PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
- B. C_L includes probe and jig capacitance.

Figure 19. Charge Injection (Q_C)



- A. C_L includes probe and jig capacitance.

Figure 20. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TS3A24159DGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A24159DGSRG4	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A24159DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TS3A24159DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TS3A24159YZPR	ACTIVE	DSBGA	YZP	10	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

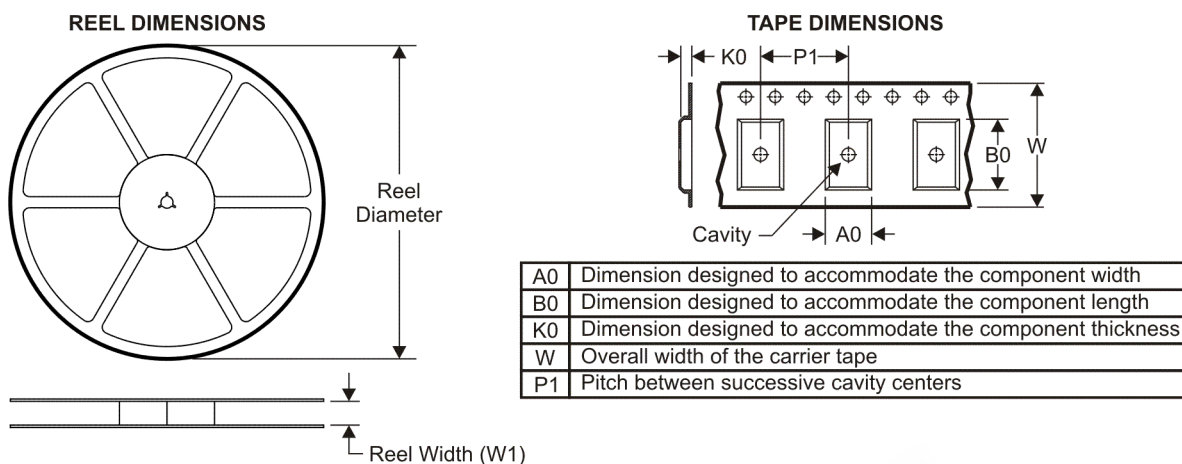
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

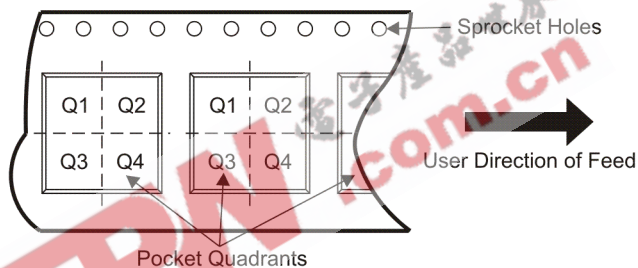
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TAPE AND REEL INFORMATION



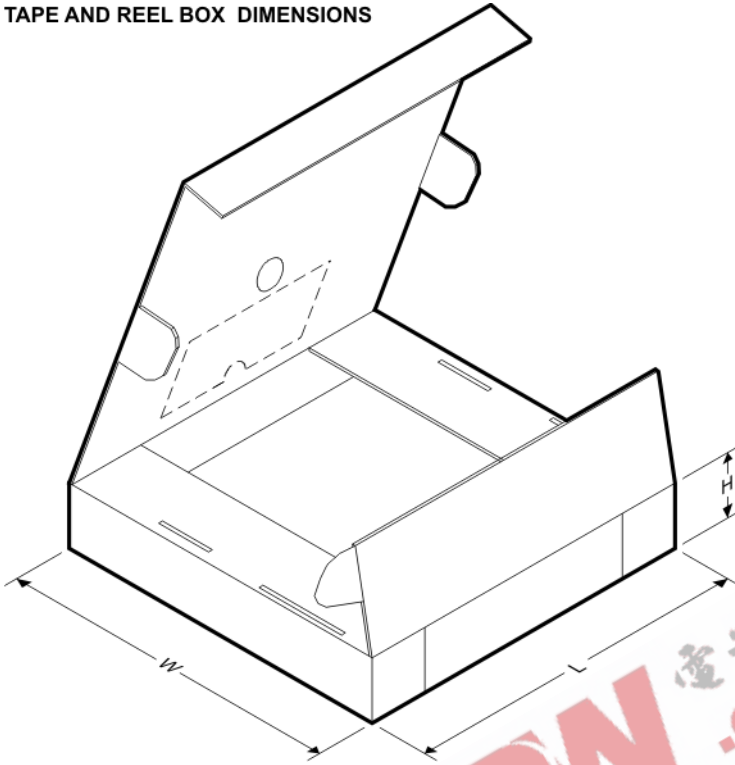
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadra
TS3A24159DGSR	MSOP	DGS	10	2500	330.0	13.0	5.3	3.4	1.4	8.0	12.0	Q1
TS3A24159DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS3A24159YZPR	DSBGA	YZP	10	3000	180.0	8.4	1.5	2.03	0.7	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



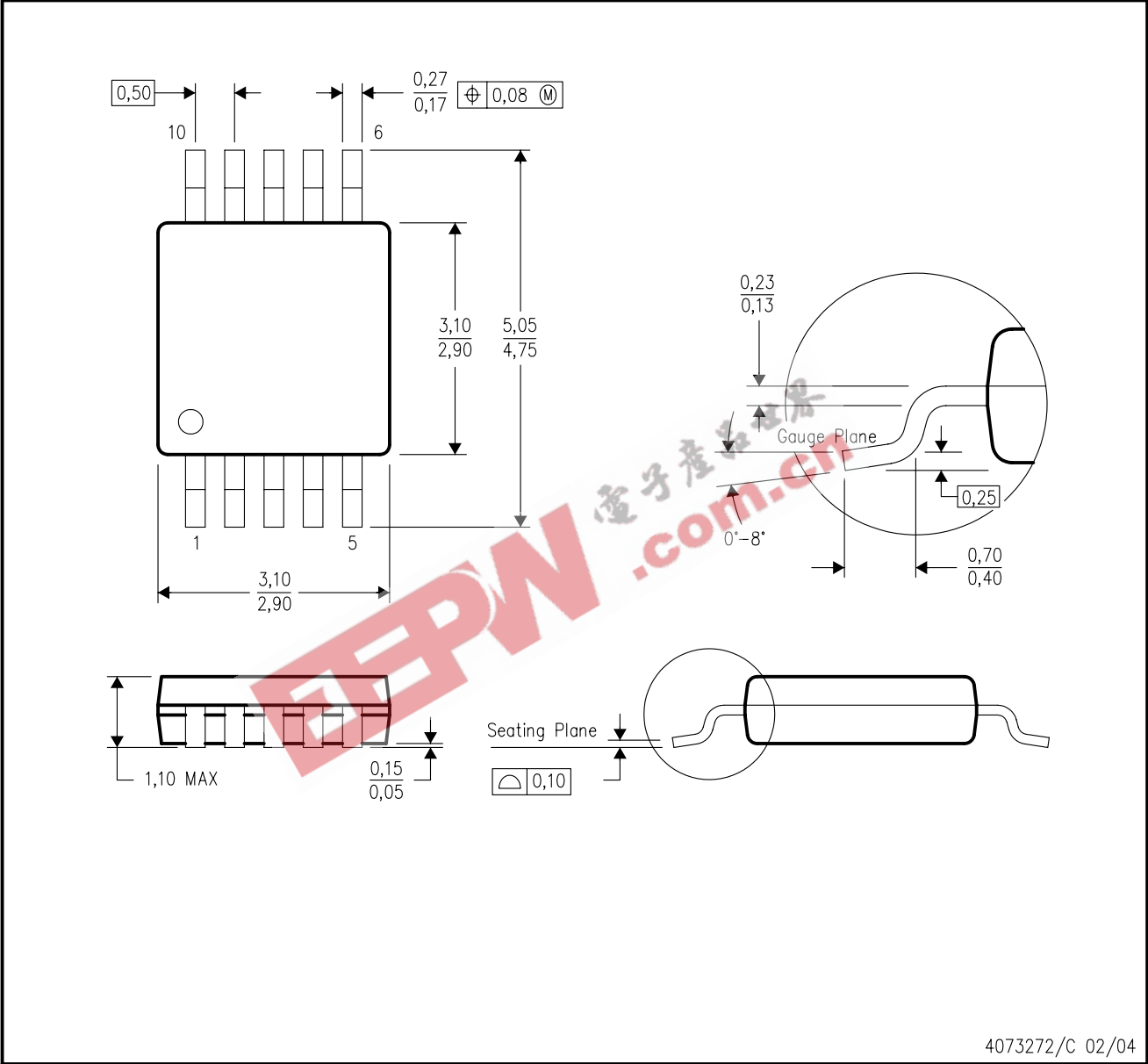
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A24159DGSR	MSOP	DGS	10	2500	358.0	335.0	35.0
TS3A24159DRCR	SON	DRC	10	3000	346.0	346.0	29.0
TS3A24159YZPR	DSBGA	YZP	10	3000	220.0	220.0	34.0

MECHANICAL DATA

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE

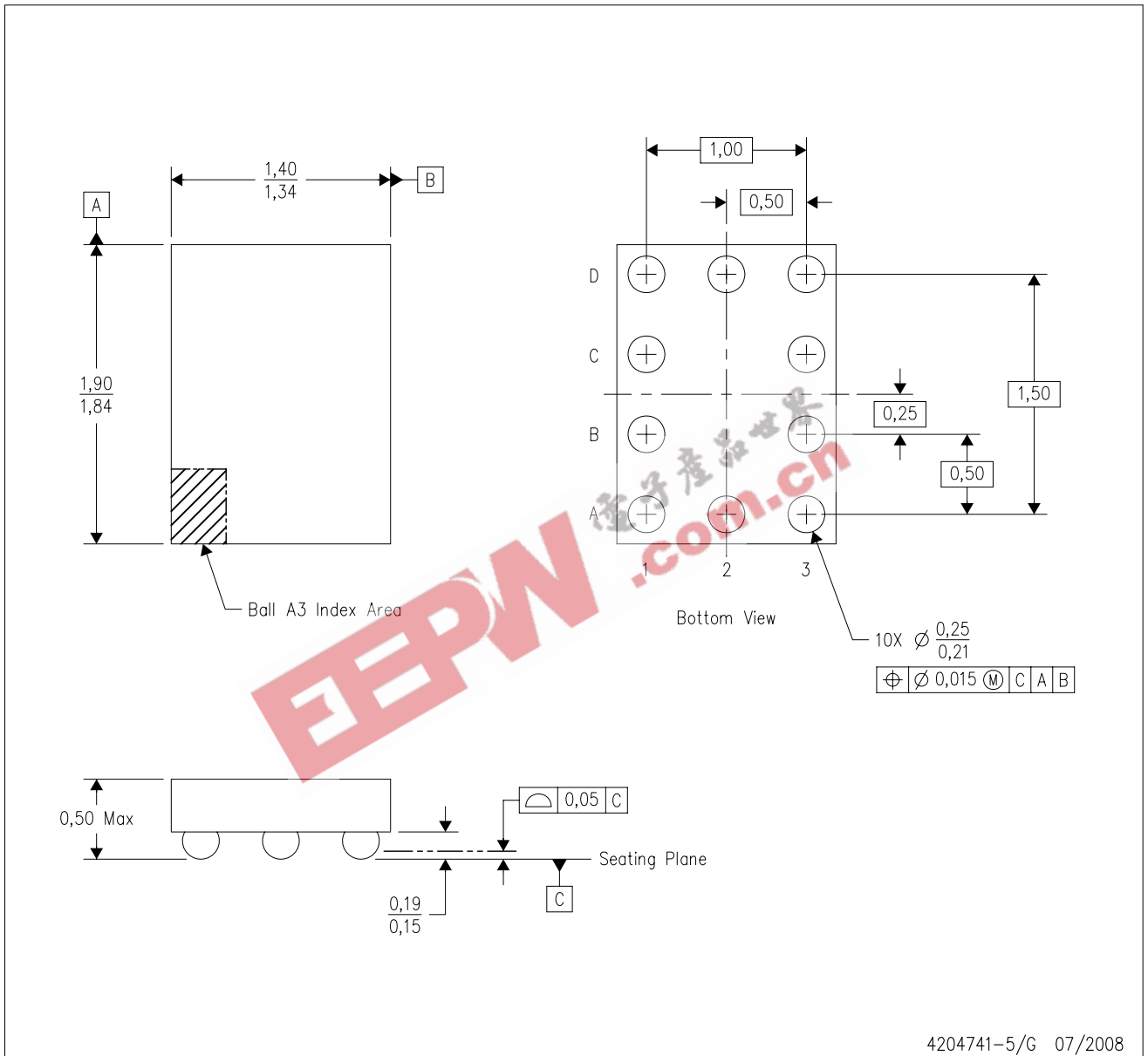


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation BA.

MECHANICAL DATA

YZP (R-XBGA-N10)

(CUSTOM) DIE-SIZE BALL GRID ARRAY



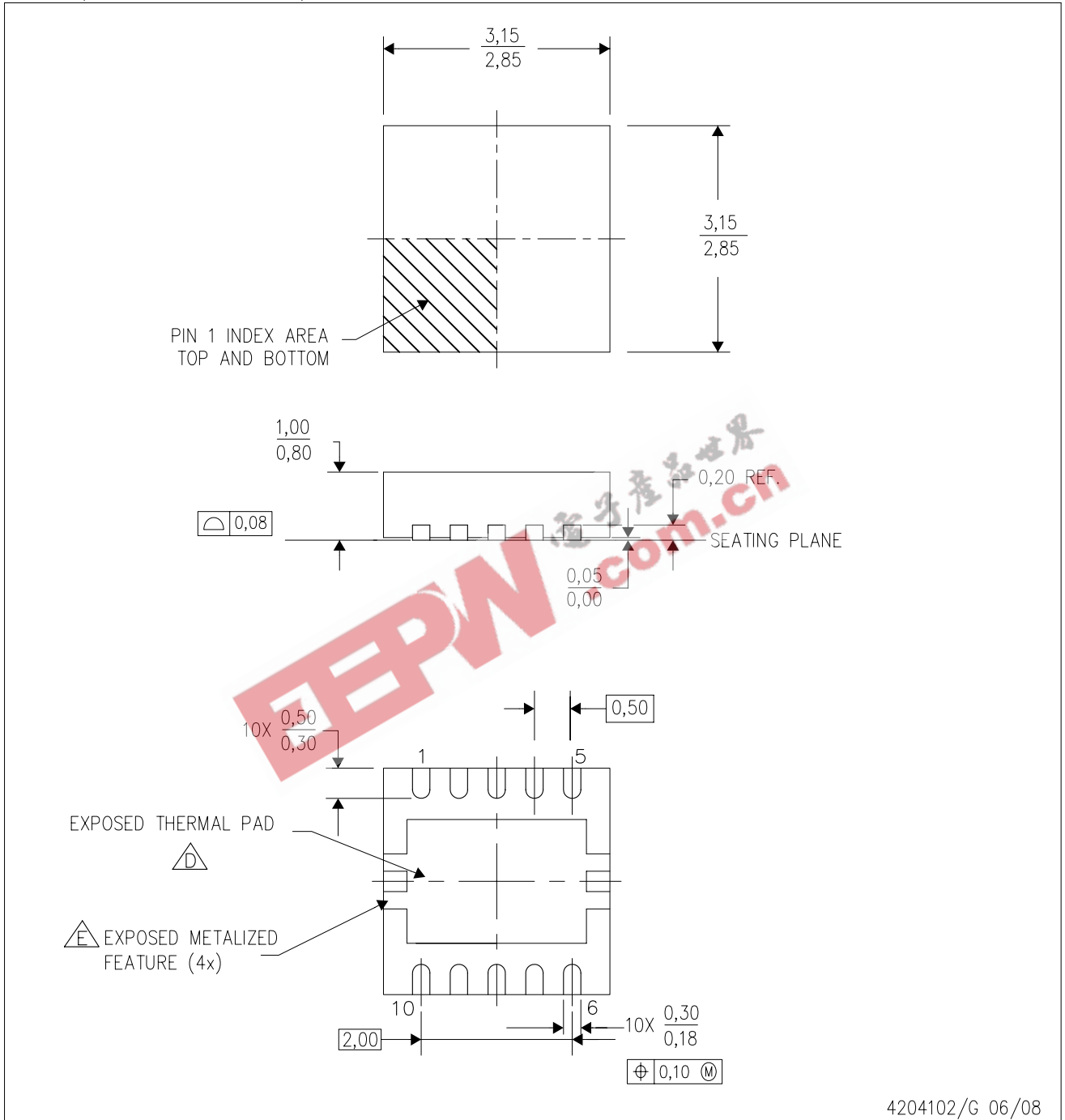
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - NanoFree™ package configuration.
 - This package is a lead-free solder ball design.

NanoFree is a trademark of Texas Instruments.

MECHANICAL DATA

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



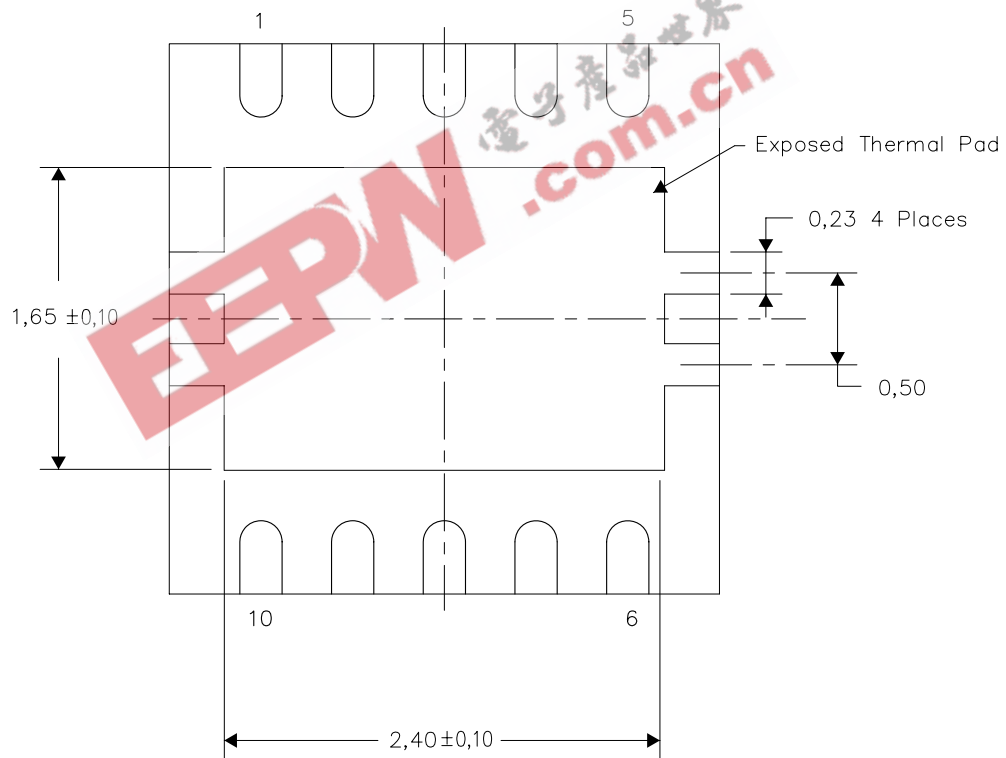
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Small Outline No-Lead (SON) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - Metalized features are supplier options and may not be on the package.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



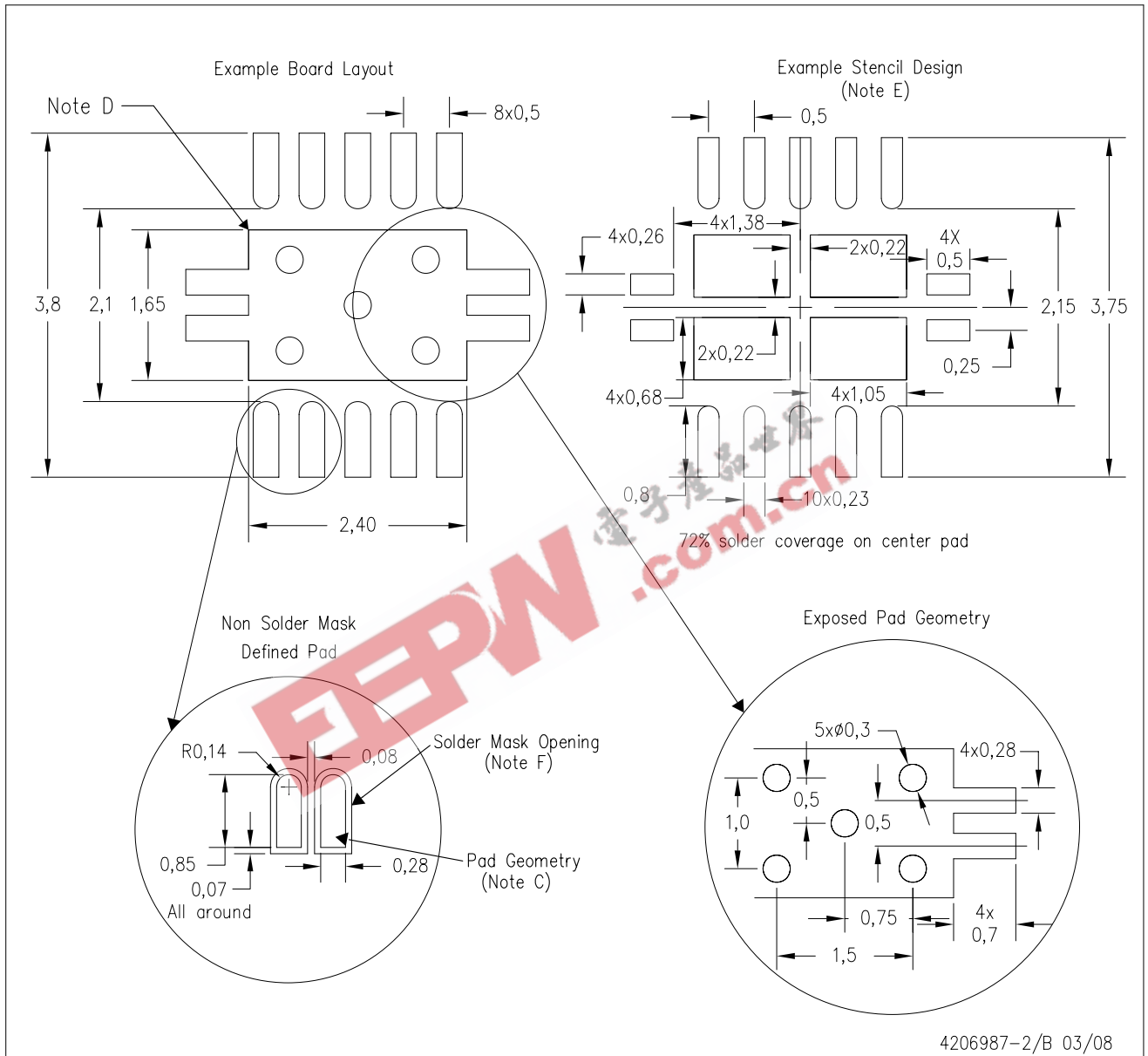
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

LAND PATTERN

DRC (S-PVSON-N10)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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