

## 74F537 1-of-10 Decoder with 3-STATE Outputs

### General Description

The 74F537 is one-of-ten decoder/demultiplexer with four active HIGH BCD inputs and ten mutually exclusive outputs. A polarity control input determines whether the outputs are active LOW or active HIGH. The 74F537 has 3-STATE outputs, and a HIGH signal on the Output Enable (OE) input forces all outputs to the high impedance state.

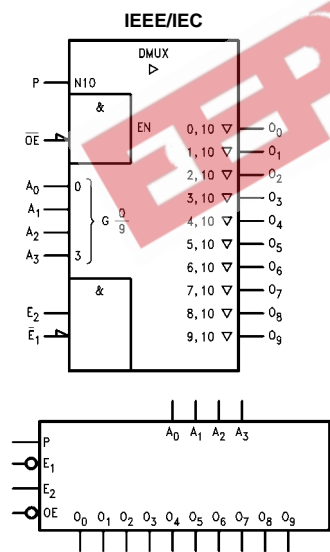
Two input enables, active HIGH  $E_2$  and active LOW  $\bar{E}_1$ , are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine cause all outputs to go to the inactive state (i.e., same polarity as the P input).

### Ordering Code:

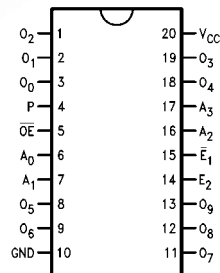
Order Number	Package Number	Package Description
74F537SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F537PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



## Unit Loading/Fan Out

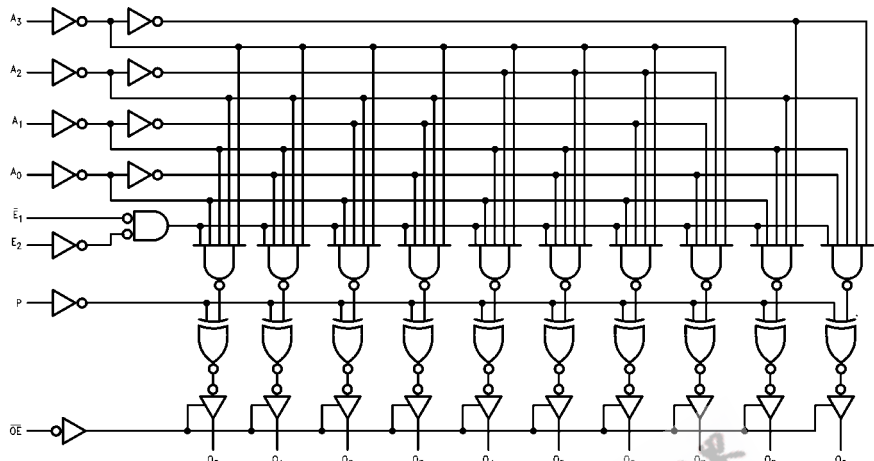
Pin Names	Description	U.L. HIGH/LOW	Input I <sub>H</sub> /I <sub>L</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
A <sub>0</sub> -A <sub>3</sub>	Address Inputs	1.0/1.0	20 μA/-0.6 mA
$\bar{E}_1$	Enable Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA
E <sub>2</sub>	Enable Input (Active HIGH)	1.0/1.0	20 μA/-0.6 mA
$\bar{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA
P	Polarity Control Input	1.0/1.0	20 μA/-0.6 mA
O <sub>0</sub> -O <sub>9</sub>	3-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

## Truth Table

Function	Inputs							Outputs										
	$\bar{OE}$	$\bar{E}_1$	E <sub>2</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	O <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>	O <sub>9</sub>	
High Impedance	H	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	
Disable	L	H	X	X	X	X	X			Outputs Equal P Input								
	L	X	L	X	X	X	X											
Active HIGH Output (P = L)	L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	
	L	L	H	L	L	L	H	L	H	L	L	L	L	L	L	L	L	
	L	L	H	L	L	H	L	L	L	H	L	L	L	L	L	L	L	
	L	L	H	L	L	H	H	L	L	L	H	L	L	L	L	L	L	
	L	L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	
	L	L	H	L	H	L	L	L	L	L	L	L	L	H	L	L	L	
	L	L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	
	L	L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	
	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L
	L	L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	L	H
	L	L	H	H	X	H	X	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	H	H	X	X	L	L	L	L	L	L	L	L	L	L	L
	Active LOW Output (P = H)	L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H
		L	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H
L		L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	
L		L	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	
L		L	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H	
L		L	H	L	H	H	L	H	H	H	H	H	L	H	H	H	H	
L		L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	
L		L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L	
L		L	H	H	X	H	X	H	H	H	H	H	H	H	H	H	H	
L		L	H	H	H	X	X	H	H	H	H	H	H	H	H	H	H	

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Absolute Maximum Ratings <sup>(Note 1)</sup>		Recommended Operating Conditions	
Storage Temperature	-65°C to +150°C	Free Air Ambient Temperature	0°C to +70°C
Ambient Temperature under Bias	-55°C to +125°C	Supply Voltage	+4.5V to +5.5V
Junction Temperature under Bias	-55°C to +150°C		
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V		
Input Voltage (Note 2)	-0.5V to +7.0V		
Input Current (Note 2)	-30 mA to +5.0 mA		
Voltage Applied to Output			
in HIGH State (with V <sub>CC</sub> = 0V)			
Standard Output	-0.5V to V <sub>CC</sub>		
3-STATE Output	-0.5V to +5.5V		
Current Applied to Output			
in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)		

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

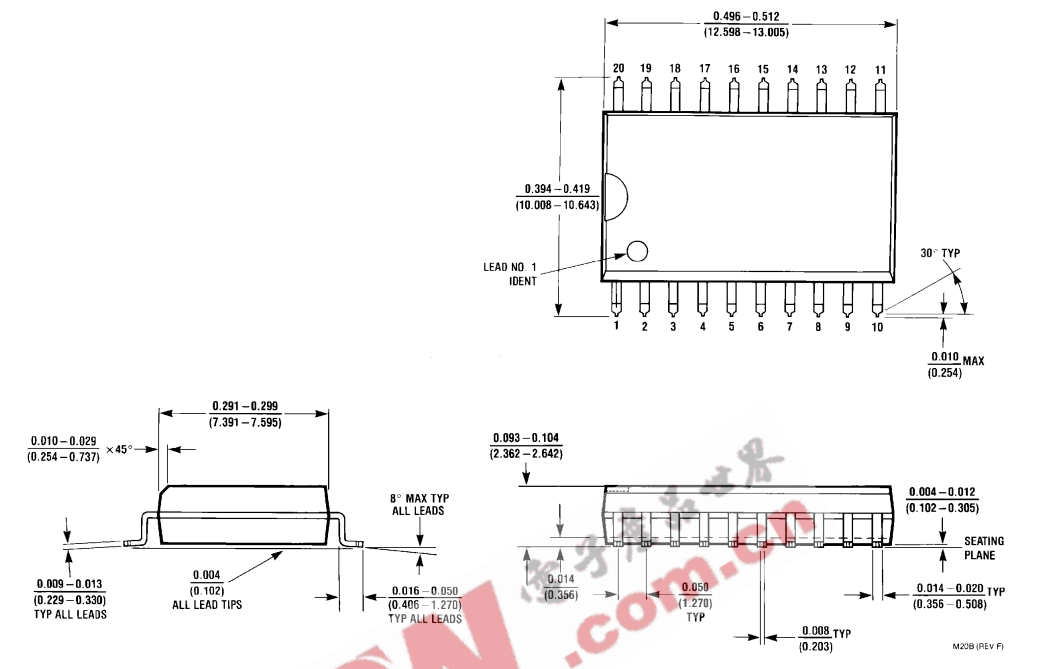
**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

### DC Electrical Characteristics

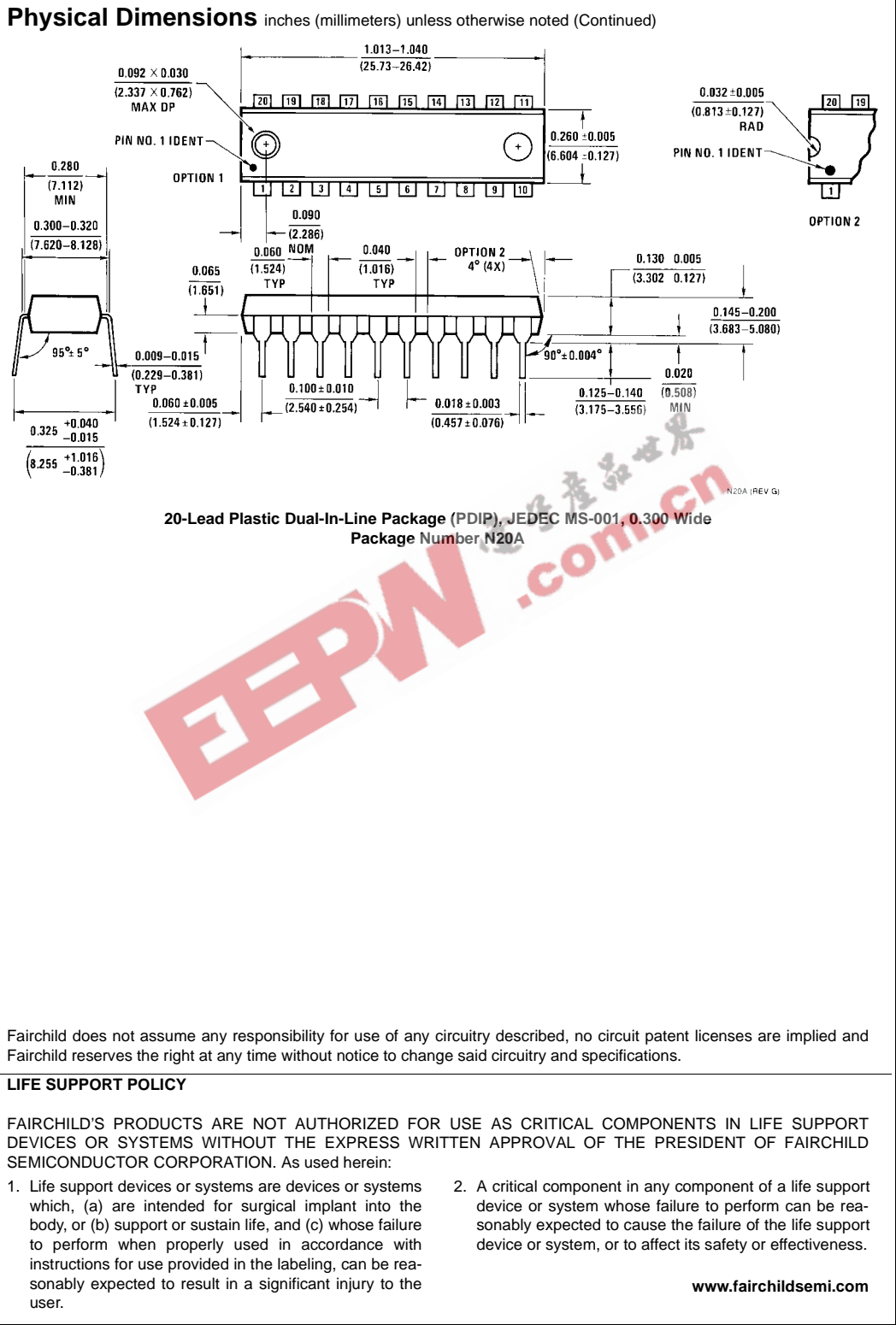
Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 2.5 10% V <sub>CC</sub> 2.4 5% V <sub>CC</sub> 2.7 5% V <sub>CC</sub> 2.7			V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current			56	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCZ</sub>	Power Supply Current		44	66	mA	Max	V <sub>O</sub> = HIGH Z

AC Electrical Characteristics							
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	6.0	11.0	16.0	6.0	17.0	ns
t <sub>PHL</sub>	A <sub>n</sub> to O <sub>n</sub>	4.0	7.5	11.0	4.0	12.0	
t <sub>PLH</sub>	Propagation Delay	5.0	8.5	14.5	5.0	15.5	ns
t <sub>PHL</sub>	$\overline{E}_1$ to O <sub>n</sub>	4.0	6.5	9.0	4.0	10.0	
t <sub>PLH</sub>	Propagation Delay	6.0	11.0	16.0	6.0	17.0	ns
t <sub>PHL</sub>	E <sub>2</sub> to O <sub>n</sub>	5.0	10.0	14.0	5.0	15.0	
t <sub>PLH</sub>	Propagation Delay	6.0	11.5	18.0	6.0	20.0	ns
t <sub>PHL</sub>	P to O <sub>n</sub>	6.0	11.0	16.0	6.0	17.0	
t <sub>PZH</sub>	Output Enable Time	3.0	5.5	10.5	3.0	11.5	ns
t <sub>PZL</sub>	$\overline{OE}$ to O <sub>n</sub>	5.0	9.0	13.0	5.0	14.0	
t <sub>PHZ</sub>	Output Disable Time	2.0	4.0	6.0	2.0	7.0	ns
t <sub>PLZ</sub>	$\overline{OE}$ to O <sub>n</sub>	3.0	5.0	7.0	3.0	8.0	

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M20B**



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