DATA SHEET

74ALVT162731

2.5V/3.3V 1-to-4 address register/driver with 30Ω termination resistors (3-State)

Product specification
IC24 Data Handbook

1999 Mar 23

Philips
Semiconductors

PHILIPS

2.5V/3.3V 1-to-4 address register/driver with 30Ω termination resistors (3-State)

74ALVT162731

FEATURES

- 5V I/O Compatible
- 3-State outputs
- Output capability: +12 mA/-12 mA
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Positive edge triggered registers
- Latch-up protection exceeds 500 mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per machine model
- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ALVT162731 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V to 3.3V with I/O compatibility up to 5V.

This device is a 1-to-4 address register/driver featuring non-inverting 3-State outputs. The state of the outputs are controlled by two enable inputs (OE1 and OE2). Each enable input controls the state of two of the four common outputs for each input. When an OEn input is a logic High, the respective outputs will be in the high impedance state. When an OEn input is a logic Low, the respective outputs are active. The device can be configured for a transparent mode from input to output or a register mode by the SEL input. When SEL is a logic High the device is configured for transparent mode and when SEL is a logic Low it is configured for register mode. While in the register mode the output follows the input on the rising edge of the CLK input. The function of the data registers is not effected by either SEL or OEn.

The 74ALVT162731 is designed with 30Ω series resistance in both the HIGH and LOW states of the output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF	3.8	3.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or V_{CC}	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	60	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVT162731 DL	AV162731 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVT162731 DGG	AV162731 DGG	SOT364-1

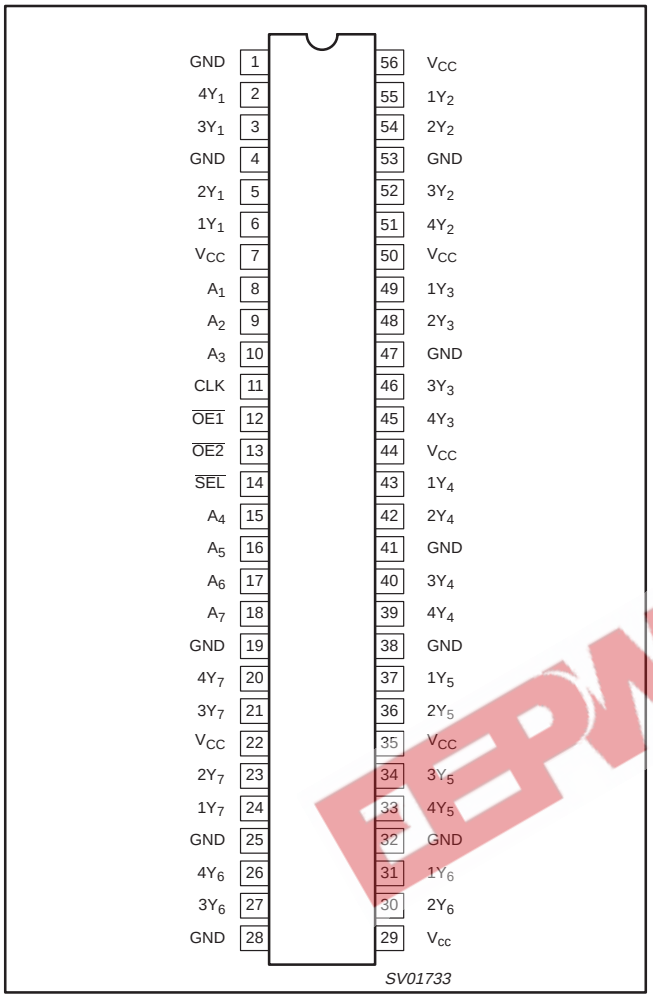
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 19, 25, 28, 32, 38, 41, 47, 53	GND	Ground
5, 6, 23, 24, 30, 31, 36, 37, 42, 43, 48, 49, 54, 55	$1Y_n$, $2Y_n$	Output, controlled by OE1
2, 3, 20, 21, 26, 27, 33, 34, 39, 40, 45, 46, 51, 52	$3Y_n$,$4Y_n$	Output, controlled by OE2
7, 22, 29, 35, 44, 50, 56	V_{CC}	Positive power supply
8, 9, 10, 15, 16, 17, 18	A_n	Data inputs
14	SEL	Select input, controls mode of device
11	CLK	Clock input
12, 13	OE_n	Output enable

2.5V/3.3V 1-to-4 address register/driver with 30Ω termination resistors (3-State)

74ALVT162731

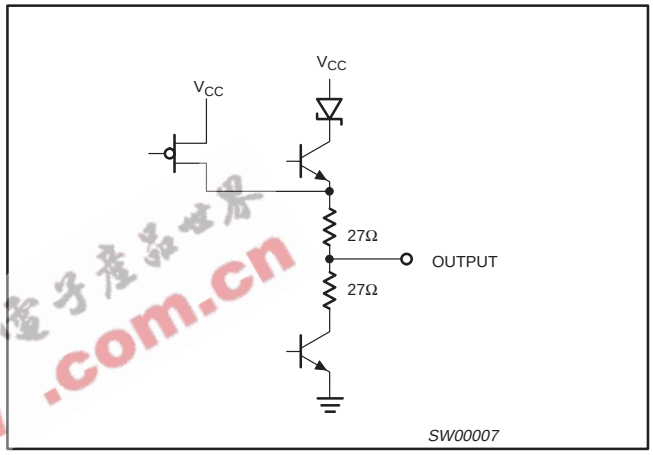
PIN CONFIGURATION



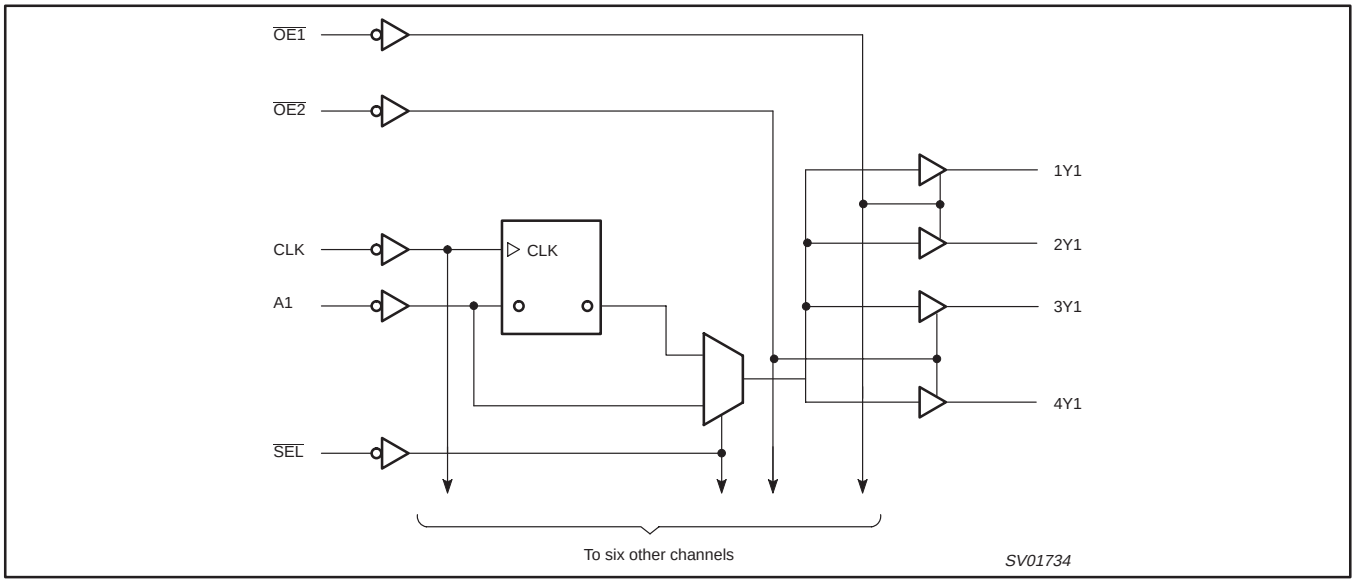
FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{OE}$	$\overline{SEL}$	CLK	A	$\overline{Y}$
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

SCHEMATIC OF EACH OUTPUT



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage[3]		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		–8		–12	mA
I_{OL}	Low-level output current		8		12	mA
$\Delta\tau/\Delta\varpi$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ±0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 3.0V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = –12mA		2.0	2.5		V
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA			0.5	0.8	V
V_{RST}	Power-up output low voltage[6]	V_{CC} = 3.6V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.5	1	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.05	0.1	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			7.0	9.0	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O=0[5]			0.06	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	3.2 2.7	5.0 4.0	ns
t_{PLH} t_{PHL}	Propagation delay CLK to nYx	3	1.5 1.5	4.0 3.8	6.3 5.4	ns
t_{PLH} t_{PHL}	Propagation delay SEL to nYx	1	1.5 1.5	4.3 3.7	6.2 5.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	4.2 3.4	7.0 4.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	3.9 3.2	6.0 4.9	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (3.3V ±0.3V RANGE)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 3.3V ±0.3V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low Ax to nYx	4	1.5 1.5	1.1 0.6	ns
th(H) th(L)	Hold time, High or Low Ax to nYx	4	0 0	–0.5 –0.9	ns
tw(H) tw(L)	Pulse width, High or Low CLK	3	1.5 1.5		ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

DC ELECTRICAL CHARACTERISTICS (2.5V ±0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.3V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.3V; I_{OH} = –8mA		1.7	2.1		V
V_{OL}	Low-level output voltage	V_{CC} = 2.3V; I_{OL} = 12mA			0.5	0.7	V
V_{RST}	Power-up output low voltage[7]	V_{CC} = 2.7V; I_O = 1mA; V_I = V_{CC} or GND				0.55	V
I_I	Input leakage current	V_{CC} = 2.7V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 2.7V; V_I = 5.5V			0.1	10	
		V_{CC} = 2.7V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 2.7V; V_I = 0			0.1	-5	
I_{OFF}	Off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current Data inputs[6]	V_{CC} = 2.3V; V_I = 0.7V			90		µA
		V_{CC} = 2.3V; V_I = 1.7V			–10		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 2.3V			10	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC} $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 2.7V; V_O = 2.3V; V_I = V_{IL} or V_{IH}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 2.7V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			0.5	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 2.7V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.04	0.1	mA
I_{CCL}		V_{CC} = 2.7V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			5.0	7.0	
I_{CCZ}		V_{CC} = 2.7V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.04	0.1	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 2.3V to 2.7V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.04	0.4	mA

NOTES:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Not guaranteed.
7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS (2.5V ±0.2V RANGE)

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	3.8 3.1	5.7 4.5	ns
t_{PLH} t_{PHL}	Propagation delay CLK to nYx	3	2.2 2.2	4.8 4.1	7.3 6.2	ns
t_{PLH} t_{PHL}	Propagation delay SEL to nYx	1	2.0 2.0	5.5 3.9	8.7 6.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	2.0 2.0	5.8 4.1	9.0 6.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	5.0 4.1	7.6 6.3	ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS (2.5V ±0.2V RANGE)

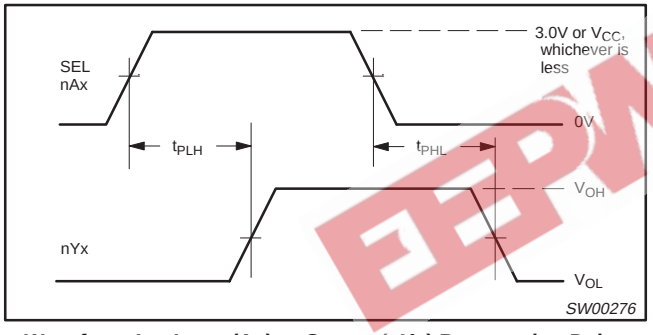
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V_{CC} = 2.5V ±0.2V		
			MIN	TYP[1]	
ts(H) ts(L)	Setup time, High or Low nYx to CLK	4	2.4 2.3	1.4 0.9	ns
th(H) th(L)	Hold time, High or Low nYx to CLK	4	0 0	–0.7 –1.0	ns
tw(H) tw(L)	Pulse width, High or Low CLK	3	1.5 1.5		ns

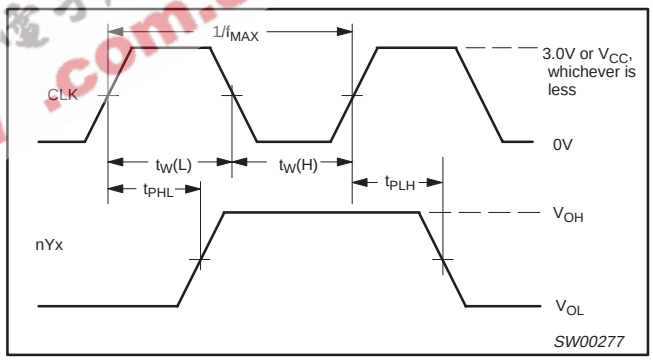
NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC WAVEFORMS

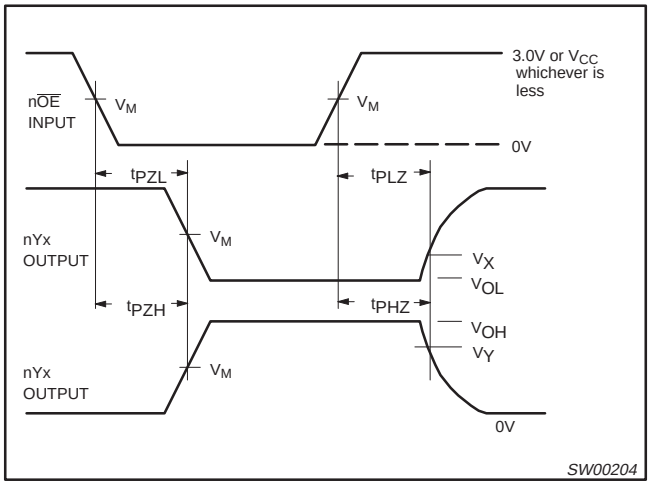
NOTES:
1. V_M = 1.5V at $V_{CC} \geq$ 3.0V, $V_M = V_{CC}/2$ at $V_{CC} \leq$ 2.7V
2. $V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 3.0V, $V_X = V_{OL}$ + 0.150V at $V_{CC} \leq$ 2.7V
3. $V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 3.0V, $V_Y = V_{OH}$ – 0.150V at $V_{CC} \leq$ 2.7V



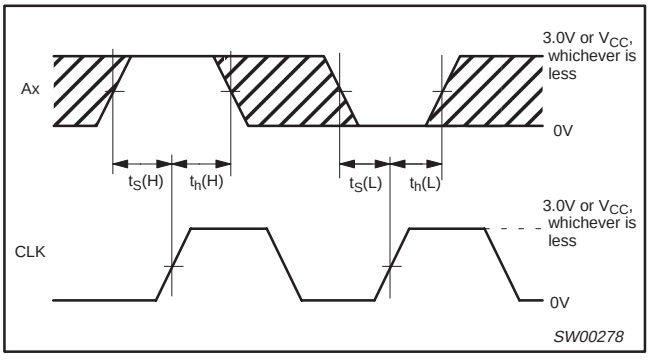
Waveform 1. Input (Ax) to Output (nYx) Propagation Delay, transparent mode. SEL to OUtput (nYx) Propagation Delay



Waveform 3. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

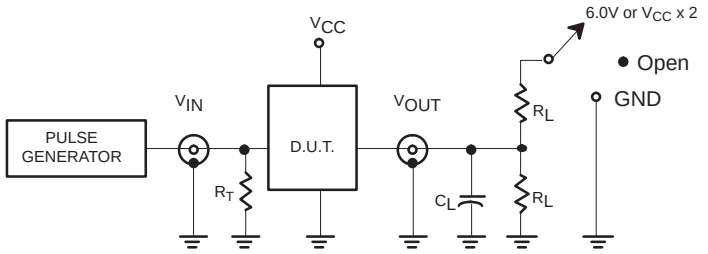


Waveform 2. 3-State Output Enable and Disable Times

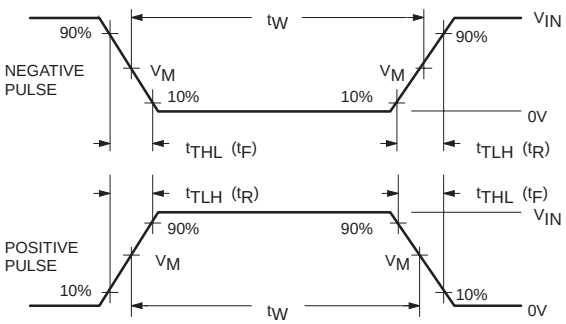


Waveform 4. Data setup and hold times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or V_{CC} x 2
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

DEFINITIONS

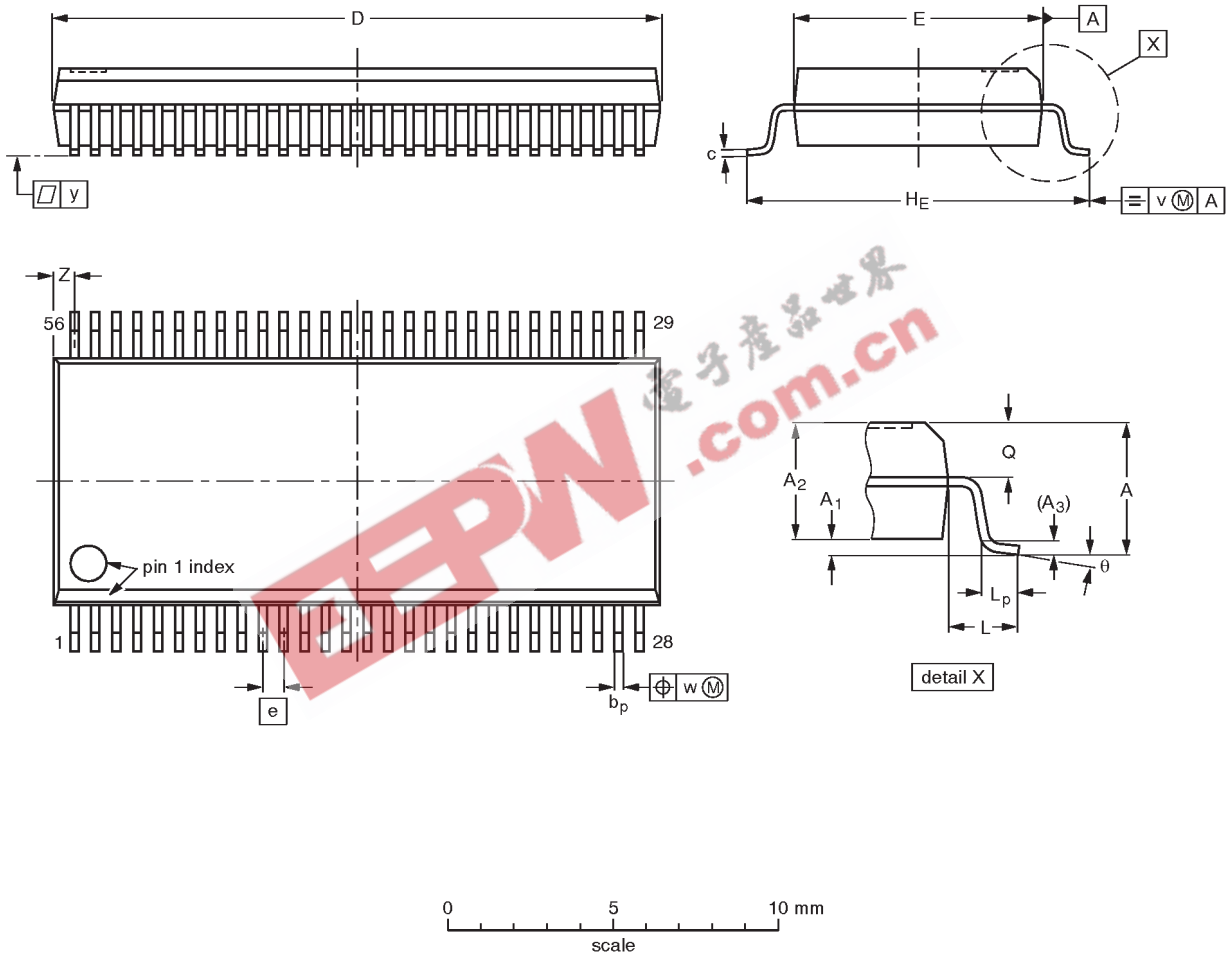
R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00025

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

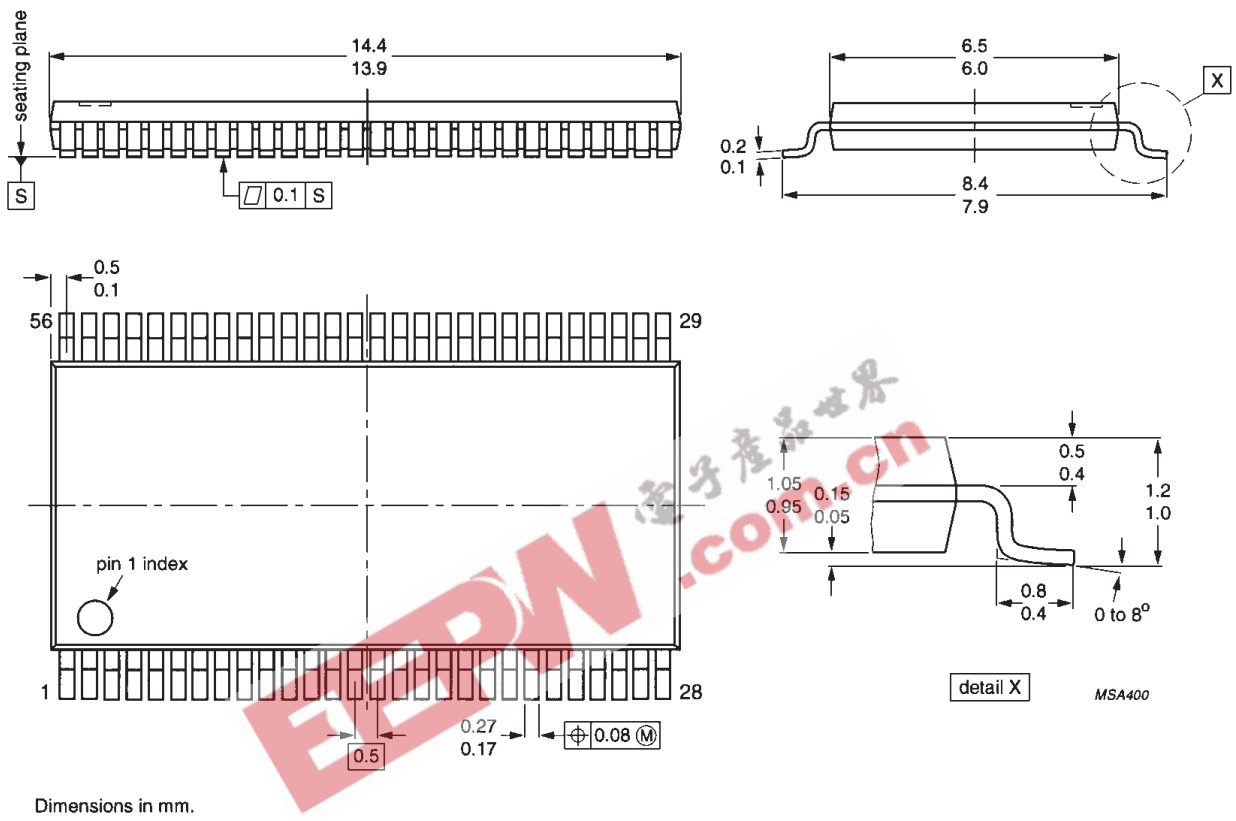
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



Dimensions in mm.

2.5 V/3.3 V 1-to-4 address register/driver with 30Ω termination resistors (3-State)

74ALVT162731

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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