ANALOG DEVICES

2 Pair/1 Pair ETSI Compatible HDSL Analog Front End

AD6472

FEATURES

Integrated Front End for Single Pair or Two Pair HDSL Systems

Meets ETSI Specifications

Supports 1168 Kbps and 2.32 Mbps

Transmit and Receive Signal Path Functions Receive Hybrid Amplifier, PGA and ADC Transmit DAC, Filter and Differential Outputs Programmable Filters

Control and Ancillary Functions

Timing Recovery DAC

Normal Loopback and Low Power Modes

Simple Interface-to-Digital Transceivers

Single 5 V Power Supply

Power Consumption: 320 mW—(Excluding Driver) Package: 80-Lead MQFP

Operating Temperature: -40°C to +85°C

GENERAL DESCRIPTION

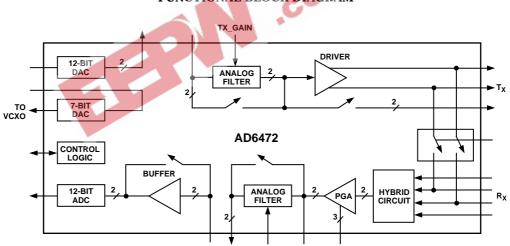
The AD6472 is a single chip analog front end for two pair or single pair HDSL applications that use 1168 Kbps or 2.32 Mbps data rates.

The AD6472 integrates all the transmit and receive functional blocks together with the timing recovery DAC.

The digital interface is designed to support industry standard digital transceivers.

While providing the full analog front end for ETSI standards (two pair or single pair HDSL applications) the AD6472 supports other applications because the architecture allows for bypassing the functional blocks.

The normal, low power, and loopback modes and the digital interface combine to make the AD6472 simple to integrate into systems.



FUNCTIONAL BLOCK DIAGRAM

REV.0

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AD6472—SPECIFICATIONS (T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Тур	Max	Units	Condition
TRANSMIT CHANNEL					
SNR THD	68 66	71 71		dB dB	The complete transmit path spectrum and pulse shape comply with ETSI requirements.
TRANSMIT DAC Clock Frequency Resolution Update Rate Output Voltage		12 2	18.688 1168	MHz Bits kHz V p-p Diff	The transmit DAC maximum update rate is half the maximum output data rate, i.e., 1168 kHz. The maximum transmit clock is 16 × 1168 = 18.688 MHz.
TRANSMIT FILTER Corner Frequency (3 dB) ¹ Accuracy Gain		320 535 ±5 9.53 3.53	±10	kHz kHz % dB dB	MODE_SEL1 = 0 MODE_SEL1 = 1
LINE DRIVER VCM Output Power Output Voltage		2.5 13.5 6		V dBm V p-p Diff	Transformer Turns Ratio = 1:2.3 at 50 kHz When Loaded by ETSI (RTR/TM3036) HDSL Test Loops
TRANSMIT VOLTAGE LEVEL		6 3		V p-p Diff V p-p Diff	$TX_GAIN = 0$ $TX_GAIN = 1$
RECEIVE CHANNEL SNR THD	68 66	71 71		dB dB	cn
HYBRID INTERFACE Input Voltage Range Input Impedance		10	5	V p-p Diff kΩ	$V_{\rm CM}$ = 2.5 V. See Figure 3
PROGRAMMABLE GAIN AMPLIFIER Overall Gain Accuracy Gain Step Gain Step Accuracy		±1 3 ±0.25		dB dB dB	Condition –6 dB to +9 dB
RECEIVE FILTER Corner Frequency (-3 dB) ¹ Accuracy		$320 \\ 640 \\ \pm 5$	±10	kHz kHz %	MODE_SEL1 = 0 MODE_SEL1 = 1
TIMING RECOVERY DAC Resolution Output Low Output High	7	0.5 4.5		Bits V V	Guaranteed Monotonic
$\begin{array}{c} \textbf{DIGITAL INTERFACE} \\ \textbf{Input Logic High, V_{IH}} \\ \textbf{Input Logic Low, V_{IL}} \\ \textbf{Output Logic High, V_{OH}} \\ \textbf{Output Logic Low, V_{OL}} \\ \textbf{Input Logic High, V_{IH}} \\ \textbf{Input Logic Low, V_{IL}} \\ \textbf{Output Logic Low, V_{IL}} \\ \textbf{Output Logic High, V_{OH}} \end{array}$	3.3 V _{DD} - 0.3 2.0 V _{DD} - 0.3		0.8 0.4 0.2	V V V V V V V V	5 V Supply, $V_{\rm MIN}$ to $V_{\rm MAX}$ 3.3 V Supply, $V_{\rm MIN}$ to $V_{\rm MAX}$
POWER SUPPLY VOLTAGE	4.75 3.15	5 3.3	5.25 3.45	V V	V _{MIN} to V _{MAX} 5 V Supply 3.3 V Supply
POWER SUPPLY CURRENT Normal Mode, Excl. Driver OVRSAMP Mode Line Driver Low Power Mode		65 73 50 17		mA mA mA mA	V_{MIN} to V_{MAX} , T_{MIN} to T_{MAX} 5 V Supply, MODE_SEL1 = 0 5 V Supply, MODE_SEL1 = 1, MODE_SEL0 = 1 With 50 Ω Differential Load
OPERATING TEMPERATURE RANGE	-40		+85	°C	T _{MIN} to T _{MAX}

NOTES ¹The ADC clock period t(1÷ f) is used for the dynamic tuning of the Tx and Rx filters.

Specifications subject to change without notice.

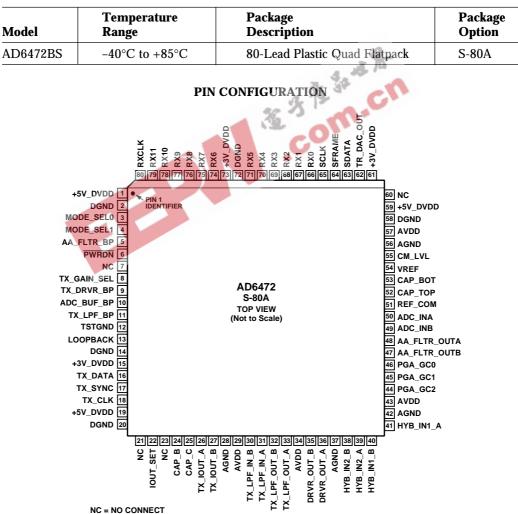
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage0.3 V to +6.0 V
Input Voltage
Output Voltage Swing $\dots \dots \dots$
Operating Temperature Range (Ambient)40°C to +85°C
Storage Temperature Range
Lead Temperature (5 sec) MQFP+280°C

*Stresses above those listed in this section may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions above those in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

80-Lead Plastic Quad Flatpack Package $\dots \dots \theta_{JA} = 45^{\circ}C/W$



ORDERING GUIDE

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6472 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS

1 +5 V_DyDD +5 V_Digital Supply. 41 HYB_INL_A Hybrid Inverting Input. 2 DGND Digital Ground. 42 AGND Analog Ground. 4 MODE_SELD Bit Rate—Filter Corner Select. 43 AVDD +5 V Analog Supply. 5 AA_FLTR_BP Antialisaing Filter Bypass. 46 PGA_GC1 PGA Gain Select Bits. 6 FWRDN Power-Down Active Low. 46 PGA_GC1 PGA Gain Select Bits. 9 TX_GAIN SEL Transmit Attenuation (6 dB) Select. 47 AA_FLTR_OUTB Differential Output of the Antialiasing Filter. 10 ADC_BUF_BP ADC Buffer Bypass. 49 ADC_INB Differential Input to the ADC. 11 TX_LPF_BP Transmit Filter Bypass. 49 ADC_INB Differential Input to the ADC. 12 TSTGND Factory test pin. Connect to DGND. 50 ADC_INA Differential Input to the ADC. 13 LOOPBACK LoopBack Select. 52 CAP_TOP Decoupling Pin for ADC Reference. 14 TX_SYNC Transmit Data Input. 57 CM_LVL Case gond. 16 TX_DXTA Transmit Data Input. 56 KND Aiso Ground. 17 TX_SYNC Transmit Data Inp	Pin	Mnemonic	Description	Pin	Mnemonic	Description
3 MODE_SEL0 Bit Rate—Filter Corner Select. 43 AVDD +5 V Ånalog Supply. 4 MODE_SEL1. Bit Rate—Filter Corner Select. 44 PCA_CC2 PCA Cain Select Bits. 6 PWRDN Power-Down Active Low. 46 PCA_CC0 PCA Cain Select Bits. 7 NC No Connect. 47 AA_FLTR_OUTB Differential Output of the Antialiasing Filter. 9 TX_CGAIN_SEL Transmit Attenuation (6 dB) Select. 40 AA_FLTR_OUTA Differential Output of the Antialiasing Filter. 10 ADC_BUF_BP ADC Buffer Bypass. 49 ADC_INB Differential Input to the ADC. 12 TSTGND Factory test pin. Connect to DGND. 50 ADC_INA Differential Input to the ADC. 14 DGND Digital Ground. 52 CAP_DOT Decoupling Pin for ADC Reference. 15 +3 V_DVDD +3.3 V Digital Supply. 53 CAP_BOT Decoupling Pin for ADC Reference. 16 TX_DATA Transmit Data Input. 54 CM_EVL CM-BOT Digital Ground. 18 TX_CLK Transmit Data Input. 54 ANDD +5 V_DVD +5 V_DVD 19 +5 V_DVDD +5 V Digital Supply. 64 +3 V_DVD +5 V Digital Supply.	1	+5 V_DVDD	+5 V Digital Supply.	41	HYB_IN1_A	Hybrid Inverting Input.
4MODE_SEL1Bit Rate—Filter Corner Select.44PGA_GC2PGA Gain Select Bits.5AA_FLTR_BPAntialiasing Filter Bypass.45PGA_GC1PGA Gain Select Bits.7NCNo Connect.47AA_FLTR_OUTBDifferential Output of the Antialiasing Filter.8TX_GAIN_SELTransmit Driver Bypass.48AA_FLTR_OUTBDifferential Output of the Antialiasing Filter.10ADC_BUF_BPADC BUF Bypass.40ADC_INADifferential Input to the ADC.11TX_LPF_BPTransmit Pilter Bypass.40ADC_INADifferential Input to the ADC.13LOOPBACKLoopback Select.51REF_COMReference Common.14DGNDDigital Ground.52CAP_DOPDecoupling Pin for ADC Reference.17TX_SYNCTransmit Data Frame Sync Input.57AMDD+5 V Digital Supply.5318TX_CLKTransmit Data Frame Sync Input.56CMEVDHaalag Ground.19+5 V_DVDD+5 V Digital Supply.56AMDDHogital Ground.22IOUT_SETDAC Complementary Current Foll Scale With Resistor Lorent Foll Scale	2	DGND	Digital Ground.	42	AGND	Analog Ground.
5 A.FLTR_BP Antialiasing Filter Bypass. 45 PGA_CC1 PGA Gain Select Bits. 6 PWRDN Power-Down Active Low. 46 PGA_CC0 PGA Gain Select Bits. 7 NC No Connect. 47 A.FLTR_OUTB Differential Output of the Antialiasing Filter. 9 TX_DRVR_BP Transmit Driver Bypass. 40 A.FLTR_OUTB Differential Input to the ADC. 10 ADC_BUF_BP ADC DE fuffer Bypass. 40 ADC_INB Differential Input to the ADC. 11 TX_LDRVR_BD Transmit Filter Bypass. 40 ADC_INB Differential Input to the ADC. 12 TSTGND Factory test pin. Connect to DGND. 50 ADC_INB Differential Input to the ADC. 14 DGND Digital Ground. 52 CAP_DOT Decoupling Pin for ADC Reference. 17 TX_SVNC Transmit Icbt Input. 54 VREF Corumon-Mode Level. 18 TX_CLK Transmit Cock Input. 56 ACMD ADG INB Digital Ground. 19 +5 V_DVDD +5 V Digital Supply. 57 ADD +5 V Analog Ground. 41 22 IOUT_SET DAC Competer Informal Node. 58 NC No Connect. 58 23	3	MODE_SEL0	Bit Rate—Filter Corner Select.	43	AVDD	+5 V Analog Supply.
6 FWRDN Power-Doom Active Low. 46 PGA_GC0 PGA Gain Select Bits. 7 NC No Connect. 47 AA.FLTR_OUTB Antialissing Filter. 9 TX.DRVR_BP Transmit Driver Bypass. 48 AA_FLTR_OUTA Differential Output of the Antialissing Filter. 10 ADC_BUF_BP Transmit Filter Bypass. 49 AD_C_INB Differential Input to the ADC. 11 TX_LPF_BP Transmit Filter Bypass. 49 AD_C_INB Differential Input to the ADC. 12 TSTGND Factory test pin. Connect to DGND. 50 ADC_INB Differential Input to the ADC. 13 LOOPBACK Loopback Select. 52 CAP_BOT Decoupling Pin for ADC Reference. 15 +3 V_DVDD +3.3 V Digital Supply. 53 CAP_BOT Common-Mode Level. 17 TX_STAK Transmit Data Input. 56 ACMD 46ND 450 18 TX_CLK Transmit Clock Input. 57 ADDD +5 V Digital Supply. 57 ADDD +5 V Analog Supply. 21 NC No Connect. 61 +3 V_DVDD +5 V Digital Supply. 56 22 IOUT_SET DAC Output Current Full Scale 60 NC No Connect. <	4	MODE_SEL1	Bit Rate—Filter Corner Select.	44	PGA_GC2	PGA Gain Select Bits.
7NCNo Connect.47AA_FLTR_OUTB AA_FLTR_OUTB Differential Output of the Antialiasing Filter.8TX_GAIN_SELTransmit Attenuation (6 dB) Selet.AA_FLTR_OUTA ATTENAME Driver Bypass.MA_FLTR_OUTA ALLER_OUTADifferential Output of the Antialiasing Filter.10ADC_BUF_BPADC Buffer Bypass.49ADC_INBDifferential Input to the ADC.11TX_LPF_BPTransmit Differ Bypass.49ADC_INADifferential Input to the ADC.13LOOPBACKLoopback Select.51REF_COMReference Common.14DGNDDigital Ground.52CAP_TOPDecoupling Pin for ADC Reference.15+3 V_DVDD+3 V Digital Supply.53CAP_BOTDecoupling Pin for ADC Reference.16TX_CLKTransmit Data Input.54VKEFExternal Voltage Reference.17TX_SYNCTransmit Data Frame Sync Input.56AKNDAnalog Ground.18TX_CLKTransmit Data Frame Sync Input.57DeCNDDigital Ground.20DGNDDigital Ground.57PGNDNo Connect.7621NCNo Connect.61+3 V_DVDD+5 V Digital Supply.7322IOUT_SETDAC Output Current Full Scale (With Restor to Ground).62TR_DAC_OUTTming Recovery DAC Output23NCNCNC Connect.64+3 V_DVDD+5 V Digital Supply.24CAP_BDecoupling Pin for Internal Node.62SDATASerial Data <td>5</td> <td>AA_FLTR_BP</td> <td>Antialiasing Filter Bypass.</td> <td>45</td> <td>PGA_GC1</td> <td>PGA Gain Select Bits.</td>	5	AA_FLTR_BP	Antialiasing Filter Bypass.	45	PGA_GC1	PGA Gain Select Bits.
8 TX_GAIN_SEL Transmit Attenuation (6 dB) Select. Image: Constraint of the const	6	PWRDN	Power-Down Active Low.	46	PGA_GC0	PGA Gain Select Bits.
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	40	111D_1111_D	Typing inverting input.	80	RXCLK	Clock Input for ADC Data.

Circuit Description

The AD6472 is an HDSL analog front end for either 2-pair or single pair applications.

Transmit Channel

The AD6472 receives, from a DSP transceiver core, a serial 2s complement data stream. The data are 16-bit words and the MSB is received first.

The 12-bit DAC converts the digital data to an analog signal. Although HDSL uses four level 2B1Q modulation, the 12-bit DAC is necessary because of the linearity requirements of the echo canceling circuit.

The active filters have dynamic tuning and selectable filter corners that meet transmit mask requirements for both two-pair and single pair applications. A 6 dB attenuation option is included as part of the filter to increase the driver output dynamic range. Bypassing the active filter means giving up the 6 dB option, and reduces the maximum TX output voltage to 2 V p-p diff.

The filtered transmit signal is then processed by the driver amplifier. The DAC output controls the driver output level. The designer can choose to bypass the driver amplifier; in this case the driver amplifier will be powered down, and the TX output will be at the TX_LPF_OUT pins.

The AD6472 meets the requirements of the ETSI masks (both frequency and time domains for pulse shape). This includes the worst case in RTR/TM 3036.

Table I.	Transmit	Spectra
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Rate	Application	Nyquist Frequency	Time Interval
Kbps		kHz	Τ (μs)
1168	2-Pair E1	292	1710
2320	Single Pair E1	580	862

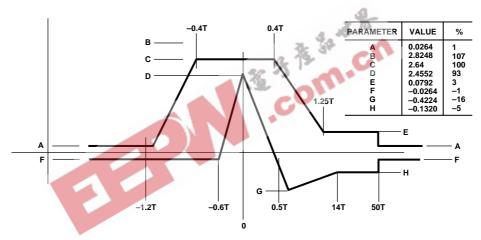


Figure 1. 2-pair Transmit Pulse Shape Mask Normalized

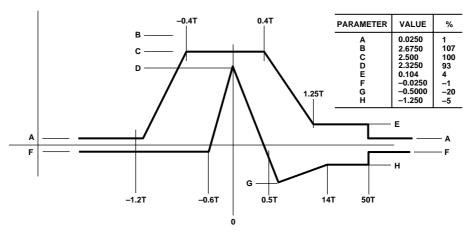


Figure 2. Single Pair Transmit Pulse Shape Mask Normalized

Receive Channel

Hybrid Amplifier

The hybrid amplifier performs balanced to unbalanced conversion.

Programmable Gain Amplifier (PGA)

The PGA can be programmed to amplify the receive signal from between -6 dB and 9 dB. Refer to Table II for PGA gain control information.

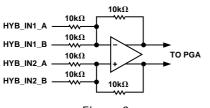


Figure 3.

Transmit and Receive Filters

Refer to Table III for transmit and receive channels filter control information. The receive channel filters meet ETSI requirements.

Analog-to-Digital Converter (ADC)

The receive channel ADC has a pipeline architecture with 12bit resolution. The ADC can be clocked at 2320 kHz, maximum. Output data is provided in 2s complement form.

Timing Recovery D/A

The AD6472 has an integrated D/A converter to control an external VCXO used for timing recovery. The D/A is 7 bits and monotonic. The D/A accepts 7 bits inverted format input data serially with the MSB first.

Configuration Control

Table IV presents control information that you use to configure the AD6472.



Table III.

Receive Channel MODE_SEL1	Filter Control Bit MODE_SEL0	Receive Clock Frequency (kHz)	3 dB Frequency (kHz)
0	0	1168/2	Rx = 320/Tx = 320
0	1	Reserved	Reserved
1	0	1160	Rx = 640/Tx = 535
1	1	1160×2	Rx = 640/Tx = 535

Table IV.	Configuration	Control
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Pin	Mnemonic	Logic 0 = Function	Logic 1 = Function
5	AA_FLTR_BP	Receive Filter in Circuit	Receive Filter Bypassed
6	PWRDN	Low Power Selected	Normal Operating Mode
7	ADC_BUF_BP	ADC Buffer in Circuit	ADC Buffer Bypassed
8	TX_GAIN_SEL	0 dB Attenuation	6 dB Attenuation
9	TX_DRVR_BP	Line Driver in Circuit	Line Driver Bypassed
11	TX_LPF_BP	Transmit Filter in Circuit	Transmit Circuit Bypassed
13	LOOPBACK	Normal Operation	Analog Loopback Selected

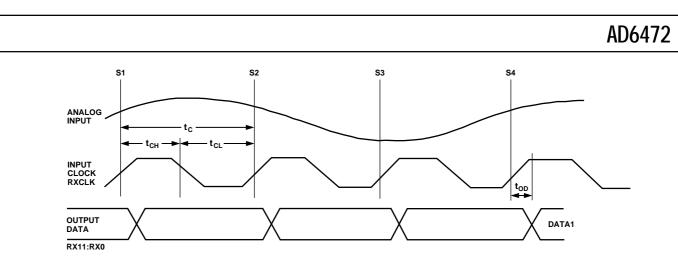


Figure 4. Receive Interface Timing Diagram

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Receive Interface Timing

The analog input is sampled at the rising edge of the RXCLK. The digital data, RX11:RX0, is valid on each falling edge of RXCLK. Figure 4 shows a three-cycle latency on the receive data.

Table V through Table VII lists the RXCLK clock switching specifications for various RXCLK conditions. See Table IV, Configuration Control.

Table V. 40% to 60% Duty Cycle when the RXCLK = 1168 ÷ 2 kHz

Symbol	Parameter	Min Typ	Max	Units
t _C	Clock Period	1712		ns
t _{CH}	Clock Pulsewidth High	685 1	1027	ns
t _{CL}	Clock Pulsewidth Low	1027	685	ns
t _{OD}	Output Delay	8 13 1	19	ns
Latency	Pipeline Delay	3 3 3	3	Cycles

Table VI. 40% to 60% Duty Cycle RXCLK Clock when the RXCLK = 1160 kHz

Symbol	Parameter	Min	Тур	Max	Units
t _C	Clock Period		862		ns
t _{CH}	Clock Pulsewidth High	342		514	ns
t _{CL}	Clock Pulsewidth Low	514		342	ns
t _{OD}	Output Delay	8	13	19	ns
Latency	Pipeline Delay	3	3	3	Cycles

Table VII. 40% to 60% Duty Cycle RXCLK when theRXCLK = 1160 × 2 kHz

Symbol	Parameter	Min	Тур	Max	Units
t _C	Clock Period		431		ns
t _{CH}	Clock Pulsewidth High	171		257	ns
t _{CL}	Clock Pulsewidth Low	257		171	ns
t _{OD}	Output Delay	8	13	19	ns
Latency	Pipeline Delay	3	3	3	Cycles

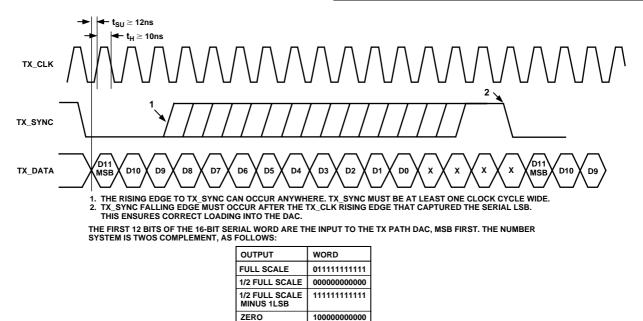
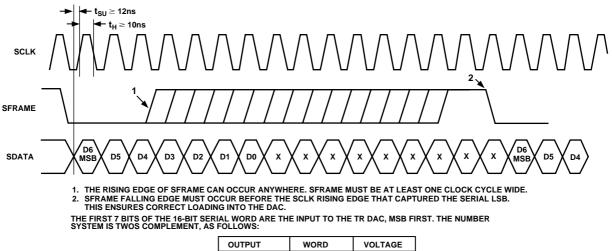


Figure 5. Transmit Interface Timing Diagram



OUTPUT	WORD	VOLTAGE
FULL SCALE	1111111	4.5
MID-SCALE	1000000	2.5
MINIMUM	0000000	0.5

X

Figure 6. Timing Recovery DAC Converter Timing

PCB Layout Recommendations

Analog and Digital Ground Planes	Separate the analog and digital grounds. Use a single 35 to 50 mil wide trace un- der the device to connect the two ground planes. Connect the IC ground pins directly to the respective ground planes.
Power Supply Capacitors	Use one 0.1 µF capacitor for each IC de- coupling power supply connection in addi- tion to capacitance shown in schematic.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

80-Lead Metric Plastic Quad Flatpack S-80A

