Low-Voltage 1.8/2.5/3.3V 16-Bit Buffer

With 3.6 V-Tolerant Inputs and Outputs (3-State, Inverting)

The 74VCX16240 is an advanced performance, inverting 16-bit buffer. It is designed for very high-speed, very low-power operation in 1.8 V, 2.5 V or 3.3 V systems.

When operating at 2.5 V (or 1.8 V) the part is designed to tolerate voltages it may encounter on either inputs or outputs when interfacing to 3.3 V busses. It is guaranteed to be over-voltage tolerant to 3.6 V.

The 74VCX16240 is nibble controlled with each nibble functioning identically, but independently. The control pins may be tied together to obtain full 16-bit operation. The 3-state outputs are controlled by an Output Enable (\overline{OEn}) input for each nibble. When \overline{OEn} is LOW, the outputs are on. When \overline{OEn} is HIGH, the outputs are in the high impedance state.

Features

- Designed for Low Voltage Operation: $V_{CC} = 1.65 \text{ V} 3.6 \text{ V}$
- 3.6V Tolerant Inputs and Outputs
- High Speed Operation: 2.5 ns max for 3.0 V to 3.6 V

3.0 ns max for 2.3 V to 2.7 V

6.0 ns max for 1.65 V to 1.95 V

• Static Drive: ±24 mA Drive at 3.0 V

±18 mA Drive at 2.3 V

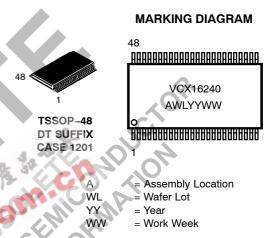
±6 mA Drive at 1.65 \

- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V
- Near Zero Static Supply Current in All Three Logic States (20 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds ±250 mA @ 125°C
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V
- All Devices in Package TSSOP are Inherently Pb-Free*



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ORDERING INFORMATION

Device	Package	Shipping [†]
74VCX16240DT	TSSOP (Pb-Free)	39 / Rail
74VCX16240DTR	TSSOP (Pb-Free)	2500 / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

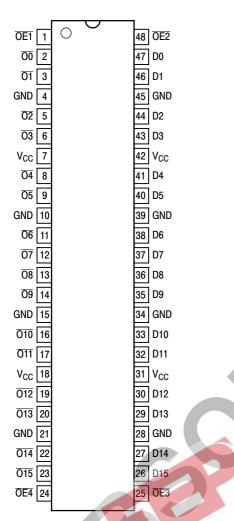


Figure 1. 48-Lead Pinout (Top View)

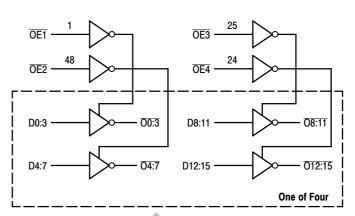


Figure 2. Logic Diagram

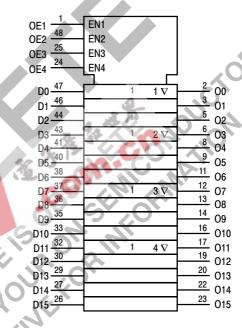


Figure 3. IEC Logic Diagram

26 D15 25 OE3 . 48-Lead Pinout Top View) Table 1. PIN NAMES	D10 33 16 01 17 01 17 01 19 01
Pins	Function
OEn D0-D15 O0-O15	Output Enable Inputs Inputs Outputs
RV	

TRUTH TABLE

OE1	D0:3	O0:3	OE2	D4:7	04:7	OE3	D8:11	O8:11	OE4	D12:15	012:15
L	L	Н	L	L	Н	L	L	Н	L	L	Н
L	Н	L	L	Н	L	L	Н	L	L	Н	L
Н	Х	Z	Н	Х	Z	Н	Х	Z	Н	Х	Z

H = High Voltage Level;

L = Low Voltage Level;

Z = High Impedance State;

X = High or Low Voltage Level and Transitions Are Acceptable, for ICC reasons, DO NOT FLOAT Inputs

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V _{CC}	DC Supply Voltage	-0.5 to +4.6		V
VI	DC Input Voltage	-0.5 ≤ V _I ≤ +4.6		V
V _O	DC Output Voltage	$-0.5 \le V_{O} \le +4.6$	Output in 3-State	V
		$-0.5 \le V_{O} \le V_{CC} + 0.5$	Note 1; Outputs Active	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
lok	DC Output Diode Current	-50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
Io	DC Output Source/Sink Current	±50		mA
Icc	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current Per Ground Pin	±100		mA
T _{STG}	Storage Temperature Range	-65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	27	Min	Тур	Max	Unit
V _{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.2	3.3 3.3	3.6 3.6	V
VI	Input Voltage	The second	-0.3		3.6	V
Vo	Output Voltage	(Active State) (3-State)	0		V _{CC} 3.6	V
I _{OH}	HIGH Level Output Current, V _{CC} = 3.0 V - 3.6 V	-V .O. <			-24	mA
I _{OL}	LOW Level Output Current, V _{CC} = 3.0 V - 3.6 V	20,00			24	mA
I _{OH}	HIGH Level Output Current, V _{CC} = 2.3 V – 2.7 V				-18	mA
I _{OL}	LOW Level Output Current, V _{CC} = 2.3 V - 2.7 V				18	mA
I _{OH}	HIGH Level Output Current, V _{CC} = 1.65 V - 1.95 V				-6	mA
I _{OL}	LOW Level Output Current, V _{CC} = 1.65 V - 1.95 V				6	mA
T _A	Operating Free-Air Temperature		-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V _{IN} from 0.8 V to	2.0 V, V _{CC} = 3.0 V	0		10	ns/V
	Input transmon rise of Fall hate, VIA now 0.5 V to					

^{1.} I_O absolute maximum rating must be observed.

DC ELECTRICAL CHARACTERISTICS

			T _A = -40°0	C to +85°C	
Symbol	Characteristic	Condition	Min	Max	Unit
V _{IH}	HIGH Level Input Voltage (Note 2)	1.65 V ≤ V _{CC} < 2.3 V	0.65 x V _{CC}		٧
		2.3 V ≤ V _{CC} ≤ 2.7 V	1.6		1
		2.7 V < V _{CC} ≤ 3.6 V	2.0		1
V _{IL}	LOW Level Input Voltage (Note 2)	1.65 V ≤ V _{CC} < 2.3 V		0.35 x V _{CC}	V
		2.3 V ≤ V _{CC} ≤ 2.7V		0.7	1
		2.7 V < V _{CC} ≤ 3.6 V		0.8	1
V _{OH}	HIGH Level Output Voltage	1.65 V ≤ V _{CC} ≤ 3.6 V; I _{OH} = −100 μA	V _{CC} - 0.2		V
		V _{CC} = 1.65 V; I _{OH} = -6 mA	1.25		1
		$V_{CC} = 2.3 \text{ V; } I_{OH} = -6 \text{ mA}$	2.0		1
		V _{CC} = 2.3 V; I _{OH} = -12 mA	1.8		1
		V _{CC} = 2.3 V; I _{OH} = -18 mA	1.7		1
		V _{CC} = 2.7 V; I _{OH} = -12 mA	2.2		1
		V _{CC} = 3.0 V; I _{OH} = -18 mA	2.4		1
		$V_{CC} = 3.0 \text{ V; } I_{OH} = -24 \text{ mA}$	2.2		
V _{OL}	LOW Level Output Voltage	$1.65 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{I}_{OL} = 100 \mu\text{A}$	2.10	0.2	٧
		$V_{CC} = 1.65 \text{ V; } I_{OL} = 6 \text{ mA}$		0.3	
		$V_{CC} = 2.3 \text{ V; } l_{OL} = 12 \text{ mA}$		0.4	
		$V_{CC} = 2.3 \text{ V; } I_{OL} = 18 \text{ mA}$		0.6	
		$V_{CC} = 2.7 \text{ V; } I_{OL} = 12 \text{ mA}$		0.4	
		$V_{CC} = 3.0 \text{ V; } I_{OL} = 18 \text{ mA}$		0.4	
		$V_{CC} = 3.0 \text{ V; } I_{OL} = 24 \text{ mA}$		0.55	
lį	Input Leakage Current	$1.65 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; 0 \text{ V} \le \text{V}_{I} \le 3.6 \text{ V}$		±5.0	μА
l _{OZ}	3-State Output Current	$1.65 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; 0 \text{ V} \le \text{V}_{O} \le 3.6 \text{ V};$ $\text{V}_{I} = \text{V}_{IH} \text{ or V}_{IL}$		±10	μΑ
I _{OFF}	Power-Off Leakage Current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 3.6 \text{ V}$		10	μΑ
I _{CC}	Quiescent Supply Current (Note 3)	$1.65 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{ V}_{I} = \text{GND or V}_{CC}$		20	μА
		$1.65 \text{ V} \le \text{V}_{\text{CC}} \le 3.6 \text{ V}; 3.6 \text{ V} \le \text{V}_{\text{I}}, \text{V}_{\text{O}} \le 3.6 \text{ V}$		±20	μА
ΔI_{CC}	Increase in I _{CC} per Input	2.7 V < V _{CC} ≤ 3.6 V; V _{IH} = V _{CC} − 0.6 V		750	μΑ

^{2.} These values of V₁ are used to test DC electrical characteristics only.

3. Outputs disabled or 3–state only.

AC CHARACTERISTICS (Note 4; t_R = t_F = 2.0 ns; C_L = 30 pF; R_L = 500 Ω)

					$T_A = -40^\circ$	C to +85°C			
			V _{CC} = 3.0	V to 3.6 V	V _{CC} = 2.3	V to 2.7 V	V _{CC} = 1.6	5 to 1.95V	
Symbol	Parameter	Waveform	Min	Max	Min	Max	Min	Max	Unit
t _{PLH} t _{PHL}	Propagation Delay Input to Output	1	0.8 0.8	2.5 2.5	1.0 1.0	3.0 3.0	1.5 1.5	6.0 6.0	ns
t _{PZH}	Output Enable Time to High and Low Level	2	0.8 0.8	3.5 3.5	1.0 1.0	4.1 4.1	1.5 1.5	8.2 8.2	ns
t _{PHZ}	Output Disable Time From High and Low Level	2	0.8 0.8	3.5 3.5	1.0 1.0	3.8 3.8	1.5 1.5	7.8 7.8	ns
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 5)			0.5 0.5		0.5 0.5		0.75 0.75	ns

^{4.} For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

AC CHARACTERISTICS ($t_R = t_F = 2.0 \text{ ns}$; $C_L = 50 \text{ pF}$; $R_L = 500 \Omega$)

			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			
			V _{CC} = 3.0	V to 3.6V Vcc =	= 2.7V	
Symbol	Parameter	Waveform	Min	Max	Max	Unit
t _{PLH} t _{PHL}	Propagation Delay Input to Output	3	1.0	3.9 3.9	5.3 5.3	ns
t _{PZH} t _{PZL}	Output Enable Time to High and Low Level	4	1.0 1.0	5.0 5.0	6.1 6.1	ns
t _{PHZ} t _{PLZ}	Output Disable Time From High and Low Level	4	1.0 1.0	4.4 4.4	4.8 4.8	ns
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 6)		10° 11	0.5 0.5	0.5 0.5	ns

^{6.} Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

^{5.} Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	Typical (T _A = +25°C)	Unit
V _{OLP}	Dynamic LOW Peak Voltage (Note 7)	$V_{CC} = 1.8 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0 \text{ V}$	0.25	V
		$V_{CC} = 2.5 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0 \text{ V}$	0.6	
		V_{CC} = 3.3 V, C_L = 30 pF, V_{IH} = V_{CC} , V_{IL} = 0 V	0.8	
V _{OLV}	Dynamic LOW Valley Voltage (Note 7)	$V_{CC} = 1.8 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0 \text{ V}$	-0.25	V
		V_{CC} = 2.5 V, C_L = 30 pF, V_{IH} = V_{CC} , V_{IL} = 0 V	-0.6	
		$V_{CC} = 3.3 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0 \text{ V}$	-0.8	
V _{OHV}	Dynamic HIGH Valley Voltage (Note 8)	V_{CC} = 1.8 V, C_L = 30 pF, V_{IH} = V_{CC} , V_{IL} = 0 V	1.5	V
		$V_{CC} = 2.5 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0 \text{ V}$	1.9	
		$V_{CC} = 3.3 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0 \text{ V}$	2.2	1

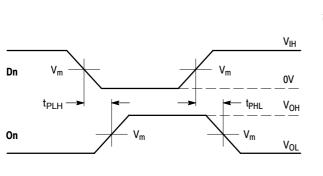
^{7.} Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

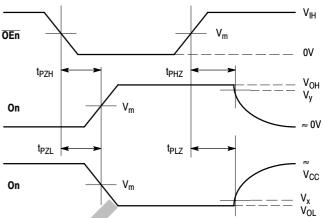
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition Typical U	Jnit
C _{IN}	Input Capacitance	Note 9 6 p	pF
C _{OUT}	Output Capacitance	Note 9 7	pF
C _{PD}	Power Dissipation Capacitance	Note 9, 10 MHz 20 p	pF

^{9.} V_{CC} = 1.8 V, 2.5 V or 3.3 V; V_I = 0 V or V_{CC}.

^{8.} Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the HIGH state.





WAVEFORM 1 - PROPAGATION DELAYS

 $t_R = t_F = 2.0 \text{ ns}, 10\% \text{ to } 90\%; f = 1 \text{ MHz}; t_W = 500 \text{ ns}$

WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES t_R = t_F = 2.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

Figure 4. AC Waveforms

Table 2. AC WAVEFORMS

		V _{CC}	A.A.
Symbol	3.3 V ± 0.3 V	2.5 V ± 0.2 V	1.8 V ± 0.15 V
V _{IH}	2.7 V	V _{CC}	Vcc
V _m	1.5 V	V _{CC} /2	V _{CC} /2
V_x	V _{OL} + 0.3 V	V _{OL} + 0.15 V	V _{OL} + 0.15 V
V _y	V _{OH} - 0.3 V	V _{OH} – 0.15 V	V _{OH} – 0.15 V

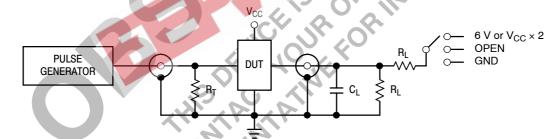
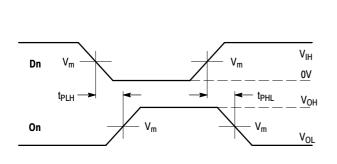


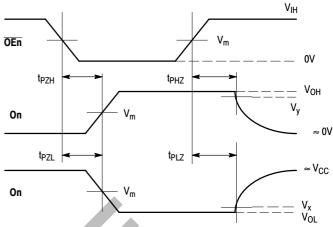
Figure 5. Test Circuit

Table 3. TEST CIRCUIT

TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	6 V at V_{CC} = 3.3 ± 0.3 V; V_{CC} × 2 at V_{CC} = 2.5 ± 0.2 V; 1.8 ± 0.15 V
t _{PZH} , t _{PHZ}	GND

 C_L = 30 pF or equivalent (Includes jig and probe capacitance) R_L = 500 Ω or equivalent R_T = Z_{OUT} of pulse generator (typically 50 Ω)





WAVEFORM 3 - PROPAGATION DELAYS

 t_R = t_F = 2.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

WAVEFORM 4 – OUTPUT ENABLE AND DISABLE TIMES $t_R = t_F = 2.0 \text{ ns}, \, 10\% \text{ to } 90\%; \, f = 1 \text{ MHz}; \, t_W = 500 \text{ ns}$

Figure 6. AC Waveforms

Table 4. AC WAVEFORMS

	Vec		
Symbol	3.3 V ± 0.3 V	2.7 V	
V _{IH}	2.7 V	2.7 V	
V _m	1.5 V	1.5 V	
V _x	V _{OL} + 0.3 V	V _{OL} + 0.3 V	
V _y	V _{OH} - 0.3 V	V _{OH} – 0.3 V	

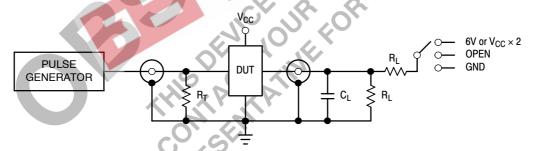


Figure 7. Test Circuit

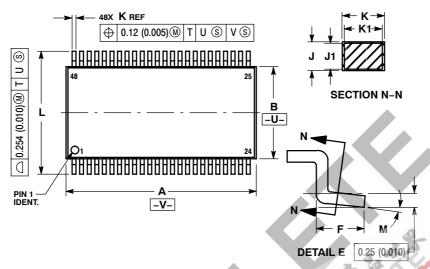
Table 5. TEST CIRCUIT

TEST	SWITCH	
t _{PLH} , t _{PHL}	Open	
t _{PZL} , t _{PLZ}	6 V at V_{CC} = 3.3 ± 0.3 V; V_{CC} × 2 at V_{CC} = 2.5 ± 0.2 V; 1.8 ± 0.15 V	
t _{PZH} , t _{PHZ}	GND	

 C_L = 50 pF or equivalent (Includes jig and probe capacitance) R_L = 500 Ω or equivalent R_T = Z_{OUT} of pulse generator (typically 50 Ω)

PACKAGE DIMENSIONS

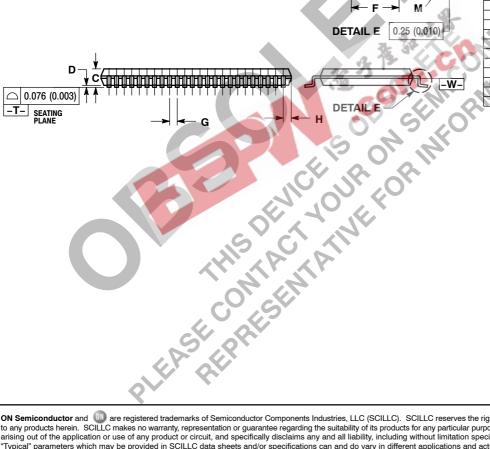
TSSOP DT SUFFIX CASE 1201-01 **ISSUE A**



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSIONS A AND B DO NOT INCLUDE
 MOLD FLASH, PROTRUSIONS OR GATE
 BURRS. MOLD FLASH OR GATE BURRS
 SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION K DOES NOT INCLUDE DAMBAR
 PROTRUSION. SALLOWABLE DAMBAR
 PROTRUSION. SALLOWABLE DAMBAR
 BORTHLISON. SALLOWABLE DE DAMBAR
- PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY. DIMENSIONS A AND B ARE TO BE
- DETERMINED AT DATUM PLANE -W-

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	12.40	12.60	0.488	0.496
В	6.00	6.20	0.236	0.244
С	4	1.10		0.043
D a	0.05	0.15	0.002	0.006
E	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
Н	0.37	22-	0.015	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8°	0 °	8°



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