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## SN74ALVCH16344 1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

SCES054H-SEPTEMBER 1995-REVISED SEPTEMBER 2004

#### **FEATURES**

- Member of the Texas Instruments Widebus™
   Family
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

#### **DESCRIPTION/ORDERING INFORMATION**

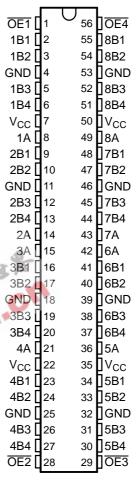
This 1-bit to 4-bit address driver is designed for 1.65-V to 3.6-V  $\mbox{V}_{\rm CC}$  operation.

The SN74ALVCH16344 is used in applications in which four separate memory locations must be addressed by a single address.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

# DGG OR DL PACKAGE (TOP VIEW)



#### ORDERING INFORMATION

T <sub>A</sub>	PACK	AGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	CCOD DI	Tube	SN74ALVCH16344DL	ALVC1146244
-40°C to 85°C	SSOP - DL	Tape and reel	SN74ALVCH16344DLR	ALVCH16344
	TSSOP - DGG	Tape and reel	SN74ALVCH16344DGGR	ALVCH16344

 Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

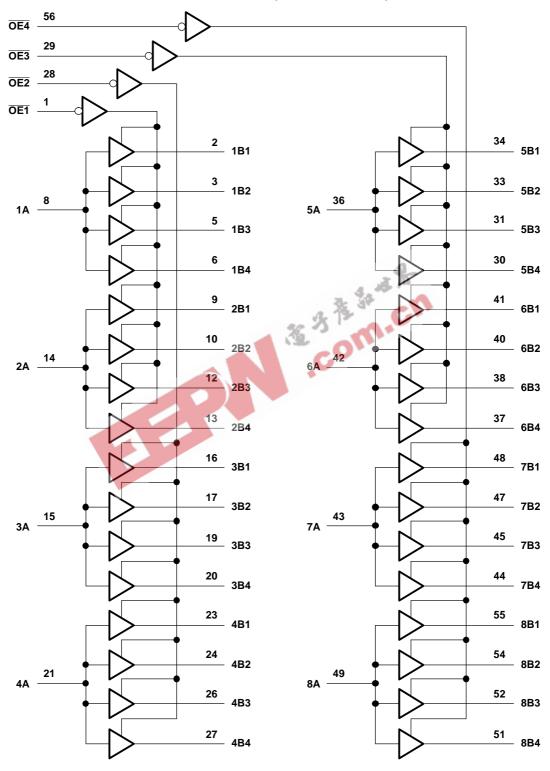
#### **FUNCTION TABLE**

INPL	JTS	OUTPUT			
ŌĒ	Α	Bn			
L	Н	Н			
L	L	L			
Н	Н	Z			

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



## LOGIC DIAGRAM (POSITIVE LOGIC)





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## **ABSOLUTE MAXIMUM RATINGS**(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range		-0.5	4.6	V	
$V_{I}$	Input voltage range <sup>(2)</sup>		-0.5	4.6	V	
Vo	Output voltage range <sup>(2)(3)</sup>		-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA	
I <sub>OK</sub>	Output clamp current		-50	mA		
Io	Continuous output current			±50		
	Continuous current through each V <sub>CC</sub> or GN	D		±100	mA	
0	Dealer of the constitute of th	DGG package		64	0000	
$\theta_{JA}$	Package thermal impedance (4)	DL package		56	°C/W	
T <sub>stg</sub>	Storage temperature range		-65	150	°C	

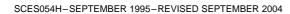
- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- 3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

## **RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		132	MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	CO	1.65	3.6	V	
		V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$			
$V_{IH}$	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC}$ = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
	Low-level input voltage  Input voltage Output voltage High-level output current  Low-level output current	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
$V_{I}$	Input voltage		0	$V_{CC}$	V	
Vo	Output voltage		0	V <sub>CC</sub>	V	
		V <sub>CC</sub> = 1.65 V		-4		
	High level output ourrent	V <sub>CC</sub> = 2.3 V		-12	mΛ	
I <sub>OH</sub>	nigri-level output current	V <sub>CC</sub> = 2.7 V		-12	mA	
		V <sub>CC</sub> = 3 V		-24		
		V <sub>CC</sub> = 1.65 V		4		
	Low lovel output ourrent	V <sub>CC</sub> = 2.3 V		12	mA	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V		12	IIIA	
		V <sub>CC</sub> = 3 V	24			
Δt/Δν	Input transition rise or fall rate			10	ns/V	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C	

<sup>(1)</sup> All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# **SN74ALVCH16344** 1-BIT TO 4-BIT ADDRESS DRIVER **WITH 3-STATE OUTPUTS**





#### **ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT			
		I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2						
		I <sub>OH</sub> = -4 mA	1.65 V	1.2	·					
		I <sub>OH</sub> = -6 mA	2.3 V	2						
$V_{OH}$			2.3 V	1.7			V			
		I <sub>OH</sub> = -12 mA	2.7 V	2.2						
			3 V	2.4						
		I <sub>OH</sub> = -24 mA	3 V	2	<del></del>					
		I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2				
		I <sub>OL</sub> = 4 mA	1.65 V			0.45				
.,		I <sub>OL</sub> = 6 mA	2.3 V			0.4	.,			
VOL		104	2.3 V		·	0.7	V			
	I <sub>OL</sub> = 12 mA	2.7 V		·	0.4					
	l <sub>I</sub>	I <sub>OL</sub> = 24 mA	3 V		·	0.55				
I <sub>I</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V		·	±5	μΑ			
		V <sub>I</sub> = 0.58 V	1.65 V	25						
		V <sub>I</sub> = 1.07 V	1.65 V	-25	·					
		V <sub>I</sub> = 0.7 V	2.3 V	45	·					
I <sub>I(hold)</sub>		V <sub>I</sub> = 1.7 V	2.3 V	-45	·		μΑ			
		V <sub>I</sub> = 0.8 V	3 V	75						
		V <sub>I</sub> = 2 V	3 V	-75						
		V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>	3.6 V		·	±500				
l <sub>OZ</sub>		$V_O = V_{CC}$ or GND	3.6 V		<del></del>	±10	μΑ			
I <sub>CC</sub>		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		<del></del>	40	μΑ			
$\Delta I_{CC}$		One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μΑ			
(	Control inputs	V V or CND	221		2.5		- n-F			
C <sub>i</sub> Data inputs		$V_I = V_{CC}$ or GND	3.3 V	3.5			pF			
C <sub>o</sub> C	Outputs	$V_O = V_{CC}$ or GND	3.3 V		4		pF			

#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2 ± 0.2	2.5 V V	V <sub>CC</sub> = 2.7	V	V <sub>CC</sub> = 3 ± 0.3	3.3 V V	UNIT
	(INT OT)	(OUTPUT)	TYP	MIN	MAX	MIN I	XAN	MIN	MAX	
t <sub>pd</sub>	Α	В	(1)	1	4.6		4.6	1.4	4	ns
t <sub>en</sub>	ŌĒ	В	(1)	1	6.2		6.2	1.2	5.1	ns
t <sub>dis</sub>	ŌĒ	В	(1)	1	5.1		4.4	1.2	4	ns
t <sub>sk(o)</sub> (2)									0.35	ns
t <sub>sk(o)</sub> (3)	_							·	0.5	ns

<sup>(1)</sup> This information was not available at the time of publication.

<sup>(1)</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ . (2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

Skew between outputs of same bank and same package (same transition)

Skew between outputs of all banks and same package (A1 through A8 tied together)





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## **OPERATING CHARACTERISTICS**

 $T_A = 25^{\circ}C$ 

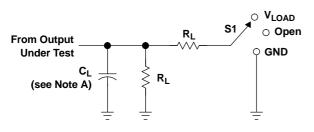
PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 1.8 V TYP	V <sub>CC</sub> = 2.5 V TYP	V <sub>CC</sub> = 3.3 V TYP	UNIT
_	Power dissipation capacitance	Outputs enabled	C 50 °F 4 40 MHz	(1)	68	84	~F
Cpd	per bit (four outputs switching)	Outputs disabled	$C_L = 50 \text{ pF, f} = 10 \text{ MHz}$	(1)	11	14	pF

(1) This information was not available at the time of publication.





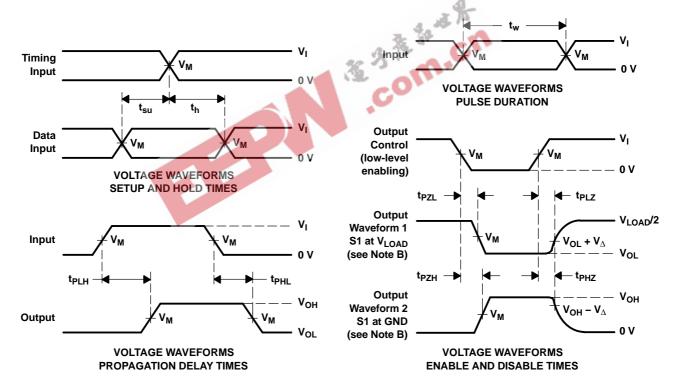
#### PARAMETER MEASUREMENT INFORMATION



TEST	<b>S</b> 1
t <sub>pd</sub> t <sub>PLZ</sub> /t <sub>PZL</sub>	Open V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

LOAD CIRCUIT

V	INPUT		V	V		В	V
V <sub>CC</sub>	V <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	V <sub>LOAD</sub>	CL	$R_L$	$V_{\Delta}$
1.8 V	v <sub>cc</sub>	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
3.3 V $\pm$ 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	<b>500</b> Ω	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



#### PACKAGE OPTION ADDENDUM

27-Sep-2007

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ALVCH16344DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16344DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16344DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16344DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16344DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16344DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16344DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): Tl's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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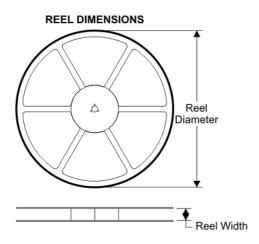
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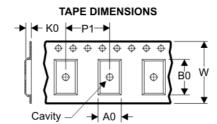


# **PACKAGE MATERIALS INFORMATION**

4-Oct-2007

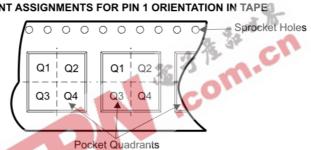
## TAPE AND REEL BOX INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPES

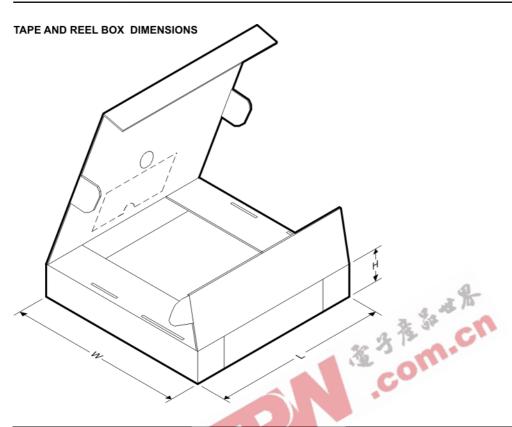


Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16344DGGR	DGG	56	SITE 41	330	24	8.6	15.6	1.8	12	24	Q1
SN74ALVCH16344DLR	DL	56	SITE 41	330	32	11.35	18.67	3.1	16	32	Q1





4-Oct-2007

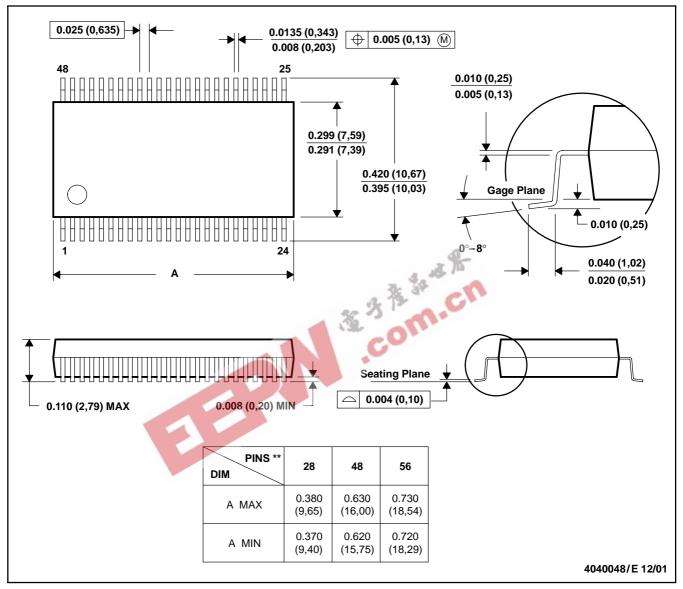


Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16344DGGR	DGG	56	SITE 41	346.0	346.0	41.0
SN74ALVCH16344DLR	DL	56	SITE 41	346.0	346.0	49.0

#### DL (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE PACKAGE

#### **48 PINS SHOWN**



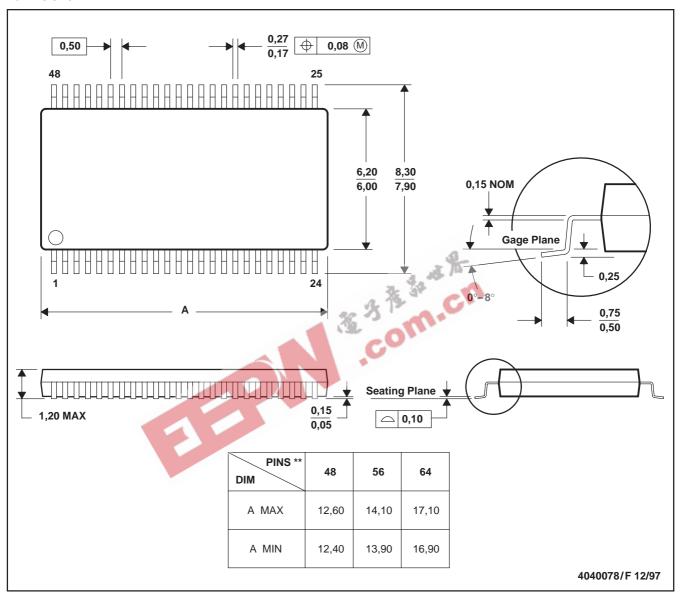
NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

## DGG (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE PACKAGE

#### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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