ANALOG DEVICES

Compact, 1.5 A Linear Charger for Single-Cell Li+ Battery

ADP2291

FEATURES

Simple, safe linear charger for single cell lithium battery
4.5 V to 12 V input voltage range
Adjustable charging current up to 1.5 A
Low cost PNP external pass element
Automatic reverse isolation with no external blocking diode
Output overshoot protection
Deep discharge precharge mode
Thermal shutdown
Automatic recharge
Programmable termination timer
LED charging status indicator
4.2 V output voltage with ±1% accuracy over line and temperature
1 µA shutdown supply current
Small, 8-pin MSOP and 3 × 3 mm LFCSP packages

APPLICATIONS

Wireless handsets
Smart handhelds and PDAs
Digital cameras
Single cell lithium ion-powered systems
Cradle chargers

GENERAL DESCRIPTION

The ADP2291 is a constant-current/constant-voltage linear charger for a single cell lithium ion battery, requiring just a few components to provide a simple and safe charging system that operates from a wide 4.5 V to 12 V input voltage range. It features an internally controlled, multistep charging cycle that improves battery life.

An external, low cost, PNP provides the charging current to the battery and an external resistor sets the maximum charge current. A small external capacitor programs the maximum charge time. The controller includes an LED driver to indicate the battery charging status.

Safety features include charging stop mode for battery faults, output overshoot protection, and thermal shutdown. The ADP2291 also features automatic reverse isolation, which does not require an additional blocking diode.

The multistep charge cycle optimizes the battery charging time in a safe manner. It features a trickle charge mode for a deeply discharged cell and a fast charging mode with a maximum current of 1.5 A. The ADP2291 controls the end of charge with a 4.2 V output voltage that is 1% accurate over line and temperature. It automatically recharges the battery if the cell voltage drops. When the input supply is removed, the part enters a low current state and reduces the current drawn from the battery to below 1 µA.

The ADP2291 is available in both a small, 8-pin MSOP package and a 3 × 3 mm LFCSP package that is ideally suited for small, portable applications.
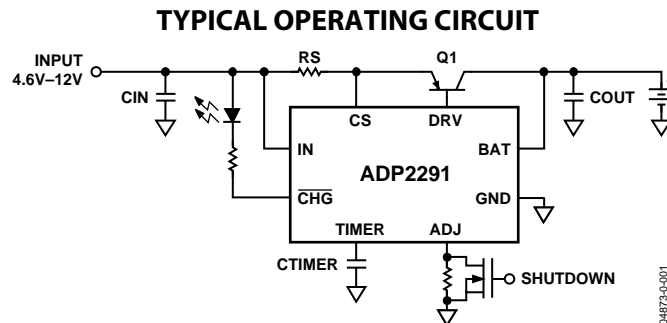
TYPICAL OPERATING CIRCUIT

Figure 1. Basic Circuit Configuration

ADP2291

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REVISION HISTORY

10/04—Initial Version: Revision 0

SPECIFICATIONS

V_{IN} = 5.5 V, V_{BAT} = 4.2 V, R_{ADJ} open, T_A = –40°C to +85°C, typical values are at 25°C unless otherwise noted.[1]

Table 1. Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Power Supply, IN					
Input Voltage		4.5		12	V
Current Draw	Fast charge/precharge/end-of-charge modes		6	9	mA
	Timeout/shutdown/battery fault		1.4	1.8	mA
Battery Voltage, BAT					
Voltage Accuracy, End-of-charge ($V_{BAT, EOC}$)	T_A = 0°C to +50°C V_{IN} = 4.5 V to 12 V V_{IN} – V_{CS} = VRS/10	4.158	4.2	4.242	V
Load Regulation, No Battery	V_{IN} – V_{CS} = 0 to VRS		–80		mV
Current Draw	Timeout mode V_{IN} = 4.5 V to 12 V			45	µA
Current Draw	Battery fault/shutdown mode V_{IN} = 4.5 V to 12 V		0.1	1	µA
Reverse Leakage Current	Power-down mode V_{IN} = float, V_{BAT} = 4.2 V		0.1		µA
Fast Charge Mode					
Sense Voltage Setpoint (VRS)	V_{IN} – V_{CS}, R_{ADJ} = open V_{IN} = 4.5 V to 12 V V_{BAT} = 3.6 V	140	150	160	mV
Sense Voltage Setpoint (VRS)	V_{IN} – V_{CS}, R_{ADJ} = 100 kΩ V_{IN} = 4.5 V to 12 V V_{BAT} = 3.6 V	40	50	60	mV
Current Regulation Adjustment	per V of (3 V – V_{ADJ})		67		mV/V
Precharge Mode					
Sense Voltage Setpoint (VRS)	V_{IN} – V_{CS}, R_{ADJ} = open V_{IN} = 4.5 V to 12 V V_{BAT} = 2 V	10	15	20	mV
Sense Voltage Setpoint (VRS)	V_{IN} – V_{CS}, R_{ADJ} = 100 kΩ V_{IN} = 4.5 V to 12 V V_{BAT} = 2 V	5	10	15	mV
BAT Precharge Threshold	V_{BAT} rising	2.65		2.85	V
Hysteresis			70		mV
Shutdown Mode					
ADJ Shutdown Threshold	V_{ADJ} falling, V_{IN} = 4.5 V	0.30		0.45	V
Hysteresis			40		mV
Pullup current from ADJ	V_{ADJ} = 0		40		µA
Power-Down Mode					
V_{IN} Powerdown Threshold	V_{IN} rising	3.6		4	V
Hysteresis			220		mV
V_{IN}_Good Comparator					
Threshold (V_{IN} > V_{BAT})	V_{IN} rising	125	170	220	mV
Hysteresis			110		mV
EOC Comparator					
Current Threshold	V_{IN} – V_{CS} falling, R_{ADJ} = open, relative to VRS	7	10	13	%
Current Threshold	V_{IN} – V_{CS} falling, R_{ADJ} = 100 kΩ, relative to VRS	6	10	16	%
Hysteresis			12		mV
Restart Comparator					
BAT Restart Threshold	V_{IN} > 4.5 V, V_{BAT} falling, relative to $V_{BAT, EOC}$	–170			mV

ADP2291

Parameter	Conditions	Min	Typ	Max	Unit
Battery Charge Timer					
Charge/Discharge TIMER Current		21.0	24.0	27.0	µA
Low Threshold			1.2		V
High Threshold			2.0		V
High-Low Threshold Delta[2]		750		850	mV
Overshoot Protection					
BAT Threshold		4.7	5	5.3	V
Current Sink	<2 ms duration		1.5		A
$\overline{CHG}$ Output					
Output Voltage Low	Current = 20 mA			0.45	V
Output Leakage Current	$V_{\overline{CHG}}$ = 5 V		0.1	1	µA
Base Drive Capability					
Max Base Drive Current		40			mA
Thermal Shutdown					
Shutdown Threshold	T_A rising		135		°C
Hysteresis			35		°C

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). Typical values are at T_A = 25° C.
[2] Guaranteed by design, not tested in production.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
IN, DRV[1], CS, $\overline{CHG}$, to GND	−0.3 V to +13.5 V
BAT, ADJ, TIMER to GND	−0.3 V to (V_{IN} + 0.3 V)
Operating Ambient Temperature	−40°C to +85°C
Operating Junction Temperature	−40°C to +125°C
θ_{JA}, 2-layer MSOP-8	220°C/W
θ_{JA}, 4-layer MSOP-8	158°C/W
θ_{JA}, 2-layer LFCSP-8	62°C/W
θ_{JA}, 4-layer LFCSP-8	48°C/W
Storage Temperature	−65°C to +150°C
Lead Temperature Range Soldering (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages referenced to GND.

[1] Pulling current from the DRV pin by driving it below ground, while V_{IN} is applied, may cause permanent damage to the device.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS
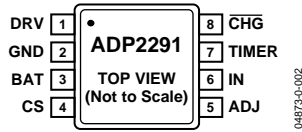
Figure 2. 8-Lead MSOP
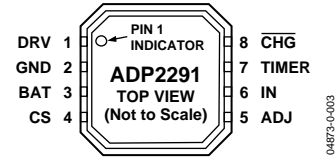
Figure 3. 8-Lead LFCSP

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DRV	Base Driver Output. Controls the base of an external PNP pass transistor.
2	GND	Ground.
3	BAT	Battery Voltage Sense Input.
4	CS	Current Sense Resistor Negative Input.
5	ADJ	Charging Current Adjust and Charger Shutdown Input.
6	IN	Power Input and Current-Sense Resistor Positive Input.
7	TIMER	Timer Programming Input/Disable.
8	$\overline{\text{CHG}}$	LED Charge-Status Indicator. This is an open-collector output.

TYPICAL PERFORMANCE CHARACTERISTICS
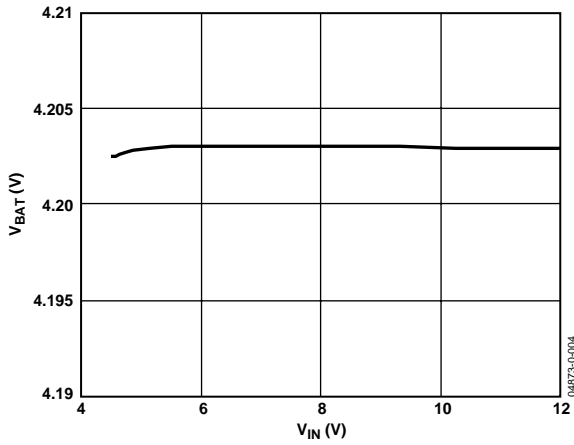
Figure 4. Battery Voltage vs. Input Voltage
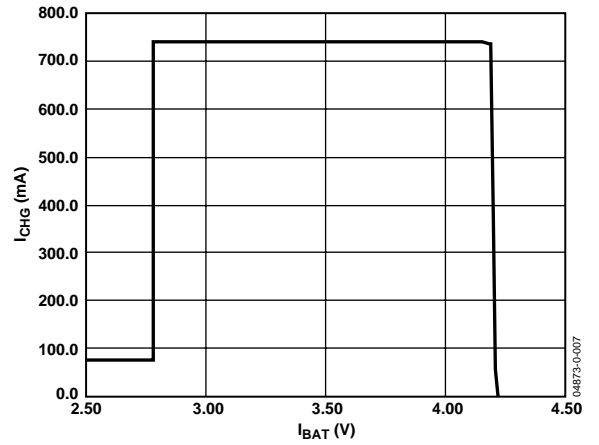
Figure 7. Charge Current vs. Battery Voltage,
$RS = 200\ m\Omega$, $V_{ADJ} = 3\ V$
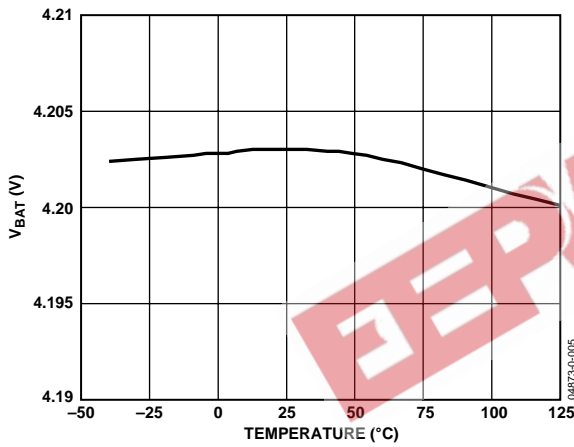
Figure 5. Battery Voltage vs. Temperature
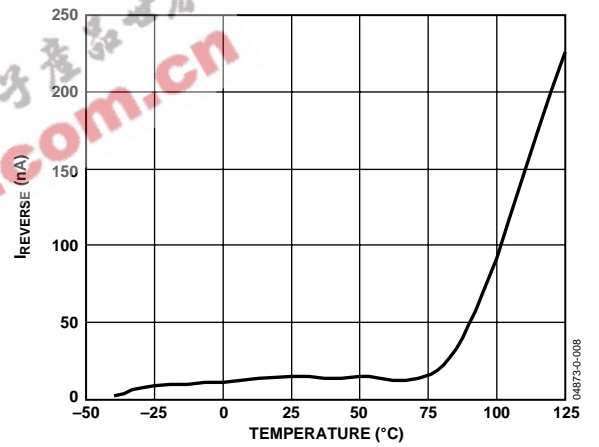
Figure 8. Battery Reverse Current vs. Temperature
$V_{IN} = float$, $V_{BAT} = 4.2\ V$
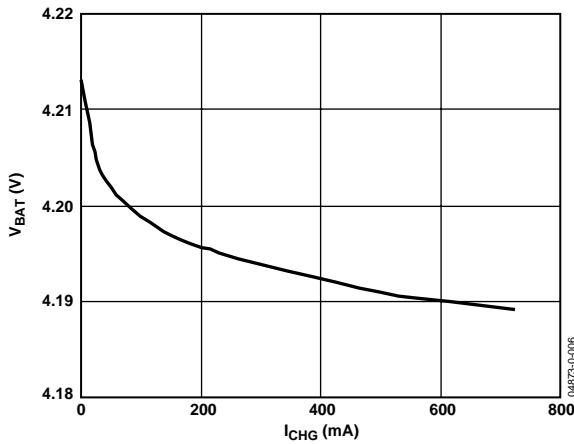
Figure 6. Battery Voltage vs. Charge Current,
$RS = 200\ m\Omega$, $V_{ADJ} = 3\ V$
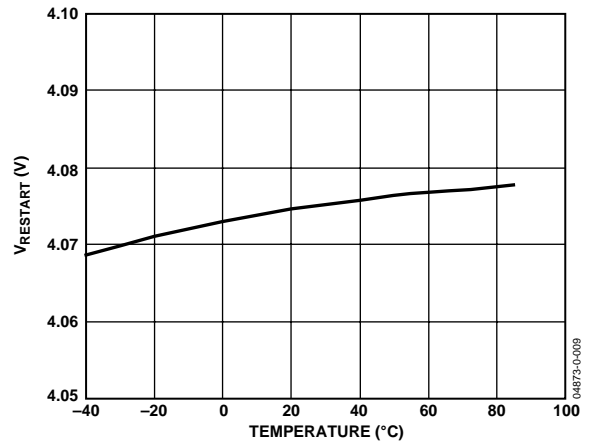
Figure 9. Restart Threshold
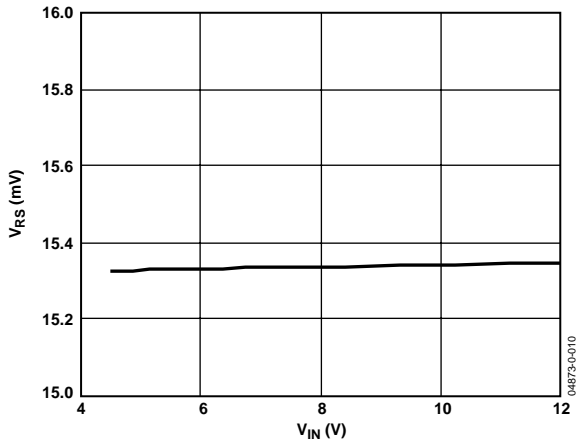
Figure 10. Precharge V$_{RS}$ vs. Input Voltage
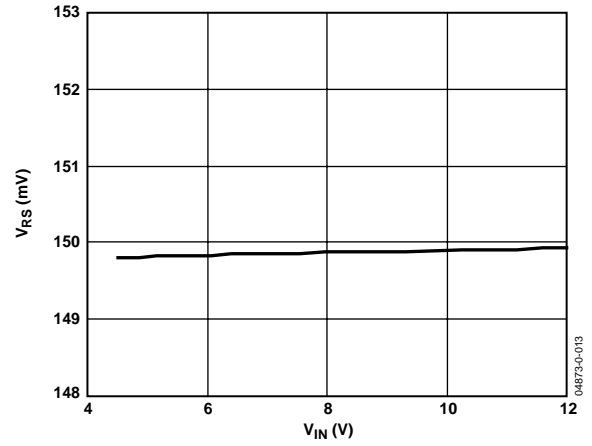
Figure 13. Fast Charge V$_{RS}$ vs. Input Voltage
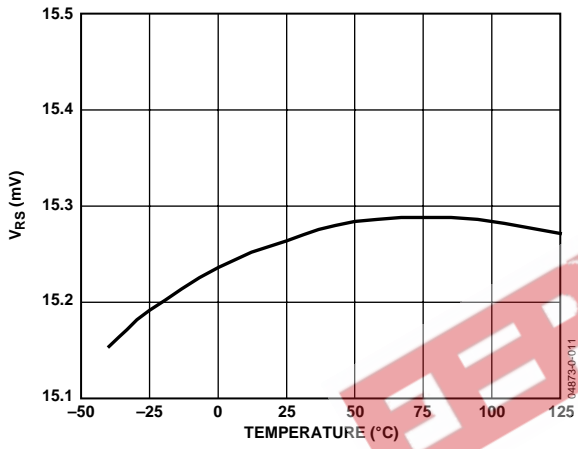
Figure 11. Precharge V$_{RS}$ vs. Temperature
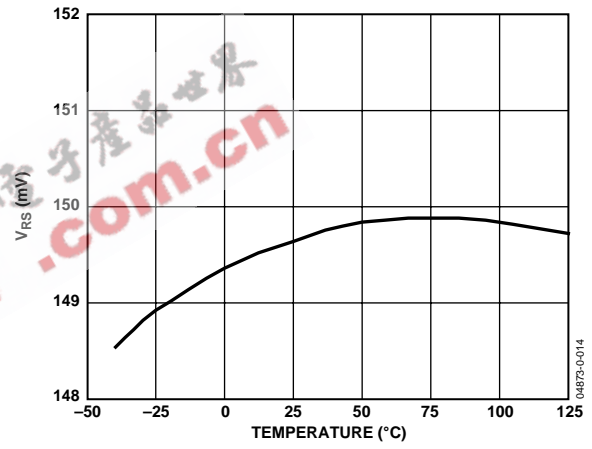
Figure 14. Fast Charge V$_{RS}$ vs. Temperature
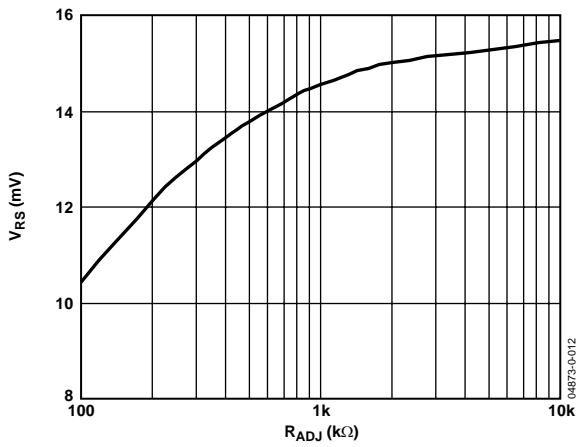
Figure 12. Precharge V$_{RS}$ vs. R$_{ADJ}$
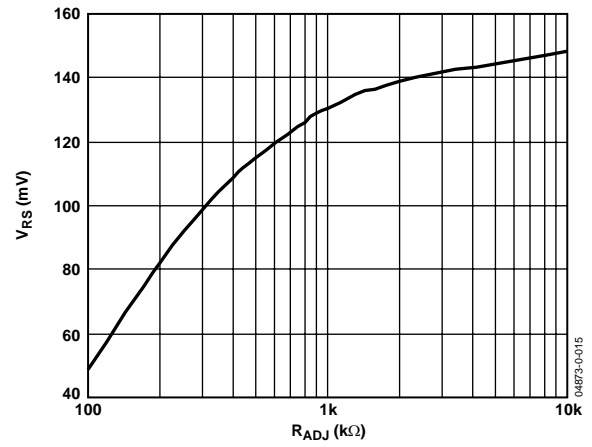
Figure 15. Fast Charge V$_{RS}$ vs. R$_{ADJ}$
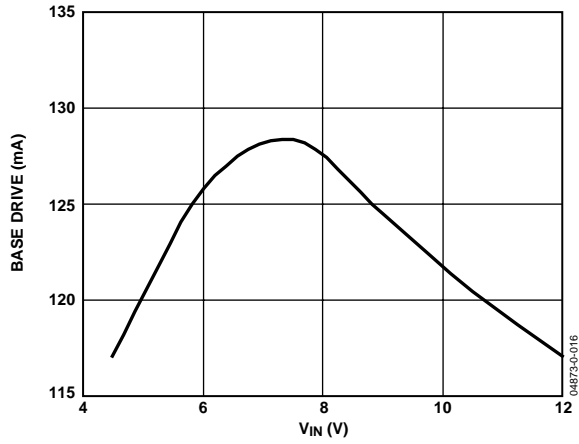
Figure 16. Base Drive vs. Input Voltage
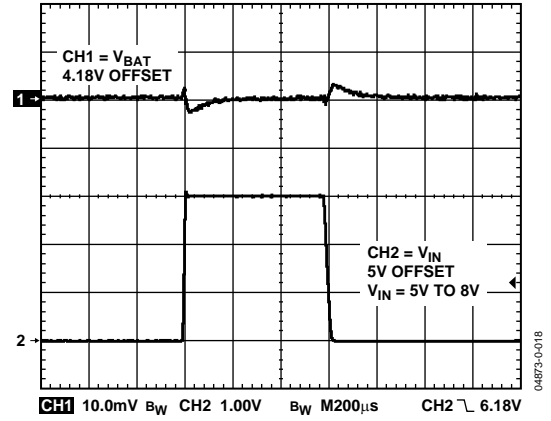
Figure 18. Line Transient Response
I_{BAT} = 350 mA
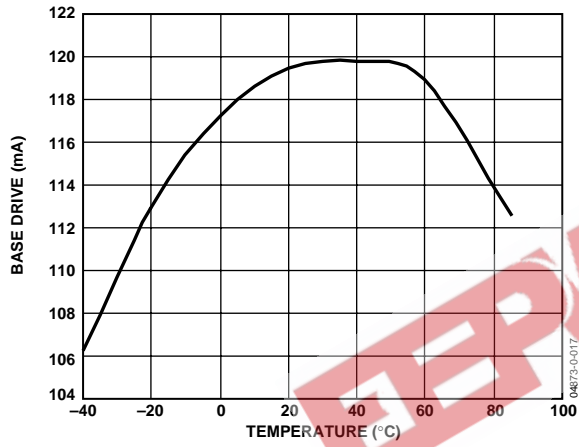
Figure 17. Base Drive vs. Temperature
V_{IN} = 5 V
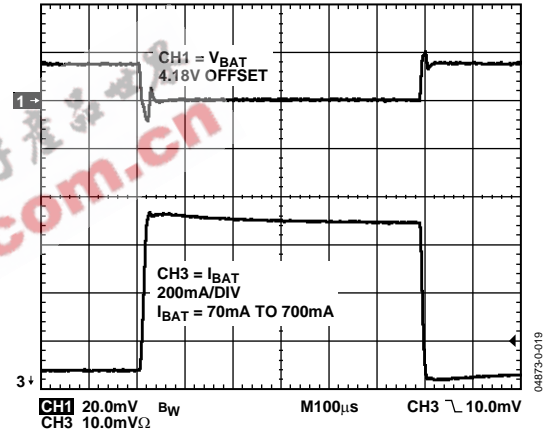
Figure 19.Load Transient Response
V_{IN} = 5 V

THEORY OF OPERATION

The ADP2291 is intended to charge a single cell, lithium battery from a supply voltage or wall adapter providing 4.5 V to 12 V. The charge controller adjusts the base current of an external PNP transistor to optimize current and voltage applied to the battery during charging. A low value resistor placed in series with the battery charging current provides current measurement for the ADP2291.

To assure safety and long battery lifetime, the ADP2291 charges the battery using a simple step-by-step cycle, as shown in the state diagram of Figure 26. The normal charge cycle begins by measuring the battery voltage to determine charge level. If the battery is deeply discharged, then low current precharge is initiated. Once precharge is complete, normal fast charge at the maximum current (denoted as I_{MAX}) begins. This maximum current can be adjusted by varying the sense resistor value or by varying the voltage at the adjust pin. As the battery approaches full capacity, the charging current is reduced until the end-of-charge condition is reached. Batteries that are not deeply discharged skip the precharge mode and immediately begin fast charging. Each of these modes and associated fault conditions are discussed in detail.

PRECHARGE MODE

For deeply-discharged cells, the ADP2291 charges at a reduced rate when the battery voltage $V_{BAT} < 2.8$ V. This reduced rate is $I_{MAX}/10$ when the ADJ pin voltage is 3 V, and $I_{MAX}/5$ when the ADJ pin voltage is 1.5 V. For ADJ pin voltages in between, the charge current can be interpolated. If the battery voltage does not increase past 2.8 V before the precharge timer elapses (typically 30 minutes), a battery fault is assumed and the ADP2291 shuts down and does not restart until the input voltage is cycled OFF and then back ON. Note that in this mode shutdown commands are ignored.

END-OF-CHARGE MODE

Once the voltage loop reduces the charge current to 1/10 of its nominal value, I_{MAX} (irrespective of the ADJ voltage), the ADP2291 detects the end-of-charge (EOC) state and the charge status indicator becomes high-impedance.

Low level charging continues until the timer terminates the charge (nominally 30 minutes).

SHUTDOWN MODE

When the ADJ input is pulled below 0.4 V, the ADP2291 is put into shutdown mode. When in this mode, the charger is disabled, the current drawn from the battery falls to less than 1 μA and the current drawn from IN falls to 0.7 mA.

When the charger is re-enabled, the charger returns to the START state but quickly sequences through the states until the proper charge mode is reached.

CHARGE RESTART

Once charge is complete in end-of-charge or timeout modes, the ADP2291 continually monitors the cell voltage and charge current. When the cell voltage falls by 100 mV or the charge current increases beyond the EOC hysteresis, the ADP2291 initiates another charge cycle to keep the cell fully charged. See the state diagram in Figure 26.

PROGRAMMABLE TIMER

The on-chip timer, controlled by an external capacitor CTIMER, determines the timeout intervals of the various charger modes. For example, a CTIMER value of 0.1 μF results in a precharge timeout interval of 30 minutes, a fast charge timeout of 3 hours, and an end-of-charge timeout of 30 minutes. The ratio between precharge and end-of-charge to fast charge time-out is always 1/6. All these time intervals are proportional to the CTIMER capacitor value, allowing them to be adjusted over a wide range. Connecting the TIMER pin to ground disables the timer.

CHARGE STATUS INDICATOR

The ADP2291 contains a charge status output, $\overline{CHG}$, that sinks current when the ADP2291 is charging the battery. This output can be used as a visual signal by connecting it to an LED, or it may be used to generate a logic-level charge status signal by connecting a resistor between $\overline{CHG}$ and logic high.

AUTOMATIC REVERSE ISOLATION

When the voltage on the BAT pin is higher than the voltage on IN, the ADP2291 automatically connects the base of the pass device to BAT. This removes the necessity of having an external diode between the pass device and battery, further reducing the charger's footprint and component count.

OVERSHOOT PROTECTION

In the event of a battery disconnect during charging, a voltage overshoot condition on BAT could occur. The ADP2291 includes an overshoot protection circuit that activates when V_{BAT} rises to 5 V and sinks up to 1.5 A to protect the external components.

POWER SUPPLY CHECKS

To assure proper operation, the ADP2291 checks the absolute voltage level of the input supply and the supply voltage relative to the battery. When the supply IN is below 3.8 V, the chip is internally powered down and does not respond to external control. In this power-down mode, the device draws less than 1 μA from the battery. The V_{IN} good comparator halts operation if the supply voltage is less than 165 mV above the battery voltage, insuring that charging only occurs if the supply voltage is sufficient.

THERMAL SHUTDOWN

In the event that the ADP2291 junction temperature rises above 135°C, thermal shutdown occurs. Extreme junction temperatures may be the result of excessive current operation and/or high ambient temperatures. A 35°C temperature hysteresis is included so that the ADP2291 does not return to operation during thermal shutdown until the on-chip temperature drops below 100°C.
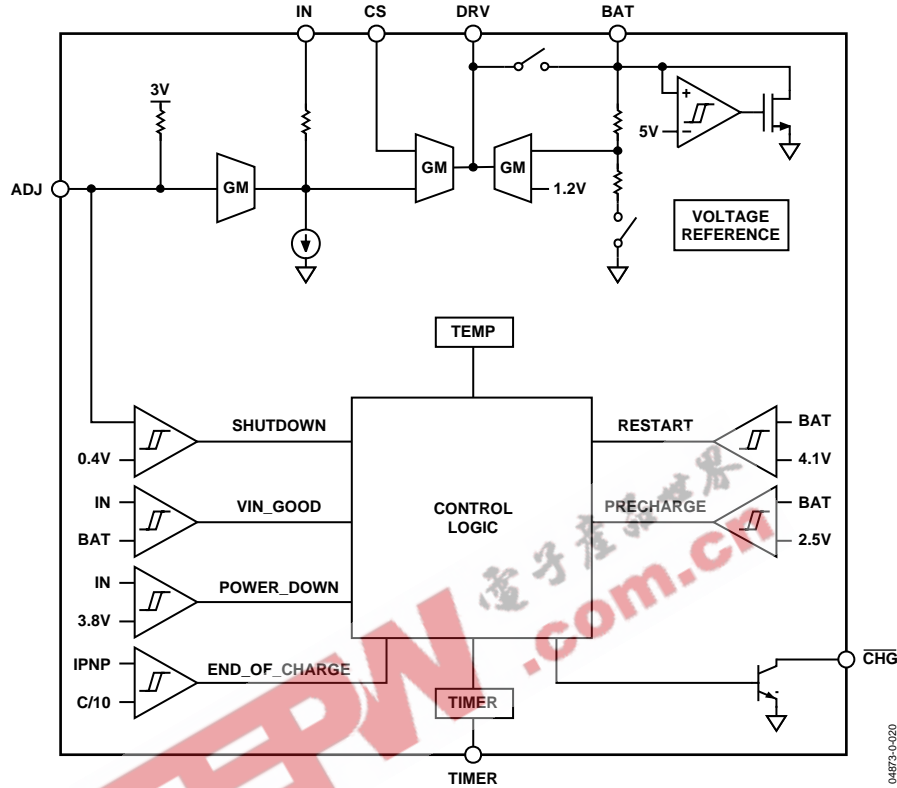

Figure 20. Functional Block Diagram

APPLICATION INFORMATION

SETTING THE MAXIMUM CHARGE CURRENT

The maximum charge current is set by choosing the proper current sense resistor, RS, and the voltage on the ADJ input. The charger nominally regulates its output current at the point where the voltage across the current sense resistor $V_{IN}-V_{CS}$ (defined as V_{RS}) is 150 mV. This setpoint voltage can be adjusted by pulling down on the ADJ input, which is internally attached through a 100 kΩ pull-up resistor to 3 V. Each volt of pull-down from 3 V will reduce V_{RS} by 67 mV during fast charge. A minimum of 50 mV is reached when a 100 kΩ resistor is attached between ADJ and ground. During slow charge the voltage across the current sense resistor is 15 mV with no connection to ADJ and drops to 10 mV with a 100 kΩ resistor attached to ground. Therefore the maximum charge rate I_{MAX} can be calculated as

$$I_{MAX} = \frac{V_{RS}(\text{mV})}{R_S(\text{m}\Omega)} \qquad (1)$$

where 50 mV ≤ V_{RS} ≤ 150 mV

After determining suitable values for V_{RS} and R_S, the value of V_{ADJ} and R_{ADJ} can be calculated as

$$V_{ADJ} = \frac{V_{RS}(\text{mV}) + 50\text{ mV}}{66.7\text{ mV}} V \qquad (2)$$

$$R_{ADJ} = 100\text{ k}\Omega \times \left(\frac{V_{ADJ}}{3V - V_{ADJ}}\right) \qquad (3)$$

Examples of resistor combinations are shown in Table 4.

Table 4. Examples of R$_S$ and R$_{ADJ}$ Selection

I$_{MAX}$	R$_S$	V$_{RS}$	V$_{ADJ}$	R$_{ADJ}$
1.5 A	100 mΩ	150 mV	3 V	Open
1 A	100 mΩ	100 mV	2.25 V	300 K
750 mA	100 mΩ	75 mV	1.87 V	167 K
500 mA	100 mΩ	50 mV	1.5 V	100 K
750 mA	200 mΩ	150 mV	3 V	Open
500 mA	200 mΩ	100 mV	2.25 V	300 K
375 mA	200 mΩ	75 mV	1.87 V	167 K
250 mA	200 mΩ	50 mV	1.5 V	100 K
500 mA	300 mΩ	150 mV	3 V	Open
333 mA	300 mΩ	100 mV	2.25 V	300 K
250 mA	300 mΩ	75 mV	1.87 V	167 K
167 mA	300 mΩ	50 mV	1.5 V	100 K

SETTING THE MAXIMUM CHARGE TIME

The maximum charge time is intended as a safety mechanism to prevent the charger from trickle charging the cell indefinitely. It does not terminate charging under normal charging conditions, but only when there is a failure to reach end-of-charge. A typical cell charges at a 1 C rate in about 1.5 hours, depending on the cell type, temperature, and manufacturer. Generally, a three hour time limit is sufficient to prevent a normal charge cycle from being interrupted by the charge timer. It is recommended that the cell manufacturer be consulted for timing details.

The maximum charge time is set by selecting the value of the CTIMER capacitor. Calculate the timer capacitance using

$$CTIMER = t_{CHG}(\text{minutes}) \times \frac{1\,\mu F}{1800\,\text{minutes}} \qquad (4)$$

The precharge and end-of-charge periods are 1/6 the duration of the fast charge time limit. The charge timers are completely disabled by connecting the TIMER pin to ground. If the timers are disabled, the FAULT and TIMEOUT states are never reached, so the timers should only be disabled if charging is monitored and controlled externally.

EXTERNAL CAPACITORS

Use an input supply capacitor (CIN) with a value in the 1 μF to 10 μF range and place it close to the ADP2291. This should provide adequate input bypassing, but the selected capacitor should be checked in the actual application circuit. Check that the input voltage does not droop or overshoot excessively during the start-up transient.

Use a battery output capacitor (COUT) with a value of at least 10 μF. This capacitance provides compensation when no battery load is present. In addition, the battery and interconnections appear inductive at high frequencies and must be accounted for when the charger is operated with a battery load. Therefore, a small amount of output capacitance is necessary to compensate for the inductive nature of the battery and connections. Use a minimum output capacitance value of 1 μF for applications where the battery cannot be removed.

REVERSE INPUT PROTECTION

The diode, D1, shown in Figure 22 through Figure 25 is optional. It is only required if the input adapter voltage can be applied with a reverse polarity.

If the adapter voltage is high enough, a Schottky diode is recommended to minimize the voltage difference from the adapter to the charger input and the power dissipation. Choose a diode with a continuous current rating high enough to handle battery charging current at the maximum ambient temperature. Use a diode whose voltage rating is greater than the maximum adapter voltage.

In cases where the voltage drop across the protection device must be kept low, a P MOSFET is recommended. Connect the MOSFET as shown in Figure 21.
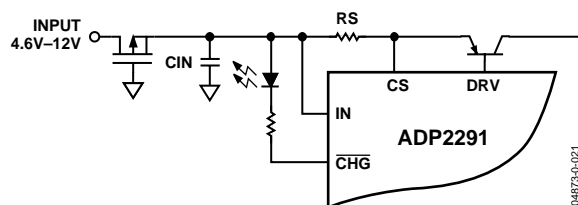

Figure 21. Reverse Input Protection

EXTERNAL PASS TRANSISTOR

Choose the external PNP pass transistor based on the given operating conditions and power handling capabilities. The pass device is determined by the base drive available, the input and output voltage, and the maximum charge current.

Select the pass transistor with a collector-emitter breakdown voltage that exceeds the maximum adapter voltage. A V_{CEO} rating of at least 15 V is recommended.

To provide a charge current of I_{MAX} with a minimum base drive of 40 mA requires a PNP beta of at least

$$\beta_{MIN} = \frac{I_{MAX}}{I_B} = \frac{I_{MAX}}{40mA} \tag{5}$$

Note that the beta of a transistor drops off with collector current. Therefore, make sure the beta at I_{MAX} meets the minimum requirement.

For cases where the adapter voltage is low (less than 5.5 V) calculate the saturation voltage using the following equation:

$$V_{CE(SAT)} = V_{ADAPTER(MIN)} - V_{PROTECT} - V_{RS} - V_{BAT} \tag{6}$$

where $V_{PROTECT}$ = the forward drop of the reverse input protection.

The power handling capabilities of the PNP pass transistor is another important parameter. The maximum power dissipation of the pass transistor is estimated using

$$P_{DISS}(W) = I_{MAX} \times (V_{ADAPTER(MAX)} - V_{PROTECT} - V_{RS} - V_{BAT}) \tag{7}$$

where V_{RS} = 150 mV *at* V_{ADJ} = 3.0 V
= 50 mV *at* V_{ADJ} = 1.5 V
V_{BAT} = 2.8 V, the lowest cell voltage where fast charge can occur

It should be noted that the adapter voltage can be either pre-regulated or unregulated. In the preregulated case the difference between the maximum and minimum adapter voltage is small. In this case use the maximum regulated adapter voltage to determine the maximum power dissipation. In the unregulated case, the adapter voltage can have a wide range specified. However, the maximum voltage specified is usually with no load applied. Therefore, the worst-case power dissipation calculation often leads to an over-specified pass device. In either case, it is best to determine the load characteristics of the adapter to optimize the charger design.

For example:

$V_{ADAPTER(MIN)}$ = 5.0 V
$V_{ADAPTER(MAX)}$ = 6.0 V
I_{MAX} = 500 mA
$V_{PROTECT}$ = 0.2 V *at* 500 mA
V_{ADJ} = 3 V
V_{RS} = 150 mV

$$\beta_{MIN} = \frac{I_{MAX}}{I_B} = \frac{500mA}{40mA} = 12.5$$

$V_{CE(SAT)} = V_{ADAPTER(MIN)} - V_{PROTECT} - V_{RS} - V_{BAT}$
= 5.0 V − 0.2 V − 0.15 V − 4.2 V
= 0.45 V

$P_{DISS}(W) = I_{MAX} \times (V_{ADAPTER(MAX)} - V_{PROTECT} - V_{RS} - V_{BAT})$
= 0.50 A × (6.0 V − 0.2 V − 0.15 V − 2.8 V)
= 1.4 W

A guide for selecting the PNP transistor is given in Table 5.

Table 5. PNP Pass Transistor Selection Guide

Vendor	Part Number	Package	Max PD@ 25°C	Beta @1A	VCE (SAT)
Fairchild	FSB6726	SuperSOT	0.5 W	150	0.5 V
	NZT45H8	SOT223	1.5 W	110	0.1 V
ON Semi	MTB35200	TSOP-6	0.625 W	200	0.175 V
	BCP53T1	SOT223	1.5 W	35	0.3 V
	MMJT9435	SOT223	1.6 W	200	0.18 V
Philips	BCP51	SOT223	1.3 W	50	0.5 V
ZETEX	ZXT10P20DE6	SOT23-6	1.1 W	270	0.17 V
	ZXT2M322	2 mm × 2 mm MLP	1.5 W	270	0.17 V
	FZT549	SOT223	2 W	130	0.25 V
	FMMT549	SOT23	0.5 W	130	0.25 V

TYPICAL APPLICATION CIRCUIT

A typical application circuit is shown in Figure 22. The circuit is capable of a 750 mA charge current for an input voltage of 4.5 V to 6 V. Higher input voltages can be used, but the increased power dissipation of the pass device must be taken into account.
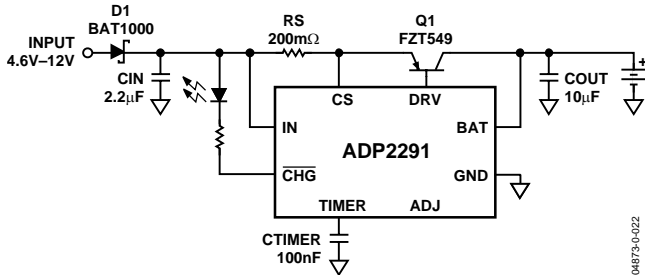

Figure 22. Typical Application Circuit

EOC TERMINATES CHARGING

In some applications, the charger is required to terminate charging when the EOC threshold is reached. Automatic charger restart is not desired. Adding components R1, C1, and Q2 terminates charging when the $\overline{CHG}$ pin opens and prevents further charging until the adapter is removed and reasserted.
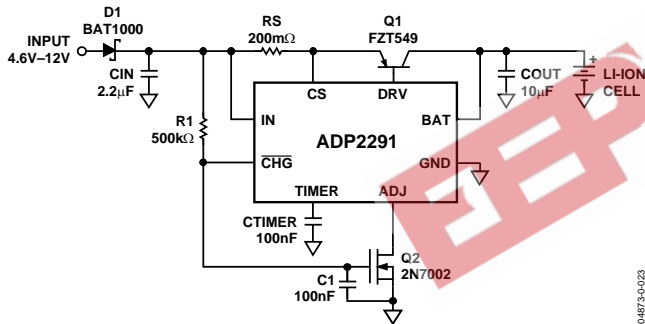

Figure 23. Self-Termination Circuit

SELECTABLE CHARGE CURRENT

In applications where the charge current needs to be selectable, use the circuit shown in Figure 24. This circuit allows a processor to determine if the charge current needs to be reduced due to an input source limitation or a different battery capacity option, or simply to reduce the stress on the pass transistor. R2 and Q2 allow the charge current to be selected between HIGH—750 mA, and LOW—250 mA.
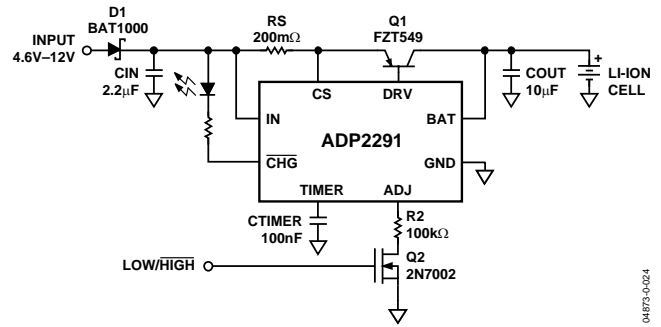
Figure 24. Selectable Charge Current Circuit

THERMAL PROTECTION

In applications where the overall size must be small or the input voltage range is wide, adding thermal regulation is suggested. This allows the charger to monitor the temperature of the pass device and decrease the charge current as the temperature increases. By adding a NTC thermistor to the ADJ pin it is possible to accomplish this; however, care is still required to ensure that the power dissipation of the pass device is not exceeded.
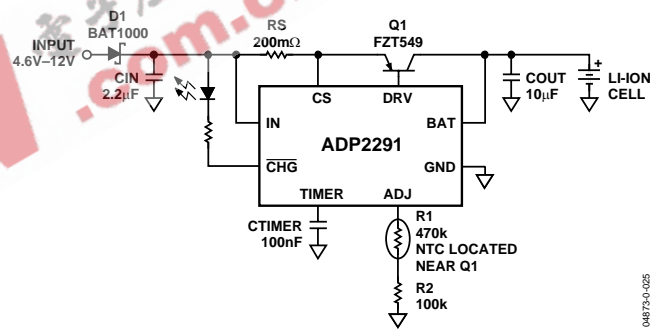
Figure 25. Thermal Regulation Circuit

Some suggested NTC thermistor suppliers are listed in Table 6.

Table 6. NTC Thermistor Manufacturers

Vendor	Part Number	Website
BetaTherm	SMD2500KJ435J	www.betatherm.com
Murata	NCP18WM474J	www.murata .com
Panasonic	ERTJ0EV474J	www.panasonic.com
Vishay	2322 615 1.474	www.vishay.com

Figure 26. State Diagram for the ADP2291,
CTIMER = 0.1μF

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Use the following general guidelines when designing printed circuit boards:

- Keep the output capacitor as close to the BAT and GND pins as possible.
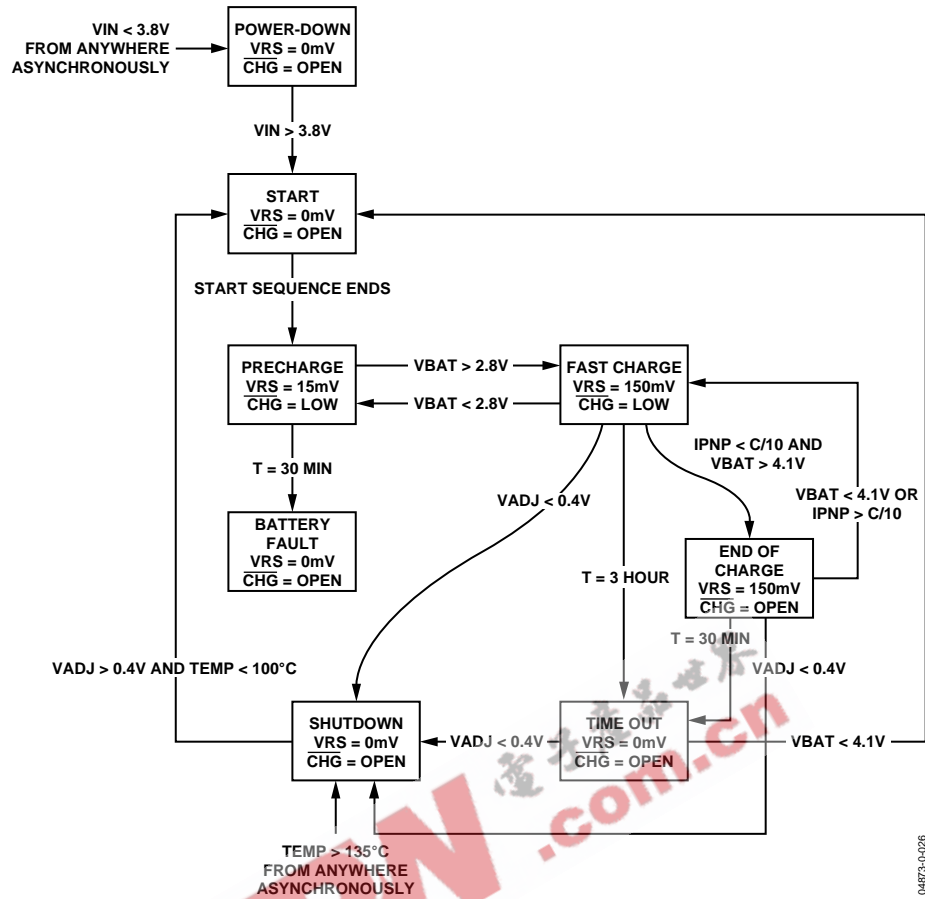
- Keep the input capacitor as close to the IN and GND pins as possible.

- PC board traces with larger cross-sectional areas remove more heat from the pass transistor. For optimum heat transfer, specify thick copper and use wide traces.

- Use additional copper layers or planes to reduce the thermal resistance. When connecting to other layers, use multiple vias if possible.

LFSCP LAYOUT CONSIDERATIONS

The CSP package has an exposed die paddle on the bottom that efficiently conducts heat to the PCB. In order to achieve the optimum performance from the CSP package, give special consideration to the layout of the PCB. Use the following layout guidelines for the CSP package:

- The pad pattern is shown in Figure 27. Follow the pad dimension closely for reliable solder joints while maintaining reasonable clearances to prevent solder bridging.

- The thermal pad of the CSP package provides a low thermal impedance path (approximately 20°C/W) to the PCB. Therefore a properly designed PCB effectively conducts the heat away from the package. This is achieved by adding thermal vias to the PCB that provide a thermal path to the inner or bottom layers. Note that the via diameter is small to prevent the solder from flowing through the via and leaving voids in the thermal pad solder joint.

Note that the thermal pad is attached to the die substrate, so the thermal planes that the vias attach the package to must be electrically isolated or connected to GND.

- The solder mask opening should be about 120 microns (4.7 mils) larger than the pad size, resulting in a minimum of 60 microns (2.4 mils) clearance between the pad and the solder mask.

- The paste mask opening is typically designed to match the pad size used on the peripheral pads of the LFCSP package. This should provide a reliable solder joint as long as the stencil thickness is about 0.125 mm. The paste mask for the thermal pad needs to be designed for the maximum coverage to effectively remove the heat from the package. However, due to the presence of thermal vias and the size of the thermal pad, eliminating voids may not be possible.

- The recommended paste mask stencil thickness is 0.125 mm. Use a laser cut stainless steel stencil with trapezoidal walls.

- Use a no clean, Type 3 solder paste for mounting the LFCSP package. A nitrogen purge during the reflow process is recommended.

- The package manufacturer recommends that the reflow temperature not exceed 220°C and the time above liquidus is less than 75 seconds. Make sure the preheat ramp is 3°C/second or lower. The actual temperature profile depends on the board's density and should be determined by the assembly house.

Figure 27. 3 mm × 3 mm LFCSP Pad Pattern
(Dimensions in mm)

Table 7. Variables Description

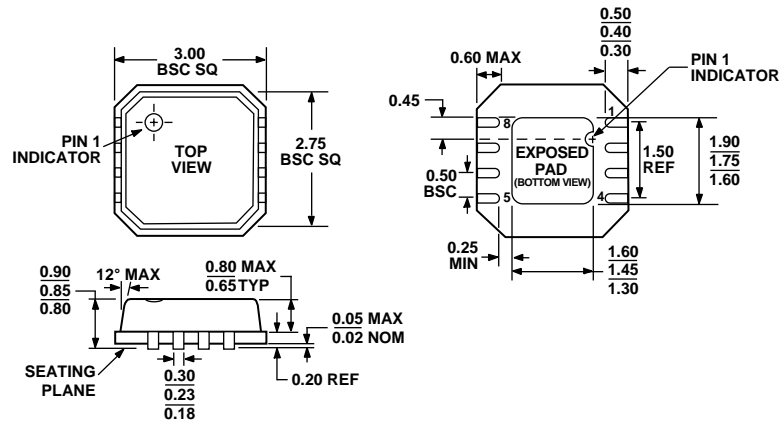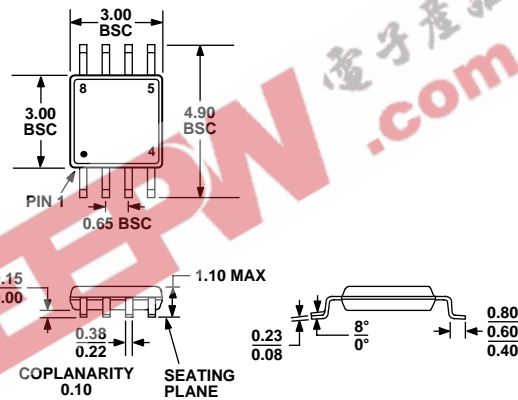| Variable Name	Description
V_X	The voltage on Pin X
V_{RS}	The regulation setpoint for the voltage across the sense resistor (RS)
$V_{BAT,\ EOC}$	The battery voltage at the point charging current is 1/10 the current setpoint
I_{MAX}	The charge current corresponding to VRS, including the effects of ADJ pin voltage
I_{MAX0}	The charge current corresponding to the VRS setpoint, ignoring ADJ effects (i.e. C0 = 150 mV/RS)
C rate	The charge current (mA) expressed as a multiple of the nominal battery capacity (mAh). A 900 mAh capacity battery charged at a 1/10 C rate, is equivalent to a 90 mA charge current.

OUTLINE DIMENSIONS

Figure 28. 8-lead 3 × 3 LFCSP Package
(CP-8)
Dimensions Shown in Millimeters

COMPLIANT TO JEDEC STANDARDS MO-187AA

Figure 29. 8-Lead MSOP Package
(RM-8)
Dimensions Shown in Millimeters

ORDERING GUIDE

Models	Temperature Range	Package Description	Package Option	Branding
ADP2291ARMZ-R7[1]	−40°C to +85°C	8-Lead MSOP	RM-8	P08
ADP2291ACPZ-R7[1]	−40°C to +85°C	8-Lead LFCSP	CP-8	P08

[1] Z = Pb-free part.

NOTES

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ANALOG DEVICES

www.analog.com