

74VCX16245

Low-Voltage 1.8/2.5/3.3V 16-Bit Transceiver

With 3.6 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The 74VCX16245 is an advanced performance, non-inverting 16-bit transceiver. It is designed for very high-speed, very low-power operation in 1.8 V, 2.5 V or 3.3 V systems.

When operating at 2.5 V (or 1.8 V) the part is designed to tolerate voltages it may encounter on either inputs or outputs when interfacing to 3.3 V busses. It is guaranteed to be overvoltage tolerant to 3.6 V.

The VCX16245 is designed with byte control. It can be operated as two separate octals, or with the controls tied together, as a 16-bit wide function. The Transmit/Receive ($T/\bar{R}n$) inputs determine the direction of data flow through the bi-directional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B to A ports. The Output Enable inputs (\overline{OEn}), when HIGH, disable both A and B ports by placing them in a HIGH Z condition.

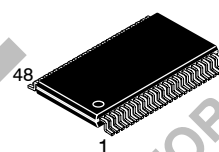
Features

- Designed for Low Voltage Operation: $V_{CC} = 1.65\text{--}3.6\text{ V}$
- 3.6 V Tolerant Inputs and Outputs
- High Speed Operation: 2.5 ns max for 3.0 to 3.6 V
3.0 ns max for 2.3 to 2.7 V
6.0 ns max for 1.65 to 1.95 V
- Static Drive: $\pm 24\text{ mA}$ Drive at 3.0 V
 $\pm 18\text{ mA}$ Drive at 2.3 V
 $\pm 6\text{ mA}$ Drive at 1.65 V
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0\text{ V}$
- Near Zero Static Supply Current in All Three Logic States (20 μA)
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds $\pm 250\text{ mA}$ @ 125°C
- ESD Performance: Human Body Model >2000 V;
Machine Model >200 V



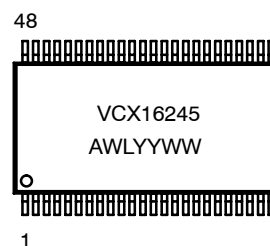
ON Semiconductor®

<http://onsemi.com>



TSSOP-48
DT SUFFIX
CASE 1201

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
74VCX16245DT	TSSOP	39 / Rail
74VCX16245DTR	TSSOP	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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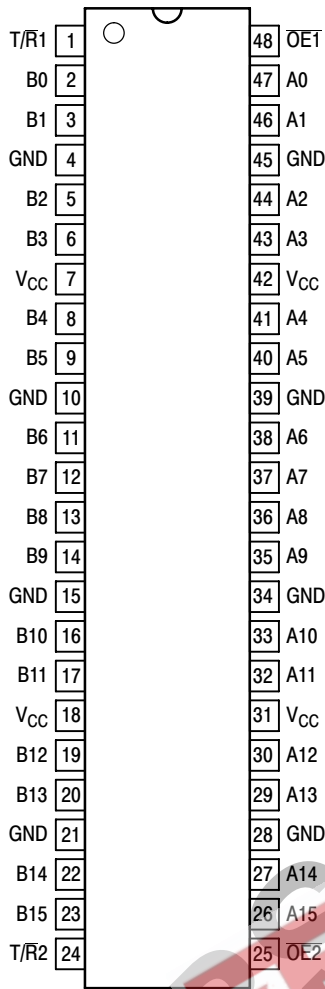


Figure 1. 48-Lead Pinout (Top View)

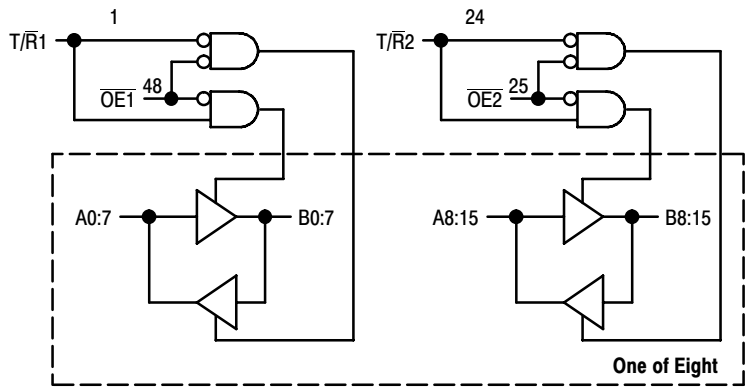


Figure 2. Logic Diagram

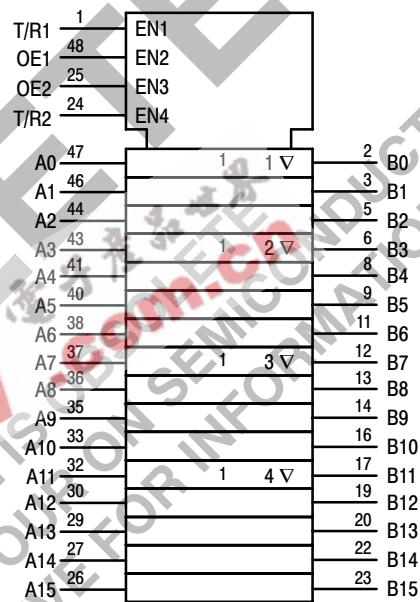


Figure 3. IEC Logic Diagram

Table 1. PIN NAMES

Pins	Function
OE \bar{n} T/R \bar{n} A0–A15 B0–B15	Output Enable Inputs Transmit/Receive Inputs Side A Inputs or 3-State Outputs Side B Inputs or 3-State Outputs

TRUTH TABLE

Inputs		Outputs	Inputs		Outputs
OE1	T/R1		OE2	T/R2	
L	L	Bus B0:7 Data to Bus A0:7	L	L	Bus B8:15 Data to Bus A8:15
L	H	Bus A0:7 Data to Bus B0:7	L	H	Bus A8:15 Data to Bus B8:15
H	X	High Z State on A0:7, B0:7	H	X	High Z State on A8:15, B8:15

H = High Voltage Level

L = Low Voltage Level

X = High or Low Voltage Level and Transitions Are Acceptable

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	-0.5 to +4.6		V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq +4.6$		V
V_O	DC Output Voltage	$-0.5 \leq V_O \leq +4.6$	Output in 3-State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$	Note 1; Outputs Active	V
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	± 50		mA
I_{CC}	DC Supply Current Per Supply Pin	± 100		mA
I_{GND}	DC Ground Current Per Ground Pin	± 100		mA
T_{STG}	Storage Temperature Range	-65 to +150		$^{\circ}C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V_{CC}	Supply Voltage	Operating	1.65	3.3	3.6	V
		Data Retention Only	1.2	3.3	3.6	
V_I	Input Voltage	-0.3		3.6	V	
V_O	Output Voltage	(Active State)	0	V_{CC}	V	
		(3-State)	0	3.6		
I_{OH}	HIGH Level Output Current, $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$			-24	mA	
I_{OL}	LOW Level Output Current, $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$			24	mA	
I_{OH}	HIGH Level Output Current, $V_{CC} = 2.3\text{ V} - 2.7\text{ V}$			-18	mA	
I_{OL}	LOW Level Output Current, $V_{CC} = 2.3\text{ V} - 2.7\text{ V}$			18	mA	
I_{OH}	HIGH Level Output Current, $V_{CC} = 1.65\text{ V} - 1.95\text{ V}$			-6	mA	
I_{OL}	LOW Level Output Current, $V_{CC} = 1.65\text{ V} - 1.95\text{ V}$			6	mA	
T_A	Operating Free-Air Temperature	-40		+85	$^{\circ}C$	
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, $V_{CC} = 3.0\text{ V}$	0		10	ns/V	

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DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Unit
			Min	Max	
V _{IH}	HIGH Level Input Voltage (Note 2)	1.65 V ≤ V _{CC} < 2.3 V	0.65 × V _{CC}		V
		2.3 V ≤ V _{CC} ≤ 2.7 V	1.6		
		2.7 V < V _{CC} ≤ 3.6 V	2.0		
V _{IL}	LOW Level Input Voltage (Note 2)	1.65 V ≤ V _{CC} < 2.3 V		0.35 × V _{CC}	V
		2.3 V ≤ V _{CC} ≤ 2.7 V		0.7	
		2.7 V < V _{CC} ≤ 3.6 V		0.8	
V _{OH}	HIGH Level Output Voltage	1.65 V ≤ V _{CC} ≤ 3.6 V; I _{OH} = -100 μA	V _{CC} - 0.2		V
		V _{CC} = 1.65 V; I _{OH} = -6 mA	1.25		
		V _{CC} = 2.3 V; I _{OH} = -6 mA	2.0		
		V _{CC} = 2.3 V; I _{OH} = -12 mA	1.8		
		V _{CC} = 2.3 V; I _{OH} = -18 mA	1.7		
		V _{CC} = 2.7 V; I _{OH} = -12 mA	2.2		
		V _{CC} = 3.0 V; I _{OH} = -18 mA	2.4		
		V _{CC} = 3.0 V; I _{OH} = -24 mA	2.2		
V _{OL}	LOW Level Output Voltage	1.65 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA		0.2	V
		V _{CC} = 1.65 V; I _{OL} = 6 mA		0.3	
		V _{CC} = 2.3 V; I _{OL} = 12 mA		0.4	
		V _{CC} = 2.3 V; I _{OL} = 18 mA		0.6	
		V _{CC} = 2.7 V; I _{OL} = 12 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 18 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 24 mA		0.55	
I _I	Input Leakage Current	1.65 V ≤ V _{CC} ≤ 3.6 V; 0 V ≤ V _I ≤ 3.6 V		±5.0	μA
I _{OZ}	3-State Output Current	1.65 V ≤ V _{CC} ≤ 3.6 V; 0 V ≤ V _O ≤ 3.6 V; V _I = V _{IH} or V _{IL}		±10	μA
I _{OFF}	Power-Off Leakage Current	V _{CC} = 0 V; V _I or V _O = 3.6 V		10	μA
I _{CC}	Quiescent Supply Current (Note 3)	1.65 V ≤ V _{CC} ≤ 3.6 V; V _I = GND or V _{CC}		20	μA
		1.65 V ≤ V _{CC} ≤ 3.6 V; 3.6 V ≤ V _I , V _O ≤ 3.6 V		±20	μA
ΔI _{CC}	Increase in I _{CC} per Input	2.7 V < V _{CC} ≤ 3.6 V; V _{IH} = V _{CC} - 0.6 V		750	μA

2. These values of V_I are used to test DC electrical characteristics only.
 3. Outputs disabled or 3-state only.

AC CHARACTERISTICS (Note 4; t_R = t_F = 2.0 ns; C_L = 30 pF; R_L = 500 Ω)

Symbol	Parameter	Waveform	T _A = -40°C to +85°C						Unit
			V _{CC} = 3.0 V to 3.6 V		V _{CC} = 2.3 V to 2.7 V		V _{CC} = 1.65 V to 1.95 V		
			Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay Input-to-Output	1	0.8	2.5	1.0	3.0	1.5	6.0	ns
			0.8	2.5	1.0	3.0	1.5	6.0	
t _{PZH} t _{PZL}	Output Enable Time to High and Low Level	2	0.8	3.8	1.0	4.9	1.5	9.3	ns
			0.8	3.8	1.0	4.9	1.5	9.3	
t _{PHZ} t _{PLZ}	Output Disable Time From High and Low Level	2	0.8	3.7	1.0	4.2	1.5	7.6	ns
			0.8	3.7	1.0	4.2	1.5	7.6	
t _{OSSL} t _{OSLH}	Output-to-Output Skew (Note 5)			0.5		0.5		0.75	ns
				0.5		0.5		0.75	

4. For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.
 5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

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AC CHARACTERISTICS ($t_R = t_F = 2.0$ ns; $C_L = 50$ pF; $R_L = 500$ Ω)

Symbol	Parameter	Waveform	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				Unit
			$V_{CC} = 3.0$ V to 3.6V		$V_{CC} = 2.7$ V		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Input-to-Output	3	1.0 1.0	3.0 3.0		3.6 3.6	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	4	1.0 1.0	4.4 4.4		5.4 5.4	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	4	1.0 1.0	4.1 4.1		4.6 4.6	ns
t_{OSHL} t_{OSLH}	Output-to-Output Skew (Note 6)			0.5 0.5		0.5 0.5	ns

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$	Unit
			Typ	
V_{OLP}	Dynamic LOW Peak Voltage (Note 7)	$V_{CC} = 1.8$ V, $C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$ V	0.25	V
		$V_{CC} = 2.5$ V, $C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$ V	0.6	
		$V_{CC} = 3.3$ V, $C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$ V	0.8	
V_{OLV}	Dynamic LOW Valley Voltage (Note 7)	$V_{CC} = 1.8$ V, $C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$ V	-0.25	V
		$V_{CC} = 2.5$ V, $C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$ V	-0.6	
		$V_{CC} = 3.3$ V, $C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$ V	-0.8	
V_{OHV}	Dynamic HIGH Valley Voltage (Note 8)	$V_{CC} = 1.8$ V, $C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$ V	1.5	V
		$V_{CC} = 2.5$ V, $C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$ V	1.9	
		$V_{CC} = 3.3$ V, $C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$ V	2.2	

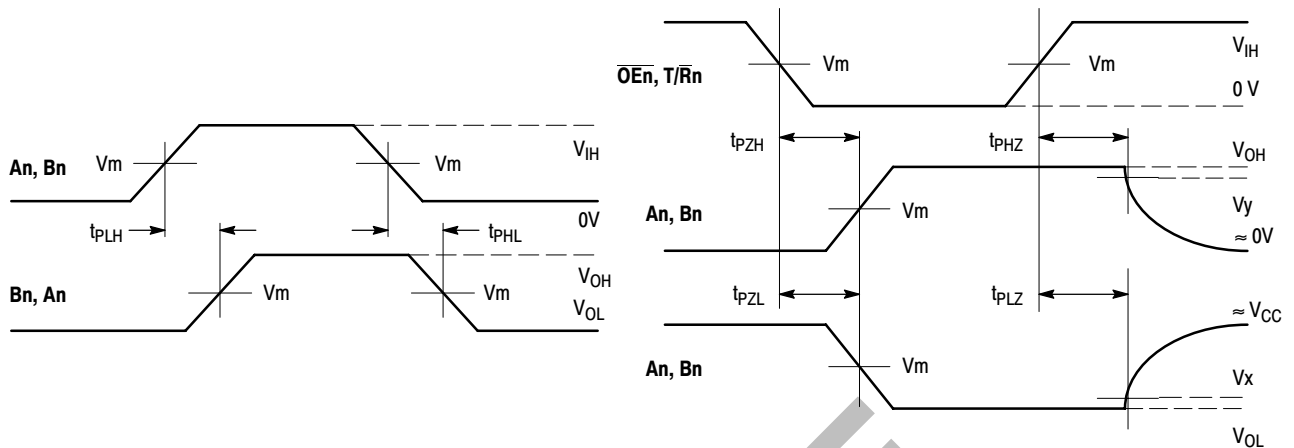
7. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.
8. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the HIGH state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	Note 9	6	pF
C_{OUT}	Output Capacitance	Note 9	7	pF
C_{PD}	Power Dissipation Capacitance	Note 9, 10 MHz	20	pF

9. $V_{CC} = 1.8$ V, 2.5 V or 3.3 V; $V_I = 0$ V or V_{CC} .

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WAVEFORM 1 - PROPAGATION DELAYS
 $t_R = t_F = 2.0$ ns, 10% to 90%; $f = 1$ MHz; $t_W = 500$ ns

WAVEFORM 2 - OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.0$ ns, 10% to 90%; $f = 1$ MHz; $t_W = 500$ ns

Figure 4. AC Waveforms

Table 2. AC WAVEFORMS

Symbol	V _{CC}		
	3.3 V ± 0.3 V	2.5 V ± 0.2 V	1.8 V ± 0.15 V
V _{IH}	2.7 V	V _{CC}	V _{CC}
V _m	1.5 V	V _{CC} /2	V _{CC} /2
V _x	V _{OL} + 0.3 V	V _{OL} + 0.15 V	V _{OL} + 0.15 V
V _y	V _{OH} - 0.3 V	V _{OH} - 0.15 V	V _{OH} - 0.15 V

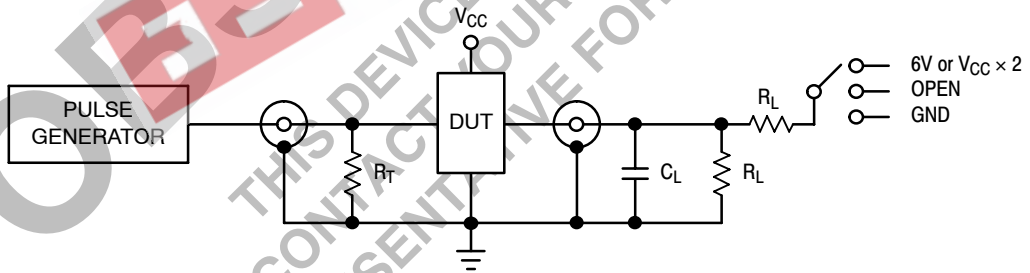


Figure 5. Test Circuit

Table 3. TEST CIRCUIT

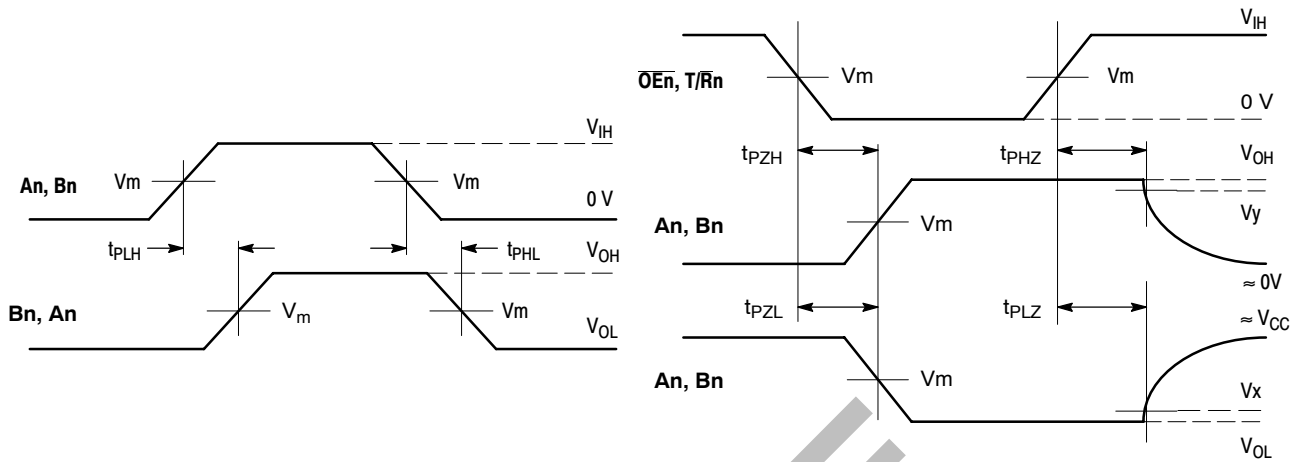
TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	6 V at V _{CC} = 3.3 ± 0.3 V; V _{CC} × 2 at V _{CC} = 2.5 ± 0.2 V; 1.8 ± 0.15 V
t _{PZH} , t _{PHZ}	GND

C_L = 30 pF or equivalent (Includes jig and probe capacitance)

R_L = 500 Ω or equivalent

R_T = Z_{OUT} of pulse generator (typically 50 Ω)

74VCX16245



WAVEFORM 3 – PROPAGATION DELAYS
 $t_R = t_F = 2.0$ ns, 10% to 90%; $f = 1$ MHz; $t_W = 500$ ns

WAVEFORM 4 – OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.0$ ns, 10% to 90%; $f = 1$ MHz; $t_W = 500$ ns

Figure 6. AC Waveforms

Table 4. AC WAVEFORMS

Symbol	V_{CC}	
	$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V
V_{IH}	2.7 V	2.7 V
V_m	1.5 V	1.5 V
V_x	$V_{OL} + 0.3\text{ V}$	$V_{OL} + 0.3\text{ V}$
V_y	$V_{OH} - 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

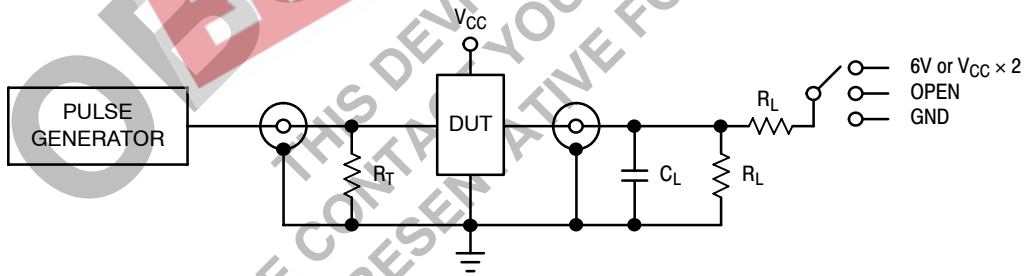


Figure 7. Test Circuit

Table 5. TEST CIRCUIT

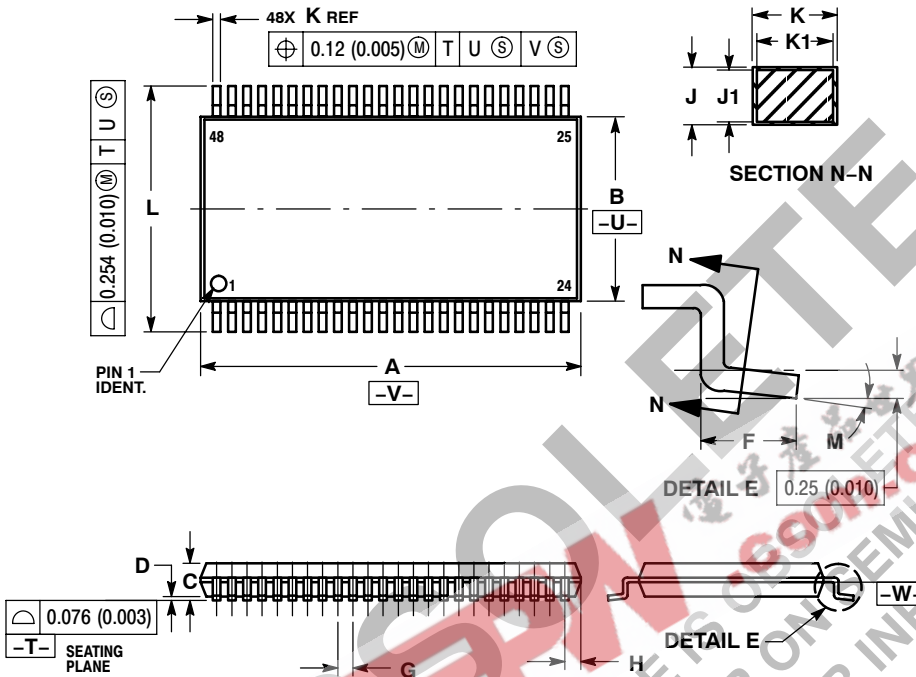
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6 V at $V_{CC} = 3.3 \pm 0.3\text{ V}$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2\text{ V}$; $1.8 \pm 0.15\text{ V}$
t_{PZH}, t_{PHZ}	GND

$C_L = 50$ pF or equivalent (Includes jig and probe capacitance)
 $R_L = 500\ \Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically $50\ \Omega$)

74VCX16245

PACKAGE DIMENSIONS

TSSOP
DT SUFFIX
CASE 1201-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	---	0.015	---
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

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