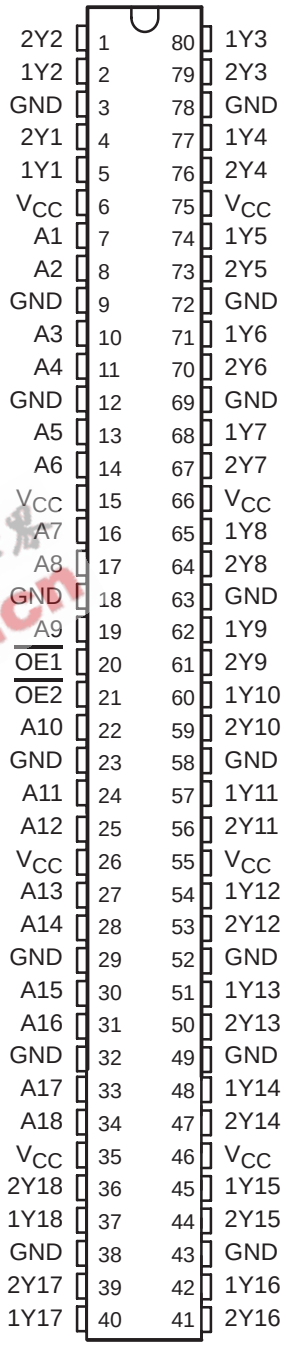
# 74ALVCHS162830A
# 1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

SCES624 – FEBRUARY 2005

- **Member of the Texas Instruments Widebus™ Family**
- **Output Ports Have Series Damping Resistors, So No External Resistors Are Required**
- **Diodes on Inputs Clamp Overshoot**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

**DBB PACKAGE**
**(TOP VIEW)**




## description/ordering information

This 1-bit to 2-bit address driver is designed for 2.3-V to 3.6-V $V_{CC}$ operation.

Diodes to $V_{CC}$ have been added on the inputs to clamp overshoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

The outputs, which are designed to sink up to 12 mA, include series damping resistors to reduce overshoot and undershoot.

The ALVCHS162830A is an improved version of the LVCHS162830 (non-A version) and has been optimized for lower power consumption and higher AC drive. Higher AC drive provides capability to drive loads with a faster edge rate.

To ensure the high-impedance state during power up or power down, the output-enable ($\overline{OE}$) input should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## description/ordering information

**ORDERING INFORMATION**

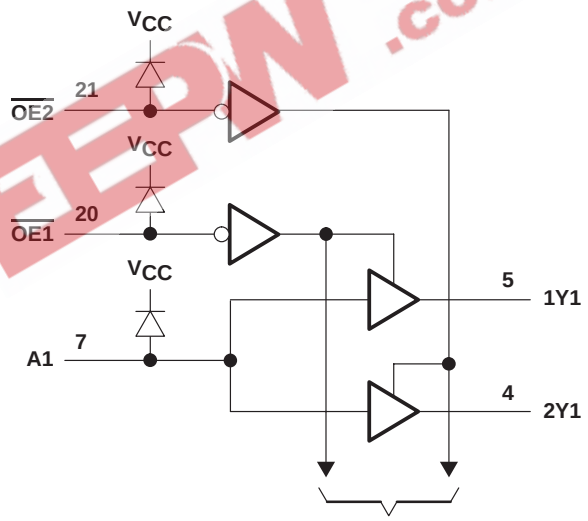
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | TVSOP − DBB | Tape and reel | 74ALVCHS162830AGR | ALVCHS162830A |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | 1Yn | 2Yn |
| L | H | H | H | Z |
| L | H | L | L | Z |
| H | L | H | Z | H |
| H | L | L | Z | L |
| L | L | H | H | H |
| L | L | L | L | L |
| H | H | X | Z | Z |

## logic diagram (positive logic)




To 17 Other Channels

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0, $V_I$ > $V_{CC}$) . . . . . ±50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . −50 mA
Continuous output current, $I_O$ . . . . . ±50 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) . . . . . 64°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2.3 V | | −6 | mA |
| | | $V_{CC}$ = 2.7 V | | −8 | |
| | | $V_{CC}$ = 3 V | | −12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2.3 V | | 6 | mA |
| | | $V_{CC}$ = 2.7 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $I_I$ = −18 mA | | 2.3 V | | | −1.2 | V |
| | | $I_I$ = 18 mA | | 2.3 V | | | $V_{CC}$ + 1.2 | |
| $V_{OH}$ | | $I_{OH}$ = −100 µA | | 2.3 V to 3.6 V | $V_{CC}$ − 0.2 | | | V |
| | | $I_{OH}$ = −4 mA, | $V_{IH}$ = 1.7 V | 2.3 V | 1.9 | | | |
| | | $I_{OH}$ = −6 mA | $V_{IH}$ = 1.7 V | 2.3 V | 1.7 | | | |
| | | | $V_{IH}$ = 2 V | 3 V | 2.4 | | | |
| | | $I_{OH}$ = −8 mA, | $V_{IH}$ = 2 V | 2.7 V | 2 | | | |
| | | $I_{OH}$ = −12 mA, | $V_{IH}$ = 2 V | 3 V | 2 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 µA | | 2.3 V to 3.6 V | | | 0.2 | V |
| | | $I_{OL}$ = 4 mA, | $V_{IL}$ = 0.7 V | 2.3 V | | | 0.4 | |
| | | $I_{OL}$ = 6 mA | $V_{IL}$ = 0.7 V | 2.3 V | | | 0.55 | |
| | | | $V_{IL}$ = 0.8 V | 3 V | | | 0.55 | |
| | | $I_{OL}$ = 8 mA, | $V_{IL}$ = 0.8 V | 2.7 V | | | 0.6 | |
| | | $I_{OL}$ = 12 mA, | $V_{IL}$ = 0.8 V | 3 V | | | 0.8 | |
| $I_I$ | | $V_I$ = $V_{CC}$ or GND | | 3.6 V | | | ±5 | µA |
| $I_{I(hold)}$ | | $V_I$ = 0.7 V | | 2.3 V | 45 | | | µA |
| | | $V_I$ = 1.7 V | | 2.3 V | −45 | | | |
| | | $V_I$ = 0.8 V | | 3 V | 75 | | | |
| | | $V_I$ = 2 V | | 3 V | −75 | | | |
| | | $V_I$ = 0 to 3.6 V‡ | | 3.6 V | | | ±500 | |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND | | 3.6 V | | | ±10 | µA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 3.6 V | | | 20 | µA |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ − 0.6 V, | Other inputs at $V_{CC}$ or GND | 3 V to 3.6 V | | | 500 | µA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 3.5 | | pF |
| | Data inputs | | | | | 4.5 | | |
| $C_o$ | Outputs | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 4.5 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

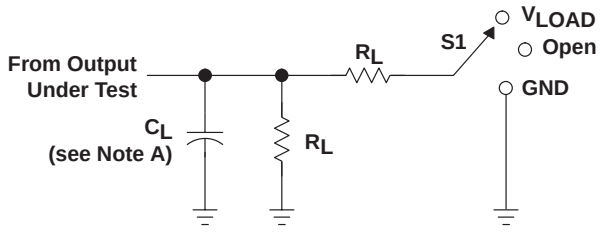
## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 1.2 | 3.8 | | 4 | 1.7 | 3.5 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | 1 | 5.7 | | 5.7 | 1 | 4.8 | ns |
| $t_{dis}$ | $\overline{OE}$ | Y | 1 | 4.9 | | 5.4 | 1.7 | 5.2 | ns |

## operating characteristics, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance per bit (one output switching) | One $\overline{OE}$ enabled | $C_L$ = 0, | f = 10 MHz | 17 | 17.5 | pF |
| | | All outputs disabled | | | 0.4 | 0.5 | |

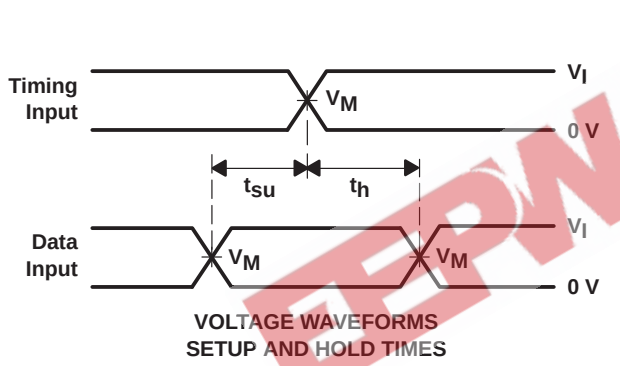
## PARAMETER MEASUREMENT INFORMATION



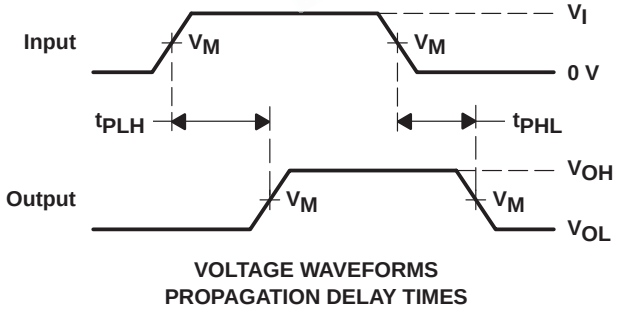

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{pd}$<br>$t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | Open<br>$V_{LOAD}$<br>GND |

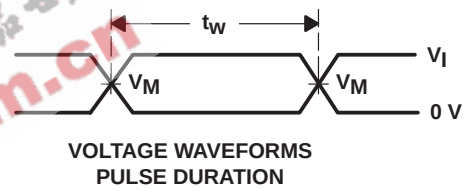
| $V_{CC}$ | INPUT | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V ± 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



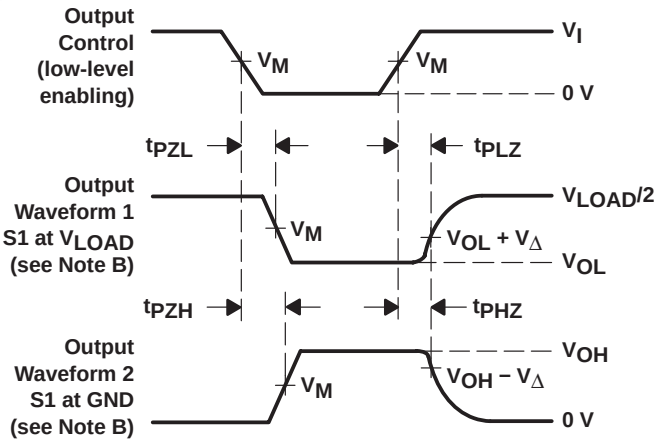

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| 74ALVCHS162830AGR | ACTIVE | TSSOP | DBB | 80 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ALVCHS162830AGRE4 | ACTIVE | TSSOP | DBB | 80 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ALVCHS162830AGRG4 | ACTIVE | TSSOP | DBB | 80 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

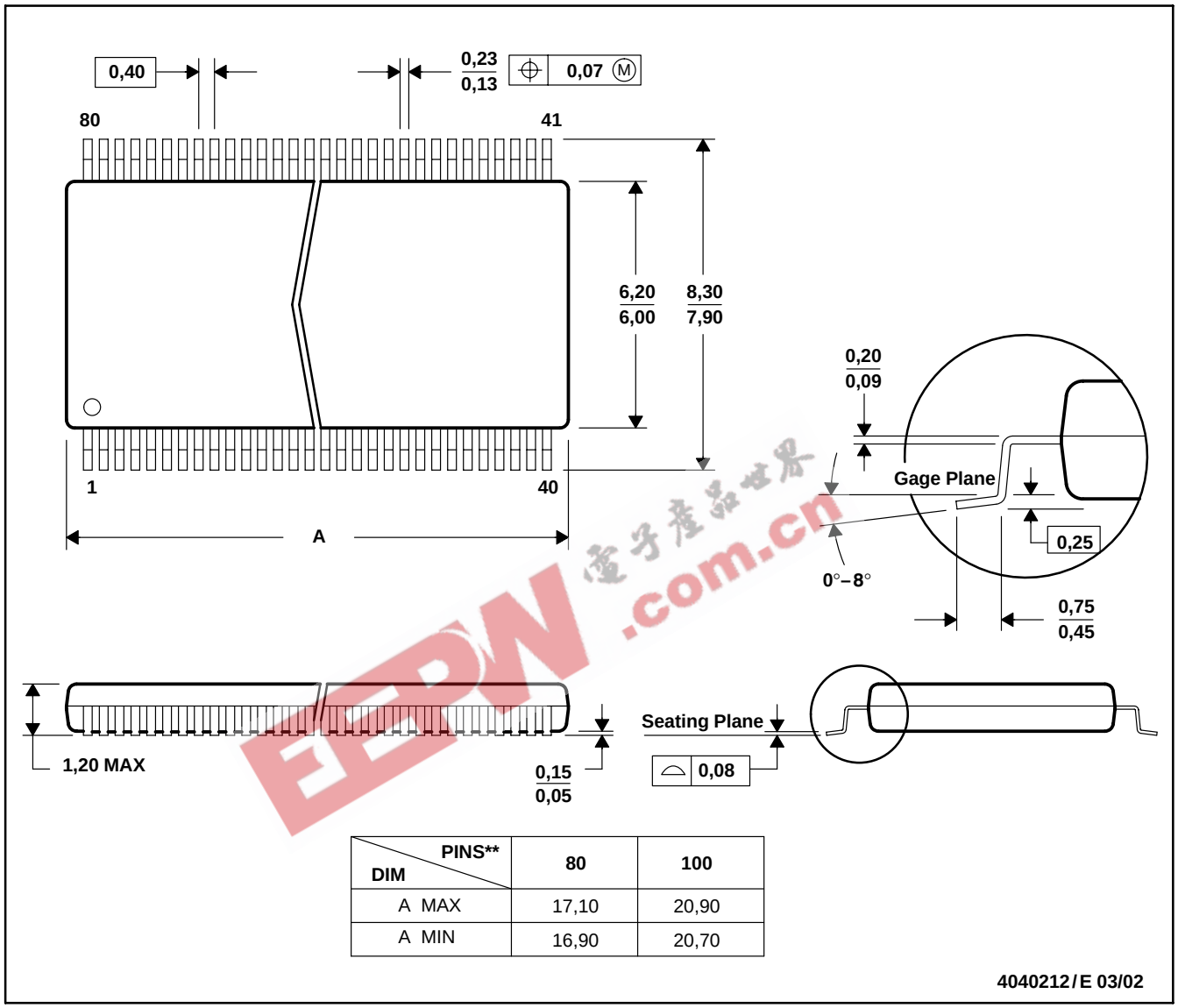
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MTSS005D – JANUARY 1995 – REVISED MARCH 2002

## DBB (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

**80 PINS SHOWN**




| DIM \ PINS** | 80 | 100 |
|---|---|---|
| A MAX | 17,10 | 20,90 |
| A MIN | 16,90 | 20,70 |

4040212 / E 03/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC : 80 Pin – MO-153 Variation FF
100 Pin – MO-194 Variation BB

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