

## 8-bit shift register with 2:1 mux-in, latched "B" inputs, and serial out

74F835

### FEATURES

- Specifically designed for Video applications
- Combines the 74F373, two 74F157s, and the 74F166 functions in one package
- Interleaved loading with 2:1 mux
- Dual 8-bit parallel inputs
- Transparent latch on all "B" inputs
- Guaranteed serial shift frequency to 100MHz
- Expandable to 16-bits or more with serial input

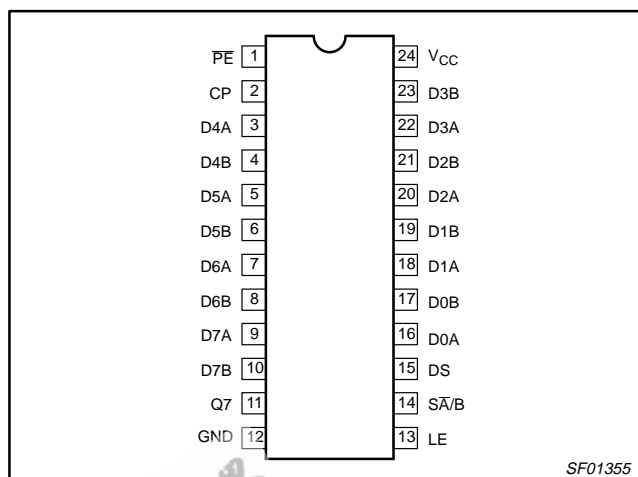
### DESCRIPTION

The 74F835 is a high speed 8-bit parallel/serial-in, serial-out shift register whose parallel inputs have been connected to an internal octal two-to-one multiplexer with all the "B" inputs connected to an octal latch.

This 24-pin part is specifically designed for video bit shifting, where interleaved loading is desired and parts count is critical. It is useful in any design where a 2:1 mux input with a transparent latch is needed.

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F835	150MHz	45mA

### PIN CONFIGURATION



### ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PACKAGE DRAWING NUMBER
24-pin plastic Slim DIP (300 mil)	N74F835N	SOT222-1
24-pin plastic SOL	N74F835D	SOT137-1

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

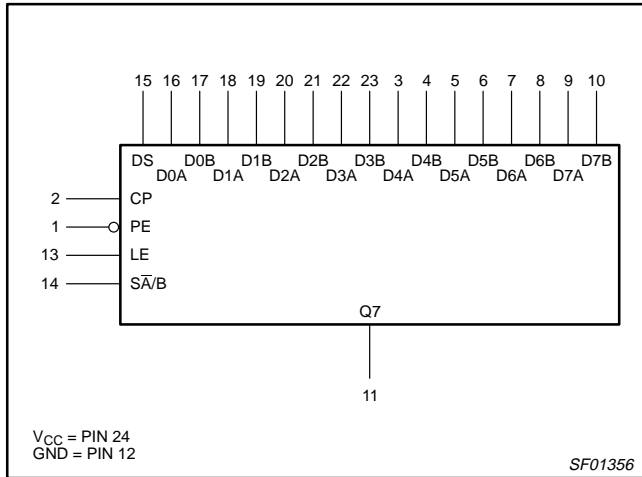
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0A – D7A	Parallel data inputs	1.0/1.0	20 $\mu$ A/0.6mA
D0B – D7B	Latched Parallel data inputs	1.0/1.0	20 $\mu$ A/0.6mA
DS	Serial data input	1.0/1.0	20 $\mu$ A/0.6mA
CP	Shift Register Clock input (active rising edge)	1.0/1.0	20 $\mu$ A/0.6mA
S̄A/B	Mux Select	1.0/1.0	20 $\mu$ A/0.6mA
LE	Latch Enable input (for B inputs)	1.0/1.0	20 $\mu$ A/0.6mA
PE	Parallel Enable input	1.0/1.0	20 $\mu$ A/0.6mA
Q7	Output	50/33	1.0mA/20mA

**NOTE:** One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

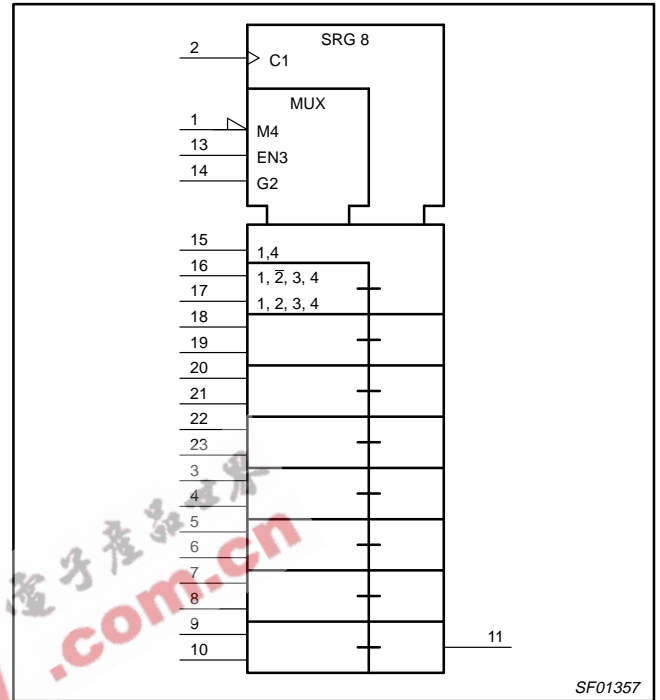
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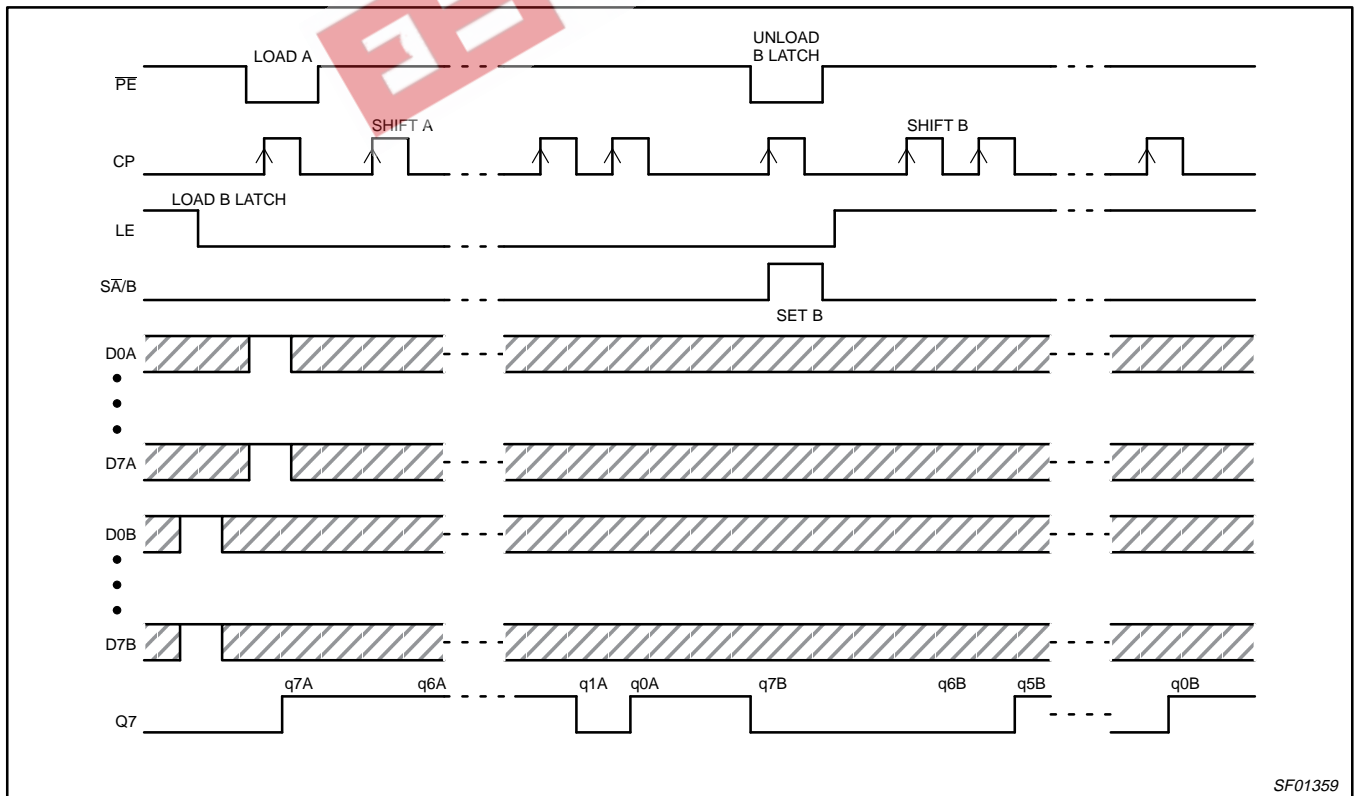
### LOGIC SYMBOL



### IEC/IEEE SYMBOL



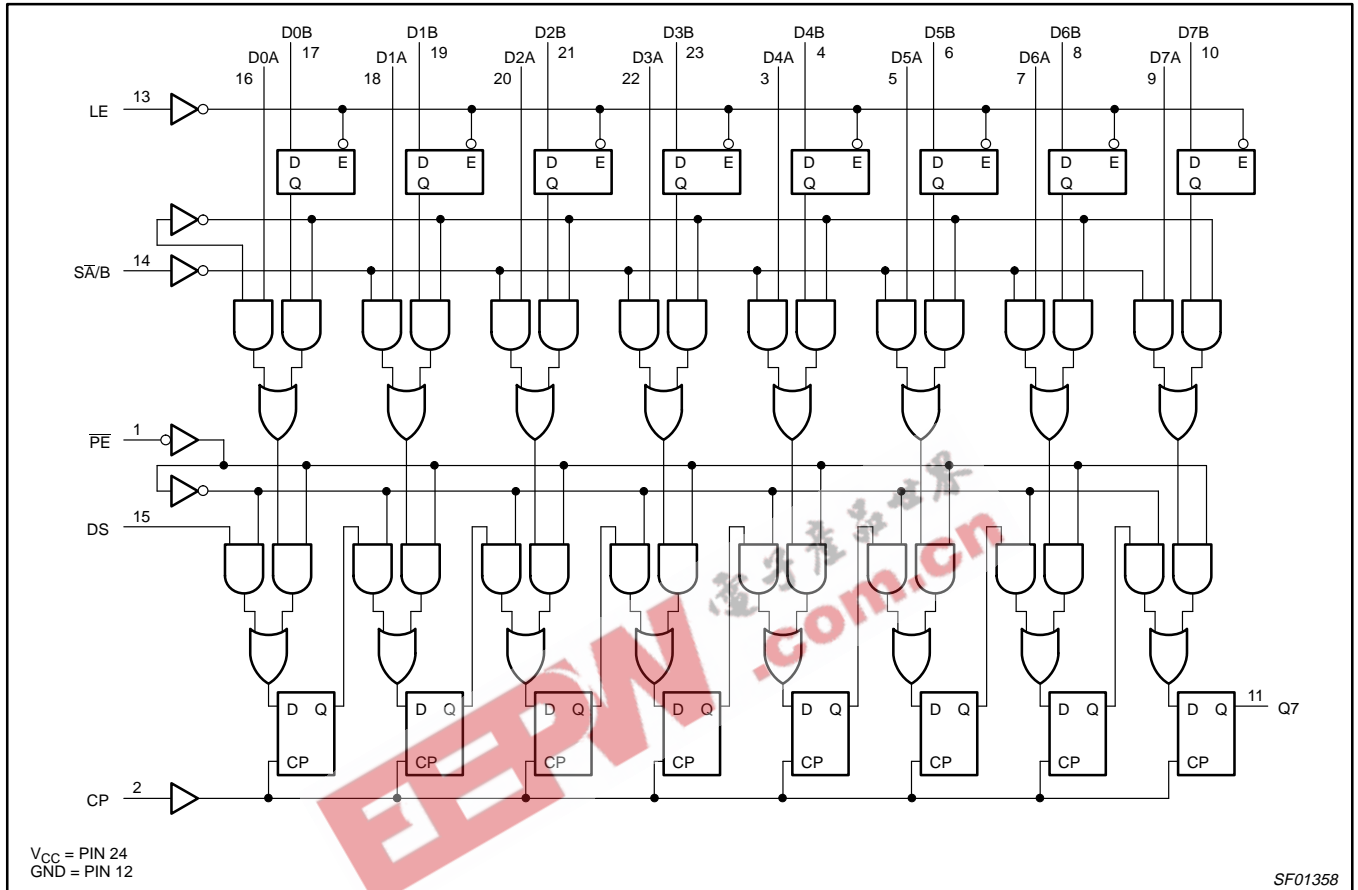
### TYPICAL TIMING DIAGRAM



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## LOGIC DIAGRAM



## FUNCTION TABLE

OPERATING MODE	INPUTS							INTERNAL			OUTPUT
	PE	CP	LE	SA/B	DnA	DnB	DS	B LATCH	SERIAL REGISTER		
									Q0	Q1-6	
Parallel load A data	L	↑	X	L	h l	X X	X X	X X	H L	H L	H L
Latch B data	X	X	L	X	X X	h l	X X	H L	X X	X X	X X
Parallel load B data (from Latch)	L	↑	L	H	X X	X X	X X	h l	H L	H L	H L
Parallel load B data (Transparent Mode)	L	↑	H	H	X X	h l	X X	h l	H L	H L	H L
Serial Shift	H	↑	X	X	X X	X X	h l	X X	H L	qn-1 qn-1	q6 q6

H = High voltage level

L = Low voltage level

h = High voltage level one setup time prior to the Low-to-High clock transition

l = Low voltage level one setup time prior to the Low-to-High clock transition

X = Don't care

qn = Lower case letters indicate the state of the referenced flop cell one cycle prior to the Low-to-High clock transition

↑ = Low-to-High clock transition

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## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>amb</sub>	Operating free-air temperature range	0		+70	°C

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±10% V <sub>CC</sub>	2.5		V	
			±5% V <sub>CC</sub>	2.7	3.4	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±10% V <sub>CC</sub>		0.30	0.50	V
			±5% V <sub>CC</sub>		0.30	0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V			100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-0.6	mA	
I <sub>OS</sub>	Short circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX	-60		-150	mA	
I <sub>CC</sub>	Supply current (total)	V <sub>CC</sub> = MAX		45	65	mA	

### NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	Waveform 1	130	150		100		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q7 (Load)	Waveform 1	5.0 5.0	7.0 7.0	9.5 9.5	5.0 5.0	10.0 10.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q7 (Shift)	Waveform 1	5.0 5.0	7.0 7.0	9.5 9.5	5.0 5.0	10.0 10.0	ns

## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time DnA or DnB to CP	Waveform 2	3.5 3.5			3.5 3.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time DnA or DnB to CP	Waveform 2	1.0 1.0			1.5 1.5		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time DS to CP	Waveform 2	1.0 1.0			1.5 1.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time DS to CP	Waveform 2	2.0 2.0			2.5 2.5		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time PE to CP	Waveform 2	3.5 3.5			4.0 4.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time PE to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time DnB to LE	Waveform 2	0.0 0.0			0.0 0.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time DnB to LE	Waveform 2	3.0 3.0			4.0 4.0		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time S $\bar{A}$ /B to CP	Waveform 2	4.5 4.5			5.0 5.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time S $\bar{A}$ /B to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	clock pulse width, High or Low	Waveform 1	4.5 4.5			5.5 5.0		ns
t <sub>w</sub> (H)	Latch Enable pulse width, High	Waveform 1	4.5			5.0		ns

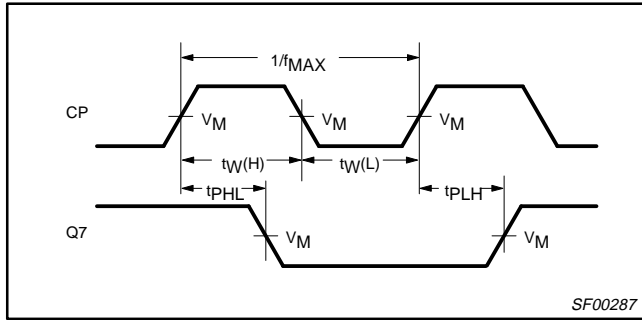
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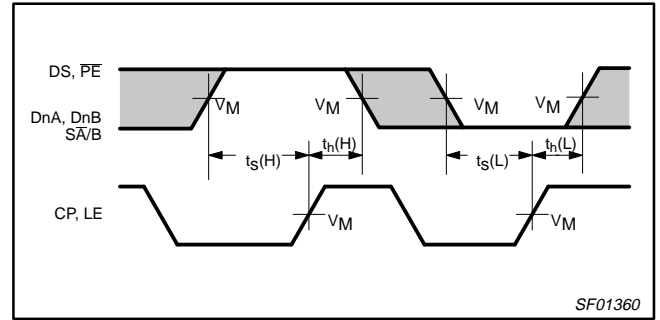
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$ .

The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data and Select Setup and Hold Times

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for Totem-Pole Outputs**

**Input Pulse Definition**

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006