National Semiconductor

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ADC08D1520QML
Low Power, 8-Bit, Dual 1.5 GSPS or Single 3.0 GSPS A/D Converter

General Description

The ADC08D1520QML is an 8–Bit, dual channel, low power, high performance CMOS analog-to-digital converter that builds upon the ADC08D1000 platform. The ADC08D1520QML digitizes signals to 8 bits of resolution at sample rates up to 1.7 GSPS. It has expanded features compared to the ADC08D1000, which include a test pattern output for system debug, clock phase adjust, and selectable output demultiplexer modes. Consuming a typical 2.0W in Demultiplex Mode at 1.5 GSPS from a single 1.9 Volt supply, this device is guaranteed to have no missing codes over the full operating temperature range. The unique folding and interpolating architecture, the fully differential comparator design, the innovative design of the internal sample-and-hold amplifier and the self-calibration scheme enable a very flat response of all dynamic parameters beyond Nyquist, producing a high 7.2 Effective Number of Bits (ENOB) with a 748 MHz input signal and a 1.5 GHz sample rate while providing a 10^{-18} Code Error Rate (C.E.R.) Output formatting is offset binary and the Low Voltage Differential Signaling (LVDS) digital outputs are compatible with IEEE 1596.3-1996, with the exception of an adjustable common mode voltage between 0.8V and 1.2V.

Each converter has a selectable output demultiplexer which feeds two LVDS buses. If the 1:2 Demultiplexed Mode is selected, the output data rate is reduced to half the input sample rate on each bus. When Non-Demultiplexed Mode is selected, that output data rate on channels DI and DQ are at the same rate as the input sample clock. The two converters can be interleaved and used as a single 3 GSPS ADC.

The converter typically consumes less than 2.9 mW in the Power Down Mode and is available in a 128-pin, thermally enhanced, multi-layer ceramic quad package and operates over the Military ($-55°C \leq T_A \leq +125°C$) temperature range.

Features

- Single +1.9V ±0.1V Operation
- Interleave Mode for 2x Sample Rate
- Multiple ADC Synchronization Capability
- Adjustment of Input Full-Scale Range, Offset and Clock Phase Adjustment
- Choice of SDR or DDR output clocking
- 1:1 or 1:2 Selectable Output Demux
- Second DCLK output
- Duty Cycle Corrected Sample Clock
- Test pattern
- Serial Interface for Extended Control

Key Specifications

Resolution	8 Bits
Max Conversion Rate	1.5 GSPS (min)
Code Error Rate	10^{-18} (typ)
ENOB @ 748 MHz Input	7.2 Bits (typ)
DNL	±0.15 LSB (typ)
Total Ionizing Dose	300 krad(Si)
Single Event Latch-up	120 MeV-cm²/mg
Power Consumption	
— Operating in 1:2 Demux Output	2.0 W (typ)
— Power Down Mode	2.9 mW (typ)

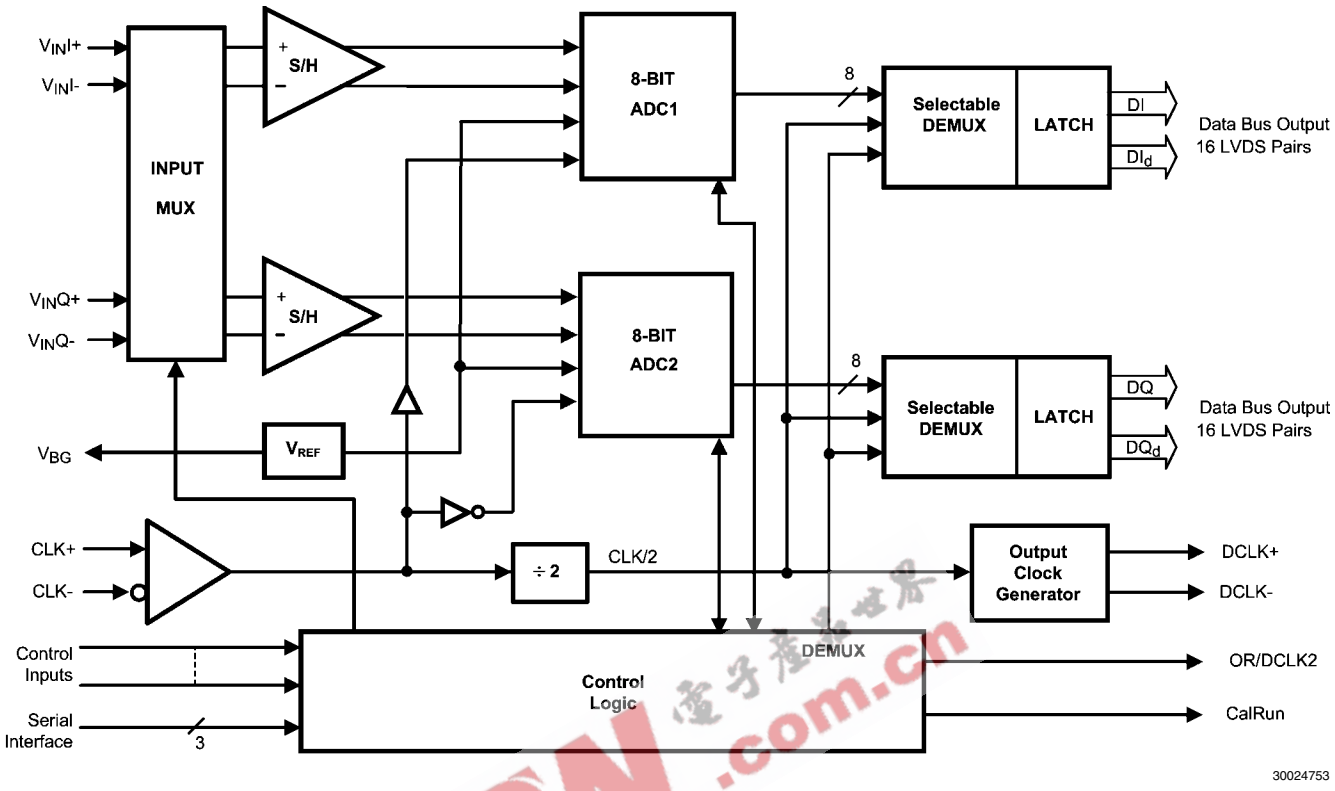
Applications

- Direct RF Down Conversion
- Digital Oscilloscopes
- Communications Systems
- Test Instrumentation

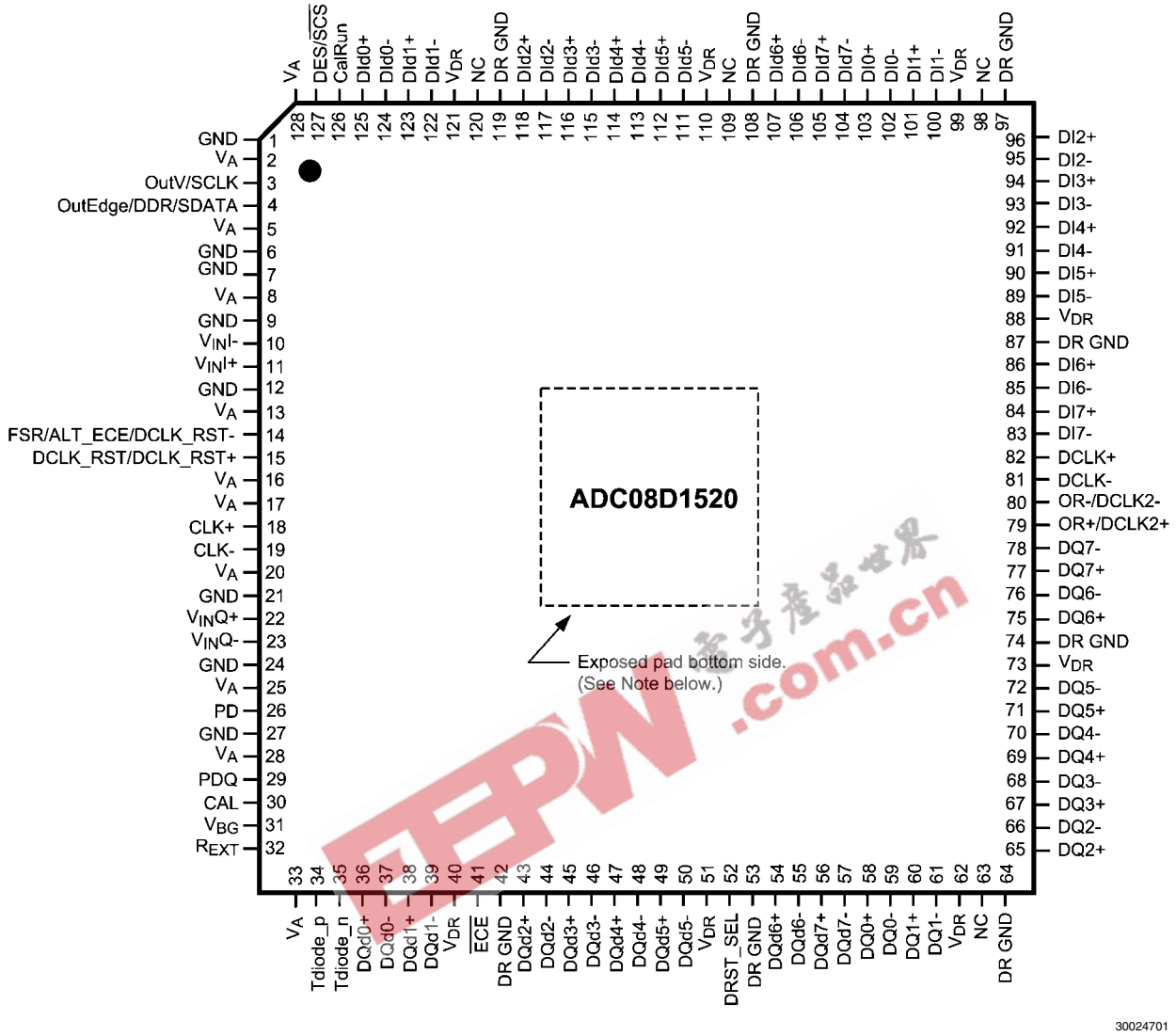
Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Discription
ADC08D1520WG-QV	5962–0721401VZC	EM128A	128L, CERQUAD GULLWING
ADC08D1520WGFQV	5962F0721401VZC 300 krad(Si)	EM128A	128L, CERQUAD GULLWING

Block Diagram



Pin Configuration



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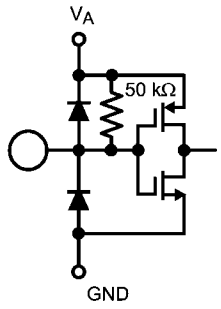
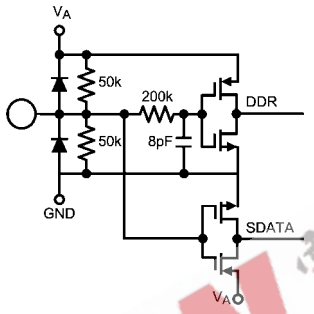
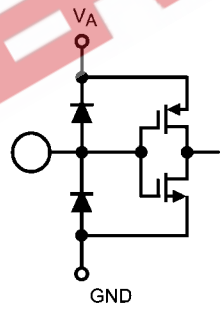
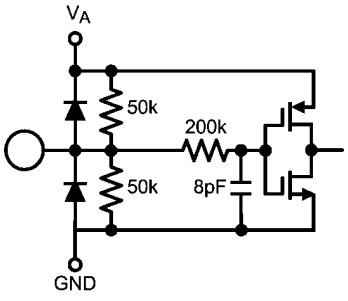
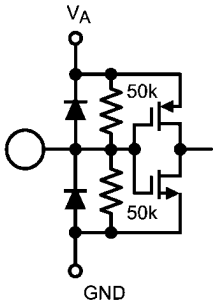
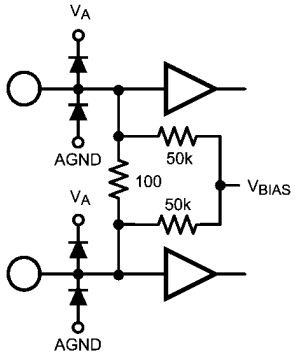
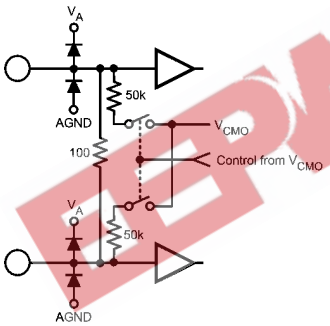
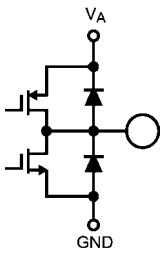
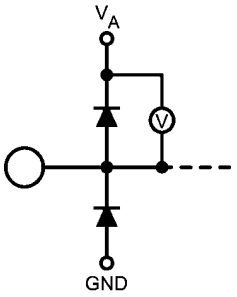
Note: The exposed pad on the bottom of the package must be soldered to a ground plane to ensure rated performance.

Pin Descriptions and Equivalent Circuits

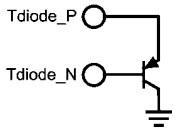
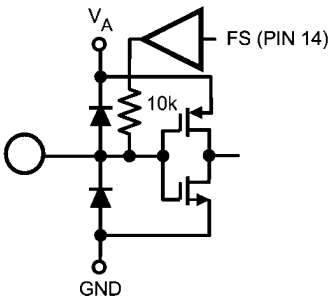
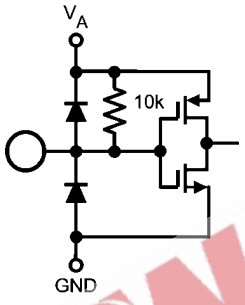
Pin Functions

Pin No.	Symbol	Equivalent Circuit	Description
3	OutV / SCLK		Output Voltage Amplitude and Serial Interface Clock. Tie this pin high for normal differential DCLK and data amplitude. Ground this pin for a reduced differential output amplitude and reduced power consumption. See *1.1.6 The LVDS Outputs*. When the extended control mode is enabled, this pin functions as the SCLK input which clocks in the serial data. See *1.2 NON-EXTENDED CONTROL/EXTENDED CONTROL* for details on the extended control mode. See *1.3 THE SERIAL INTERFACE* for description of the serial interface.
29	PDQ		A logic high on the PDQ pin puts only the Q-Channel ADC into the Power Down mode.
4	OutEdge / DDR / SDATA		DCLK Edge Select, Double Data Rate Enable and Serial Data Input. This input sets the output edge of DCLK+ at which the output data transitions. See *1.1.5.2 OutEdge and Demultiplex Control Setting* When this pin is connected to 1/2 the supply voltage, $V_A/2$, DDR clocking is enabled. When the Extended Control Mode is enabled, this pin functions as the SDATA input. See *1.2 NON-EXTENDED CONTROL/ EXTENDED CONTROL* for details on the Extended Control Mode. See *1.3 THE SERIAL INTERFACE* for description of the serial interface.
15	DCLK_RST/ DCLK_RST+		DCLK Reset. When single-ended DCLK_RST is selected by setting pin 52 logic high or to $V_A/2$, a positive pulse on this pin is used to reset and synchronize the DCLK outputs of multiple converters. See *1.5 MULTIPLE ADC SYNCHRONIZATION* for detailed description. When differential DCLK_RST is selected by setting pin 52 logic low, this pin receives the positive polarity of a differential pulse signal used to reset and synchronize the DCLK outputs of multiple converters.
26	PD		Power Down Pins. A logic high on the PD pin puts the entire device into the Power Down Mode.
30	CAL		Calibration Cycle Initiate. A minimum t_{CAL_L} input clock cycles logic low followed by a minimum of t_{CAL_H} input clock cycles high on this pin initiates the calibration sequence. See *2.5.2 Calibration* for an overview of calibration and *2.5.2.1 Initiating Calibration* for a description of calibration.
14	FSR/DCLK_RST-		Full Scale Range Select, Alternate Extended Control Enable and DCLK_RST-. This pin has two functions. It can conditionally control the ADC full-scale voltage, or become the negative polarity signal of a differential pair in differential DCLK_RST Mode. If pin 52 and pin 41 are connected at logic high, this pin can be used to set the full-scale-range. When used as the FSR pin, a logic low on this pin sets the full-scale differential input range to a reduced V_{IN} input level. A logic high on this pin sets the full-scale differential input range to Higher V_{IN} input level. See Converter Electrical Characteristics. When pin 52 is held at logic low, this pin acts as the DCLK_RST- pin. When in differential DCLK_RST Mode, there is no pin-controlled FSR and the full-scale-range is defaulted to the higher V_{IN} input level.

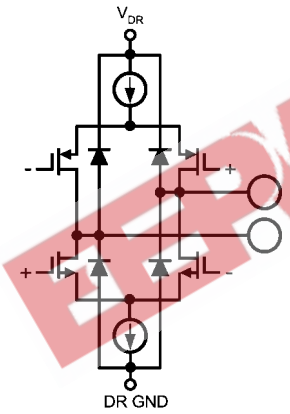
Pin Functions

Pin No.	Symbol	Equivalent Circuit	Description
127	DES / $\overline{SCS}$		Dual Edge Sampling and Serial Interface Chip Select. With pin 41 logic low, the device is in Extended Control Mode and this pin is the enable pin for the Serial Interface . When in Non-Extended Control Mode and this pin is connected to $V_A/2$, DES Mode is selected where the I- Channel input is sampled at twice the input clock rate and the Q- Channel input is ignored. See *1.1.5.1 Dual-Edge Sampling*. When in Non-Extended Controll Mode and DES is not desired, this pin should be tied to V_A.
18 19	CLK+ CLK-		LVDS Clock input pins for the ADC. The differential clock signal must be a.c. coupled to these pins. The input signal is sampled on the falling edge of CLK+. See *1.1.2 Acquiring the Input* for a description of acquiring the input and *2.4 THE CLOCK INPUTS* for an overview of the clock inputs.
10 11 .22 23	$V_{IN}I-$ $V_{IN}I+$ $V_{IN}Q+$ $V_{IN}Q-$		Analog signal inputs to the ADC. These differential input signals must be a.c. coupled to these pins. The differential full-scale input range is programmable using the FSR pin 14 in Non-Extended Control Mode and the Input Full-Scale Voltage Adjust register in the Extended Control Mode. Refer to the V_{IN} specification in the Converter Electrical Characteristics for the full-scale input range in the Non-Extended Control Mode. Refer to *1.4 REGISTER DESCRIPTION* for the full-scale input range in the Extended Control Mode.
31	V_{BG}		Bandgap output voltage. This pin is capable of sourcing or sinking 100 µA and can drive a load up to 80 pF.
126	CalRun		Calibration Running indication. This pin is at a logic high when calibration is running.
32	R_{EXT}		External bias resistor connection. Nominal value is 3.3 kΩ (±0.1%) to ground. See *1.1.1 Calibration*.

Pin Functions

Pin No.	Symbol	Equivalent Circuit	Description
34 35	Tdiode_P Tdiode_N		Temperature Diode Positive (Anode and Negative (Cathode). This pin is used for die temperature measurements. See *2.7.2 Thermal Management*.
41	$\overline{ECE}$		Extended Control Enable. This pin always enables or disables Extended Control Mode. When this pin is set logic high, the Extended Control Mode is inactive and all control of the device must be through control pins only . When it is set logic low, the Extended Control Mode is active. This pin overrides the Extended Control Enable signal set using pin 14.
52	DRST_SEL		DCLK_RST select. This pin selects whether the DCLK is reset using a single-ended or differential signal. When this pin is connected at logic high, the DCLK_RST operation is single-ended and pin 14 functions as FSR/ALT_ECE. When this pin is logic low, the DCLK_RST operation becomes differential with functionality on pin 15 (DCLK_RST+) and pin 14 (DCLK_RST-). When in differential DCLK_RST Mode, there is no pin-controlled FSR and the full-scale-range is defaulted to 870mV. When pin 41 is set logic low, the Extended Control Mode is active and the Full-Scale Voltage Adjust registers can be programmed.

Pin Functions

Pin No.	Symbol	Equivalent Circuit	Description
83 / 78	DI7– / DQ7–		I- and Q- channel LVDS Data Outputs that are not delayed in the output demultiplexer. Compared with the DId and DQd outputs, these outputs represent the later time samples. These outputs should always be terminated with a 100Ω differential resistor.
84 / 77	DI7+ / DQ7+		
85 / 76	DI6– / DQ6–		
86 / 75	DI6+ / DQ6+		
89 / 72	DI5– / DQ5–		
90 / 71	DI5+ / DQ5+		
91 / 70	DI4– / DQ4–		
92 / 69	DI4+ / DQ4+		
93 / 68	DI3– / DQ3–		
94 / 67	DI3+ / DQ3+		
95 / 66	DI2– / DQ2–		
96 / 65	DI2+ / DQ2+		
100 / 61	DI1– / DQ1–		
101 / 60	DI1+ / DQ1+		
102 / 59	DI0– / DQ0–		
103 / 58	DI0+ / DQ0+		
104 / 57	DId7– / DQd7–		I- and Q- channel LVDS Data Outputs that are delayed by one CLK cycle in the output demultiplexer. Compared with the DI and DQ outputs, these outputs represent the earlier time sample. These outputs should always be terminated with a 100Ω differential resistor. In Non Demux Mode, these outputs are disabled and are high impedance. When disabled, these outputs must be left floating.
105 / 56	DId7+ / DQd7+		
106 / 55	DId6– / DQd6–		
107 / 54	DId6+ / DQd6+		
111 / 50	DId5– / DQd5–		
112 / 49	DId5+ / DQd5+		
113 / 48	DId4– / DQd4–		
114 / 47	DId4+ / DQd4+		
115 / 46	DId3– / DQd3–		
116 / 45	DId3+ / DQd3+		
117 / 44	DId2– / DQd2–		
118 / 43	DId2+ / DQd2+		
122 / 39	DId1– / DQd1–		
123 / 38	DId1+ / DQd1+		
124 / 37	DId0– / DQd0–		
125 / 36	DId0+ / DQd0+		
79 80	OR+/DCLK2+ OR-/DCLK2-		Out Of Range output. A differential high at these pins indicates that the differential input is out of range $\pm V_{IN}/2$ as programmed by the FSR pin in Non-Extended Control Mode or the Input Full-Scale Voltage Adjust register setting in the Extended Control Mode). DCLK2 is the exact mirror of DCLK and should output the same signal at the same rate.
81 82	DCLK- DCLK+		Data Clock. Differential Clock outputs used to latch the output data. Delayed and non-delayed data outputs are supplied synchronous to this signal. In 1:2 Demultiplexed Mode, this signal is at 1/2 the input clock rate in SDR Mode and at 1/4 the input clock rate in the DDR Mode. By default, the DCLK outputs are not active during the termination resistor trim section of the calibration cycle. If a system requires DCLK to run continuously during a calibration cycle, the termination resistor trim portion of the cycle can be disabled by setting the Resistor Trim Disable (RTD) bit to logic high in the Extended Configuration Register (address 9h). This disables all subsequent termination resistor trims after the initial trim which occurs during the power on calibration. Therefore, this output is not recommended as a system clock unless the resistor trim is disabled. When the device is in the Non-Demultiplexed Mode, DCLK can only be in DDR Mode and the signal is at 1/2 the input clock rate.

Pin Functions

Pin No.	Symbol	Equivalent Circuit	Description
2, 5, 8, 13, 16, 17, 20, 25, 28, 33, 128	V_A		Analog power supply pins. Bypass these pins to ground.
40, 51, 62, 73, 88, 99, 110, 121	V_{DR}		Output Driver power supply pins. Bypass these pins to DR GND.
1, 6, 7, 9, 12, 21, 24, 27	GND		Ground return for V_A.
42, 53, 64, 74, 87, 97, 108, 119	DR GND		Ground return for V_{DR}.
63, 98, 109, 120	NC		No Connection. Make no connection to these pins.

Absolute Maximum Ratings

(Notes 1, 2)

Supply Voltage (V_A, V_{DR})	2.2V
Supply Difference V_{DR} - V_A	0V to 100 mV
Voltage on Any Input Pin	−0.15V to (V_A +0.15V)
Ground Difference |GND - DR GND|	0V to 100 mV
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Junction Temperature	≤ 175°C
ESD Susceptibility (Note 4) Human Body Model	Class 3A (6000V)
Storage Temperature	−65°C to +175°C

Operating Ratings (Notes 1, 2)

Ambient Temperature Range	−55°C ≤ T_A ≤ +125°C
V_A/2 Tolerance for supply 1.9V	650mV ≥ V_A/2 ≤ 1.2V
Supply Voltage (V_A)	+1.8V to +2.0V
Driver Supply Voltage (V_{DR})	+1.8V to V_A
V_{IN}+, V_{IN}- Voltage Range (Maintaining Common Mode)	200mV to V_A
Ground Difference (|GND - DR GND|)	0V
CLK Pins Voltage Range	0V to V_A
Differential CLK Amplitude	0.4V_{P-P} to 2.0V_{P-P}

Package Thermal Resistance

Package	θ_{JA}	θ_{JC} Top of Package	θ_{JC} Thermal Pad
128L Cer Quad Gullwing	11.5°C/ W	3.8°C/ W	2.0°C/ W

Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging.

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Setting time at	+25
13	Setting time at	+125
14	Setting time at	-55

ADC08D1520QML Converter Electrical Characteristics

DC Parameters (Note 14)

The following specifications apply after calibration for $V_A = V_{DR}$ = +1.9V; OutV = 1.9V; V_{IN} FSR (a.c. coupled) = differential 870 mV_{P-P}; C_L = 10 pF; Differential, a.c. coupled Sine Wave Input Clock, f_{CLK} = 1.5 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = Floating; Non-Extended Control Mode; SDR Mode; R_{EXT} = 3300 Ω ±0.1%; Analog Signal Source Impedance = 100 Ω Differential; 1:2 Output Demultiplex, duty cycle stabilizer on. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (Notes 5, 6)

Symbol	Parameter	Conditions	Notes	Typical (Note 7)	Min	Max	Units	Sub-groups
STATIC CONVERTER CHARACTERISTICS								
INL	Integral Non-Linearity (Best fit)	DC Coupled, 1 MHz Sine Wave Overanged		±0.3		**±.9**	LSB	1, 2, 3
DNL	Differential Non-Linearity	DC Coupled, 1 MHz Sine Wave Overanged		±0.15		**±.6**	LSB	1, 2, 3
	Resolution with No Missing Codes					**8**	Bits	1, 2, 3
V_{OFF}	Offset Error			−0.55	**−1.5**	**1.5**	LSB	1, 2, 3
PFSE	Positive Full-Scale Error		(Note 8)	−0.6		**±25**	mV	1, 2, 3
NFSE	Negative Full-Scale Error		(Note 8)	−1.31		**±25**	mV	1, 2, 3
ANALOG INPUT AND REFERENCE CHARACTERISTICS								
V_{IN}	Full Scale Analog Differential Input Range	FSR pin 14 Low		600	**530**		mV_{P-P}	1, 2, 3
						650	mV_{P-P}	1, 2, 3
		FSR pin 14 High		900	**840**		mV_{P-P}	1, 2, 3
						960	mV_{P-P}	1, 2, 3
R_{IN}	Differential Input Resistance			100	**94**		Ω	1, 2, 3
						106	Ω	1, 2, 3
ANALOG OUTPUT CHARACTERISTICS								
V_{BG}	Bandgap Reference Output Voltage	I_{BG} = ±100 µA		1.26	**1.20**		V	1, 2, 3
						1.33	V	1, 2, 3
CLOCK INPUT CHARACTERISTICS								
V_{ID}	Differential Clock Input Level	Sine Wave Clock		0.6	**.5**		V_{P-P}	1, 2, 3
						2.0	V_{P-P}	1, 2, 3
		Square Wave Clock		0.6	**.5**		V_{P-P}	1, 2, 3
						2.0	V_{P-P}	1, 2, 3
DIGITAL CONTROL PIN CHARACTERISTICS								
V_{IH}	Logic High Input Voltage				**0.85 x V_A**		V	1, 2, 3
V_{IL}	Logic Low Input Voltage					**0.15 x V_A**	V	1, 2, 3
DIGITAL OUTPUT CHARACTERISTICS								
V_{OD}	LVDS Differential Output Voltage	Measured differentially, OutV = V_A, V_{BG} = Floating	(Note 13)	780	**580**		mV_{P-P}	1, 2, 3
						920	mV_{P-P}	1, 2, 3
		Measured differentially, OutV = GND, V_{BG} = Floating	(Note 13)	590	**380**		mV_{P-P}	1, 2, 3
						720	mV_{P-P}	1, 2, 3

Symbol	Parameter	Conditions	Notes	Typical (Note 7)	Min	Max	Units	Sub-groups
POWER SUPPLY CHARACTERISTICS								
I_A	Analog Supply Current	**1:2 Demux Output** PD = PDQ = Low PD = Low, PDQ = High PD = PDQ = High		 820 565 1.5		 **875** **615**	 mA (max) mA (max) mA	 1, 2, 3 1, 2, 3
I_{DR}	Output Driver Supply Current	**1:2 Demux Output** PD = PDQ = Low PD = Low, PDQ = High PD = PDQ = High		 230 125 0.018		 **290** **170**	 mA (max) mA (max) mA	 1, 2, 3 1, 2, 3
P_D	Power Consumption	**1:2 Demux Output** PD = PDQ = Low PD = Low, PDQ = High PD = PDQ = High		 2 1.3 2.9		 **2.2** **1.49**	 W (max) W (max) mW	 1, 2, 3 1, 2, 3

AC Parameters (Note 14)

Symbol	Parameter	Conditions	Notes	Typical (Note 7)	Min	Max	Units	Sub-groups
Non-DES MODE DYNAMIC CONVERTER CHARACTERISTICS, 1:2 DEMUX MODE								
ENOB	Effective Number of Bits	f_{IN} = 373 MHz, V_{IN} = FSR – 0.5 dB f_{IN} = 748 MHz, V_{IN} = FSR – 0.5 dB		7.4 7.2	7		Bits (min) Bits (min)	4, 5, 6 4, 5, 6
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 373 MHz, V_{IN} = FSR – 0.5 dB f_{IN} = 748 MHz, V_{IN} = FSR – 0.5 dB		46.3 45.4	**43.9**		dB (min) dB (min)	4, 5, 6 4, 5, 6
SNR	Signal-to-Noise Ratio	f_{IN} = 373 MHz, V_{IN} = FSR – 0.5 dB f_{IN} = 748 MHz, V_{IN} = FSR – 0.5 dB		47 45	**43.9**		dB (min) dB (min)	4, 5, 6 4, 5, 6
THD	Total Harmonic Distortion	f_{IN} = 373 MHz, V_{IN} = FSR – 0.5 dB f_{IN} = 748 MHz, V_{IN} = FSR – 0.5 dB		–53.4 –53		**–47.5**	dB (max) dB (max)	4, 5, 6 4, 5, 6
SFDR	Spurious-Free dynamic Range	f_{IN} = 373 MHz, V_{IN} = FSR – 0.5 dB f_{IN} = 748 MHz, V_{IN} = FSR – 0.5 dB		55.5 53	**47.5**		dB (min) dB (min)	4, 5, 6 4, 5, 6
	Out of Range Output Code	$(V_{IN}+) - (V_{IN}-)$ > + Full Scale				**255**		4, 5, 6
		$(V_{IN}+) - (V_{IN}-)$ < – Full Scale				**0**		4, 5, 6
INTERLEAVE MODE (DES Pin 127=V_A/2) - DYNAMIC CONVERTER CHARACTERISTICS, 1:4 DEMUX MODE								
ENOB	Effective Number of Bits	f_{IN} = 373 MHz, V_{IN} = FSR – 0.5 dB		7.0	**6.6**		Bits	4, 5, 6
SINAD	Signal to Noise Plus Distortion Ratio	f_{IN} = 373 MHz, V_{IN} = FSR – 0.5 dB		44	**41.5**		dB	4, 5, 6
SNR	Signal to Noise Ratio	f_{IN} = 373 MHz, V_{IN} = FSR – 0.5 dB		44	**41.5**		dB	4, 5, 6
THD	Total Harmonic Distortion	f_{IN} = 373 MHz, V_{IN} = FSR – 0.5 dB		–55		**–45.2**	dB	4, 5, 6
SFDR	Spurious Free Dynamic Range	f_{IN} = 373 MHz, V_{IN} = FSR – 0.5 dB		50	**44.1**		dB	4, 5, 6

AC Timing Parameters (Note 14)

Symbol	Parameter	Conditions	Notes	Typical (Note 7)	Min	Max	Units	Sub-groups
AC TIMING CHARACTERISTICS								
$f_{CLK(max)}$	Maximum Input Clock Frequency	Non-DES Mode or DES Mode in 1:2 Output Demux		1.7		**1.5**	GHz	9, 10, 11
		Non-DES Mode or DES Mode in Non-demux Output				**1.0**	GHz	9, 10, 11
	DCLK Duty Cycle			50	**45**		%	9, 10, 11
						55	%	9, 10, 11
t_{PWR}	Pulse Width DCLK_RST±					**4**	CLK± Cycles (min)	9, 10, 11
t_{CAL_L}	CAL Pin Low Time	See *Figure 10*			**1280**		CLK± Cycles	9, 10, 11
t_{CAL_H}	CAL Pin High Time	See *Figure 10*			**1280**		CLK± Cycles	9, 10, 11

Typical Electrical Characteristics

DC Parameters

The following specifications apply after calibration for $V_A = V_{DR}$ = +1.9V; OutV = 1.9V; V_{IN} FSR (a.c. coupled) = differential 870 mV_{P-P}; C_L = 10 pF; Differential, a.c. coupled Sine Wave Input Clock, f_{CLK} = 1.5 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = Floating; Non-Extended Control Mode; SDR Mode; R_{EXT} = 3300 Ω ±0.1%; Analog Signal Source Impedance = 100 Ω Differential; 1:2 Output Demultiplex, duty cycle stabilizer on. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**. All other limits T_A = 25°C, unless otherwise noted. (Notes 5, 6)

Symbol	Parameter	Conditions	Notes	Typical (Note 7)	Units
STATIC CONVERTER CHARACTERISTICS					
V_{OFF}_ADJ	Input Offset Adjustment Range	Extended Control Mode		±45	mV
FS_ADJ	Full-Scale Adjustment Range	Extended Control Mode		±20	%FS
ANALOG INPUT AND REFERENCE CHARACTERISTICS					
C_{IN}	Analog Input Capacitance, Normal operation	Differential	(Note 9)	0.02	pF
		Each input pin to ground		1.6	pF
	Analog Input Capacitance, DES Mode	Differential	(Note 9)	0.08	pF
		Each input pin to ground		2.2	pF
ANALOG OUTPUT CHARACTERISTICS					
TC V_{BG}	Bandgap Reference Voltage Temperature Coefficient	T_A = −55°C to +125°C, I_{BG} = ±100 µA		61	ppm/°C
C_{LOAD} V_{BG}	Maximum Bandgap Reference load Capacitance			80	pF
TEMPERATURE DIODE CHARACTERISTICS					
ΔV_{BE}	Temperature Diode Voltage	192 µA vs 12 µA, T_J = 25°C		71.23	mV
		192 µA vs 12 µA, T_J = 125°C		94.8	mV
CHANNEL-TO-CHANNEL CHARACTERISTICS					
	Offset Match			1	LSB
	Positive Full-Scale Match	Zero offset selected in Control Register		1	LSB
	Negative Full-Scale Match	Zero offset selected in Control Register		1	LSB
	Phase Matching (I,Q)	f_{IN} = 1.0 GHz		< 1	Degree
X-TALK	Crosstalk from I- Channel (Aggressor) to Q- Channel (Victim)	Aggressor = 1160 MHz F.S. Victim = 100 MHz F.S.		−66	dB
X-TALK	Crosstalk from Q- Channel (Aggressor) to I- Channel (Victim)	Aggressor = 1160 MHz F.S. Victim = 100 MHz F.S.		−66	dB
CLOCK INPUT CHARACTERISTICS					
I_I	Input Current	V_{IN} = 0 or V_{IN} = V_A		±1	µA
C_{IN}	Input Capacitance	Differential	(Note 9)	0.02	pF
		Each input to ground		1.5	pF
DIGITAL CONTROL PIN CHARACTERISTICS					
C_{IN}	Input Capacitance	Each input to ground	(Note 11)	1.2	pF
DIGITAL OUTPUT CHARACTERISTICS					
$\Delta V_{O\ DIFF}$	Change in LVDS Output Swing Between Logic Levels			±1	mV
V_{OS}	Output Offset Voltage	V_{BG} = Floating (See *Figure 1*)		800	mV
V_{OS}	Output Offset Voltage	V_{BG} = V_A (See *Figure 1*)	(Note 13)	1100	mV
ΔV_{OS}	Output Offset Voltage Change Between Logic Levels			±1	mV
I_{OS}	Output Short Circuit Current	Output+ & Output− connected to 0.8V, V_{BG} = Floating, OutV = V_A		±4	mA

Symbol	Parameter	Conditions	Notes	Typical (Note 7)	Units
Z_O	Differential Output Impedance			100	Ω
V_{OH}	CalRun H level output	I_{OH} = −400 µA	(Note 10)	1.72	V
V_{OL}	CalRun L level output	I_{OH} = 400 µA	(Note 10)	0.17	V
POWER SUPPLY CHARACTERISTICS					
PSRR1	D.C. Power Supply Rejection Ratio	Change in Full Scale Error with change in V_A from 1.8V to 2.0V		30	dB
PSRR2	A.C. Power Supply Rejection Ratio	248 MHz, 50 mV_{P-P} injected on V_A		51	dB

AC Parameters

Symbol	Parameter	Conditions	Notes	Typical (Note 7)	Units
Non-DES MODE DYNAMIC CONVERTER CHARACTERISTICS, 1:2 DEMUX MODE					
FPBW	Full Power Bandwidth	Non-DES Mode		2.0	GHz
C.E.R.	Code Error Rate			10^{-18}	Error/Sample
	Gain Flatness	d.c. to 498 MHz		±0.5	dBFS
		d.c. to 1 GHz		±1.0	dBFS
2nd Harm	Second Harmonic Distortion	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB		−60	dB
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB		−55	dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB		−62	dB
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB		−58	dB
IMD	Intermodulation Distortion	f_{IN1} = 365 MHz, V_{IN} = FSR − 7 dB f_{IN2} = 375 MHz, V_{IN} = FSR − 7 dB		−50	dB
INTERLEAVE MODE (DES Pin 127=V_A/2) - DYNAMIC CONVERTER CHARACTERISTICS, 1:4 DEMUX MODE					
FPBW	Full Power Bandwidth	Dual Edge Sampling Mode		1.7	GHz
2nd Harm	Second Harmonic Distortion	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB		−60	dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB		−65	dB

AC Timing Parameters

Symbol	Parameter	Conditions		Notes	Typical (Note 7)	Units
AC TIMING CHARACTERISTICS						
$f_{CLK(min)}$	Minimum Input Clock Frequency	Non-DES Mode			200	MHz
		DES Mode			500	MHz
	Input Clock Duty Cycle	200 MHz ≤ f_{CLK} ≤ 1.5 GHz **(Non-DES Mode)**		(Note 10)	50	% (min)
						% (max)
		500 MHz ≤ f_{CLK} ≤ 1.5 GHz **(DES Mode)**		(Note 10)	50	% (min)
						% (max)
t_{CL}	Input Clock Low Time			(Note 10)	333	ps (min)
t_{CH}	Input Clock High Time			(Note 10)	333	ps (min)
t_{SR}	Setup Time DCLK_RST±				90	ps
t_{HR}	Hold Time DCLK_RST±				30	ps
t_{SD}	Synchronizing Edge to DCLK Output Delay				t_{OD} + t_{OSK}	
t_{LHT}	Differential Low-to-High Transition Time	10% to 90%, C_L = 2.5 pF			150	ps
t_{HLT}	Differential High-to-Low Transition Time	10% to 90%, C_L = 2.5 pF			150	ps
t_{OSK}	DCLK-to-Data Output Skew	50% of DCLK transition to 50% of Data transition, SDR Mode and DDR Mode, 0° DCLK			±50	ps (max)
t_{SU}	Data-to-DCLK Set-Up Time	DDR Mode, 90° DCLK			400	ps
t_H	DCLK-to-Data Hold Time	DDR Mode, 90° DCLK			560	ps
t_{AD}	Sampling (Aperture) Delay	Input CLK+ Fall to Acquisition of Data			1.6	ns
t_{AJ}	Aperture Jitter				0.4	ps rms
t_{OD}	Input Clock-to Data Output Delay (in addition to Pipeline Delay)	50% of Input Clock transition to 50% of Data transition			4	ns
	Pipeline Delay (Latency) 1:2 Demux Mode	DI Outputs		(Notes 10, 12)	13	CLK± Cycles
		DId Outputs			14	
		DQ Outputs	Non-DES Mode		13	
			DES Mode		13.5	
		DQd Outputs	Non-DES Mode		14	
			DES Mode		14.5	
	Pipeline Delay (Latency) 1:1 Demux Mode	DI Outputs		(Notes 10, 12)	13	CLK± Cycles
		DId Outputs			13	
		DQ Outputs	Non-DES Mode		13	
			DES Mode		13.5	
		DQd Outputs	Non-DES Mode		13	
			DES Mode		13.5	
	Over Range Recovery Time	Differential V_{IN} step from ±1.2V to 0V to get accurate conversion			1	CLK± Cycle
t_{WU}	PD low to Rated Accuracy Conversion (Wake-Up Time)	Non-DES Mode			500	ns
		DES Mode			1	µs
f_{SCLK}	Serial Clock Frequency				15	MHz
t_{SSU}	Data to Serial Clock Setup Time				2.5	ns (min)
t_{SH}	Data to Serial Clock Hold Time				1	ns (min)
	Serial Clock Low Time				26	ns

Symbol	Parameter	Conditions	Notes	Typical (Note 7)	Units
	Serial Clock High Time			26	ns
t_{CAL}	Calibration Cycle Time			1.4 x 10^6	CLK± Cycles

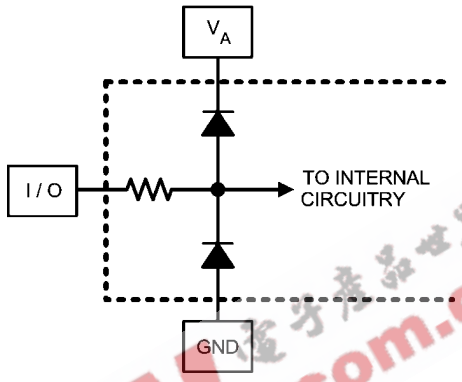
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no guarantee of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = DR GND = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supply limits (that is, less than GND or greater than V_A), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two. This limit is not placed upon the power, ground and digital output pins.

Note 4: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 5: The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



Note 6: To guarantee accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors. Additionally, achieving rated performance requires that the backside exposed pad be well grounded.

Note 7: Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to MIL-PRF-38535.

Note 8: Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error. See *Figure 2*. For relationship between Gain Error and Full-Scale Error, see Specification Definitions for Gain Error.

Note 9: The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.65 pF differential and 0.95 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Note 10: This parameter is guaranteed by design and/or characterization and is not tested in production.

Note 11: The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Note 12: Each of the two converters of the ADC08D1520QMLQML has two LVDS output buses, which each clock data out at one half the sample rate. The data at each bus is clocked out at one half the sample rate. The second bus (D0 through D7) has a pipeline latency that is one Input Clock cycle less than the latency of the first bus (Dd0 through Dd7). 1:2 Demux Mode.

Note 13: Tying V_{BG} to the supply rail will increase the output offset voltage (V_{OS}) by 300mv (typical), as shown in the V_{OS} specification above. Tying V_{BG} to the supply rail will also affect the differential LVDS output voltage (V_{OD}), causing it to increase by 30mV (typical).

Note 14: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019

Specification Definitions

APERTURE (SAMPLING) DELAYis the amount of delay, measured from the sampling edge of the Clock input, after which the signal present at the input pin is sampled inside the device.

APERTURE JITTER (t_{AJ}) is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

CODE ERROR RATE (C.E.R.) is the probability of error and is defined as the probable number of word errors on the ADC output per unit of time divided by the number of words seen in that amount of time.. A C.E.R. of 10^{-18} corresponds to a statistical error in one word about every four (4) years.

CLOCK DUTY CYCLE is the ratio of the time that the clock waveform is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. Measured at sample rate = 500 MSPS with a 1MHz input sinewave.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD – 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH (FPBW) is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full-scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Offset and Full-Scale Errors:

Positive Gain Error = Offset Error – Positive Full-Scale Error

Negative Gain Error = –(Offset Error – Negative Full-Scale Error)

Gain Error = Negative Full-Scale Error – Positive Full-Scale Error = Positive Gain Error + Negative Gain Error

INTEGRAL NON-LINEARITY (INL) is a measure of worst case deviation of the ADC transfer function from an ideal straight line drawn through the ADC transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The best fit method is used.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$$V_{FS} / 2^N$$

where V_{FS} is the differential full-scale amplitude V_{IN} as set by the FSR input and "N" is the ADC resolution in bits, which is 8, for the ADC08D1520QML.

LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) DIFFERENTIAL OUTPUT VOLTAGE (V_{OD}) is the absolute value of the difference between the V_D+ and V_D- outputs; each measured with respect to Ground.

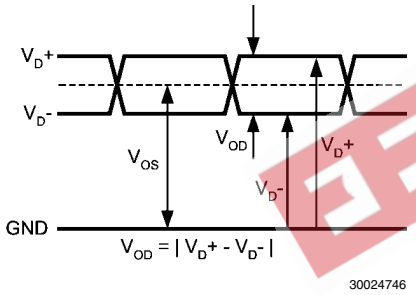


FIGURE 1.

LVDS OUTPUT OFFSET VOLTAGE (V_{OS}) is the midpoint between the D+ and D- pins output voltage with respect to ground; ie., [(V_D+) +(V_D-)]/2.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL-SCALE ERROR (NFSE) is a measure of how far the first code transition is from the ideal 1/2 LSB above a differential $–V_{IN}$/2 with the FSR pin low. For the ADC08D1520QML the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

OFFSET ERROR (V_{OFF}) is a measure of how far the mid-scale point is from the ideal zero voltage differential input.

Offset Error = Actual Input causing average of 8k samples to result in an average code of 127.5.

OUTPUT DELAY (t_{OD}) is the time delay (in addition to Pipeline Delay) after the falling edge of CLK+ before the data update is present at the output pins.

OVER-RANGE RECOVERY TIME is the time required after the differential input voltages goes from ±1.2V to 0V for the converter to recover and make a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of input clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the t_{OD}.

POSITIVE FULL-SCALE ERROR (PFSE) is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential $+V_{IN}$/2. For the ADC08D1520QML the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

POWER SUPPLY REJECTION RATIO (PSRR) can be one of two specifications. PSRR1 (DC PSRR) is the ratio of the change in full-scale error that results from a power supply voltage change from 1.8V to 2.0V. PSRR2 (AC PSRR) is a measure of how well an a.c. signal riding upon the power supply is rejected from the output and is measured with a 248 MHz, 50 mV_{P-P} signal riding upon the power supply. It is the ratio of the output amplitude of that signal at the output to its amplitude on the power supply pin. PSRR is expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the input clock frequency, including harmonics but excluding d.c.

SPURIOUS-FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding d.c.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$\text{THD} = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}}$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

– Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3rd Harm) is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

Transfer Characteristic

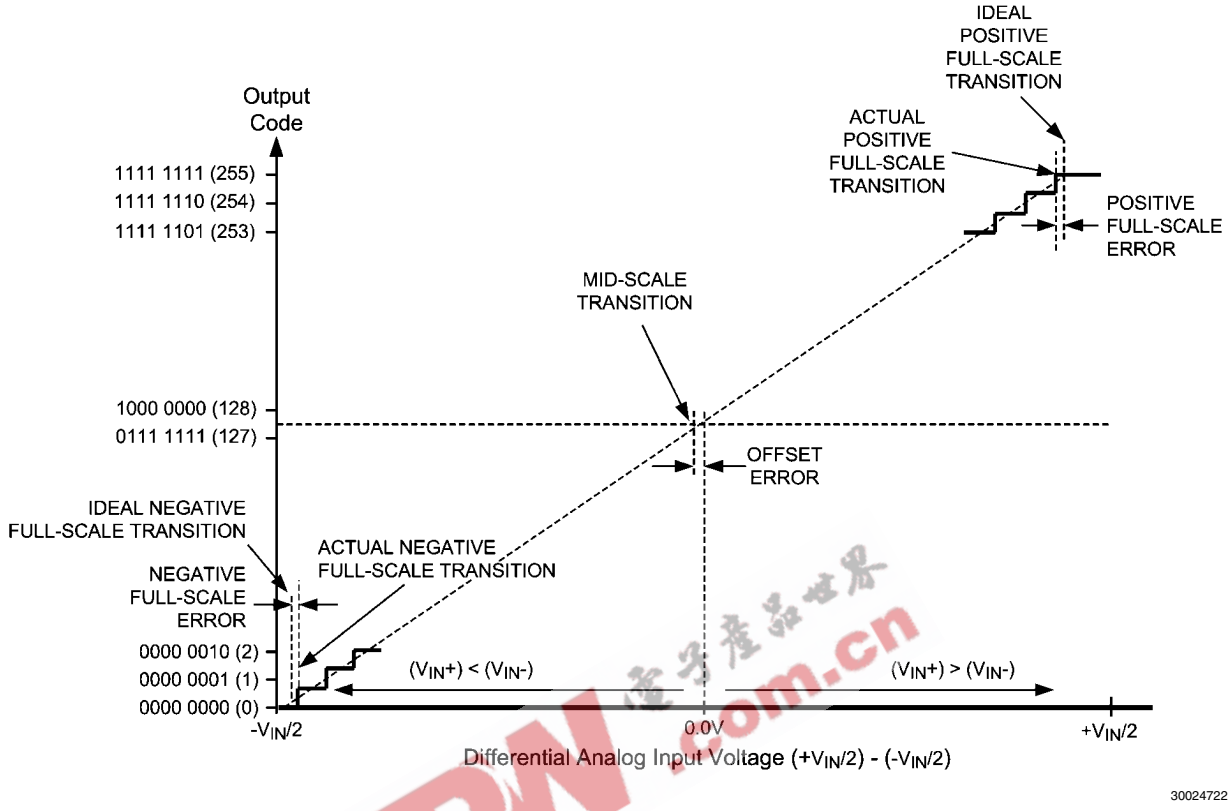


FIGURE 2. Input / Output Transfer Characteristic

Timing Diagrams

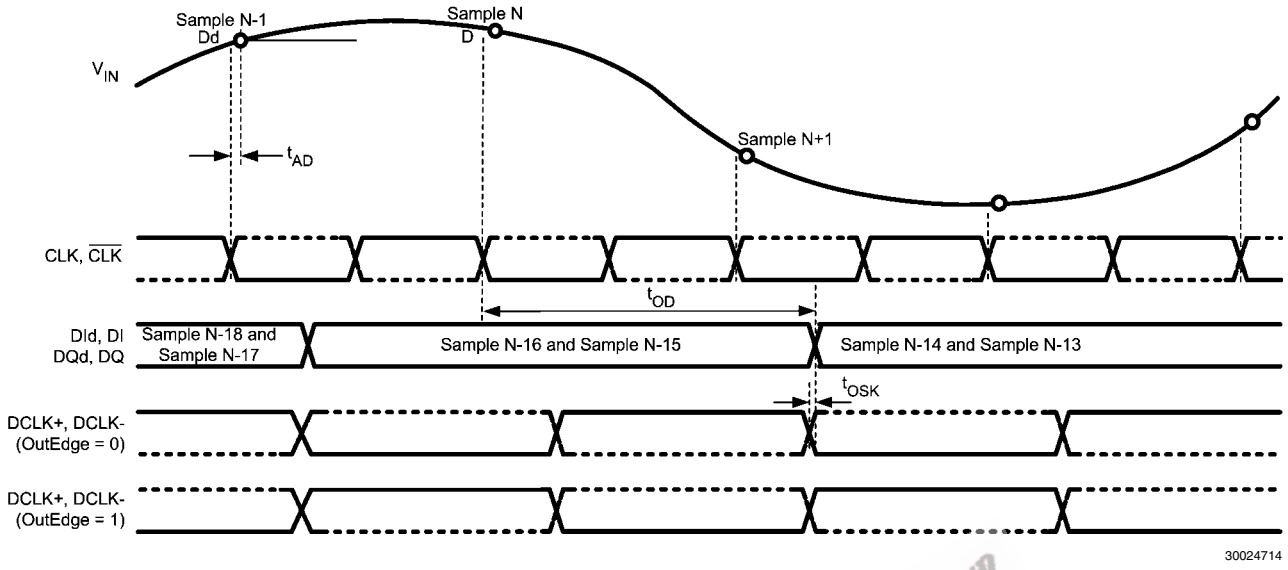


FIGURE 3. SDR Clocking in 1:2 Demultiplexed Mode

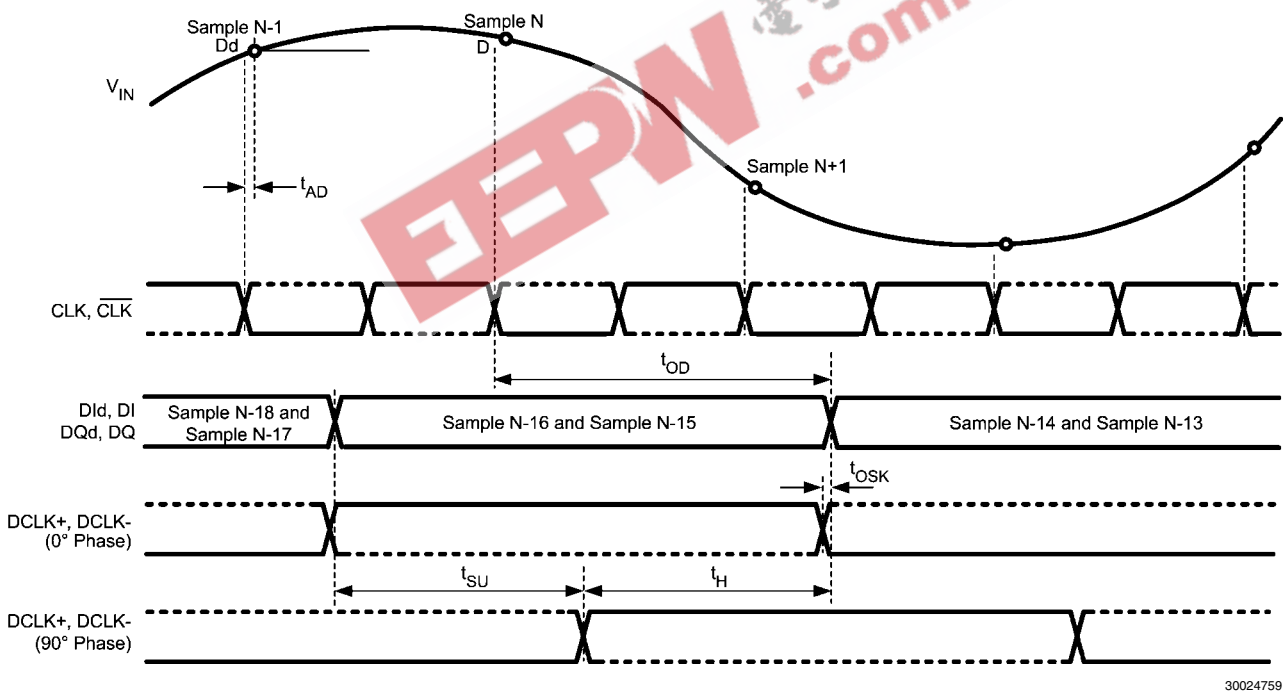


FIGURE 4. DDR Clocking in 1:2 Demultiplexed and Non-DES Mode

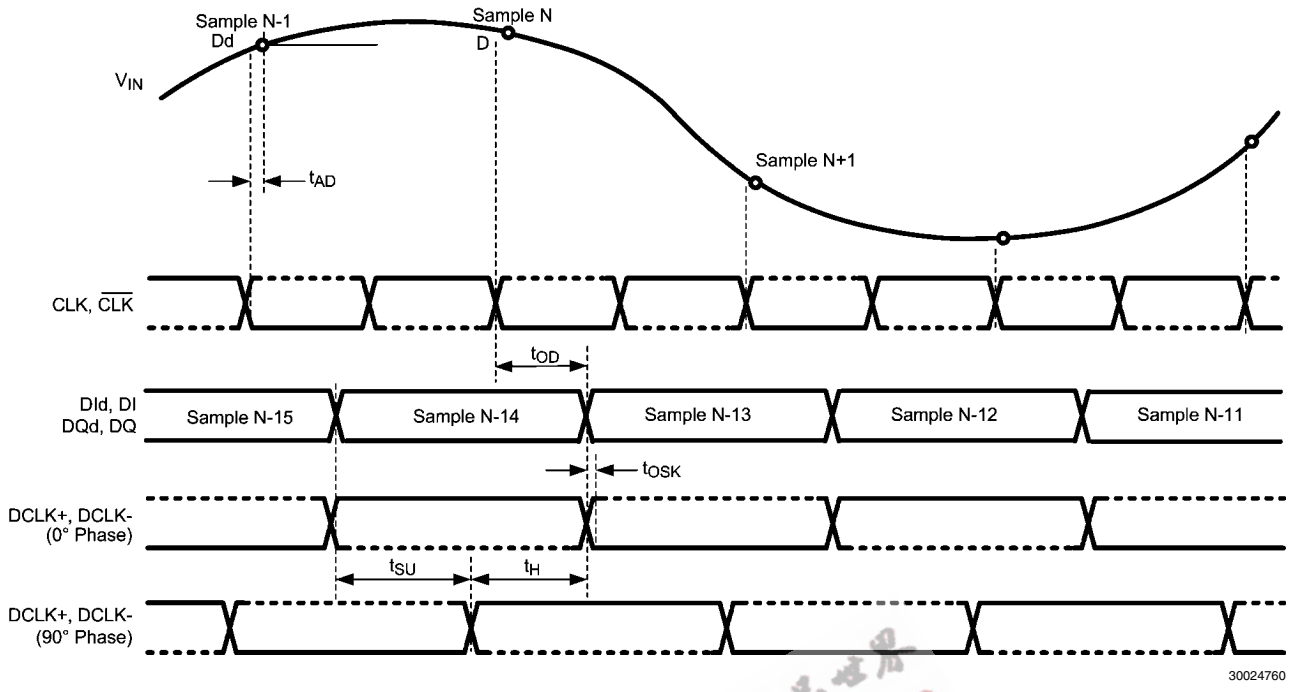


FIGURE 5. DDR Clocking in Non-Demultiplexed and Non-DES Mode

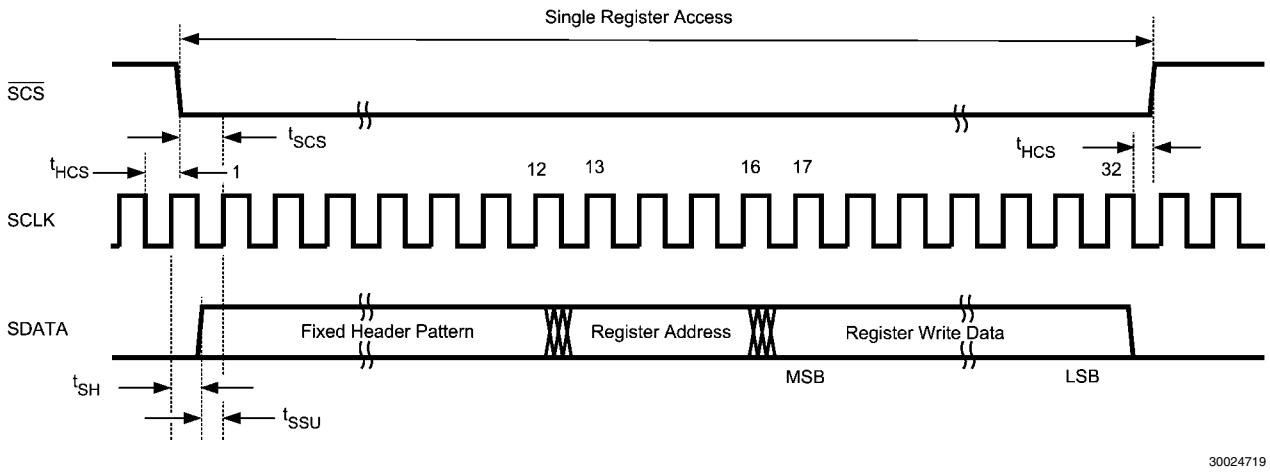


FIGURE 6. Serial Interface Timing

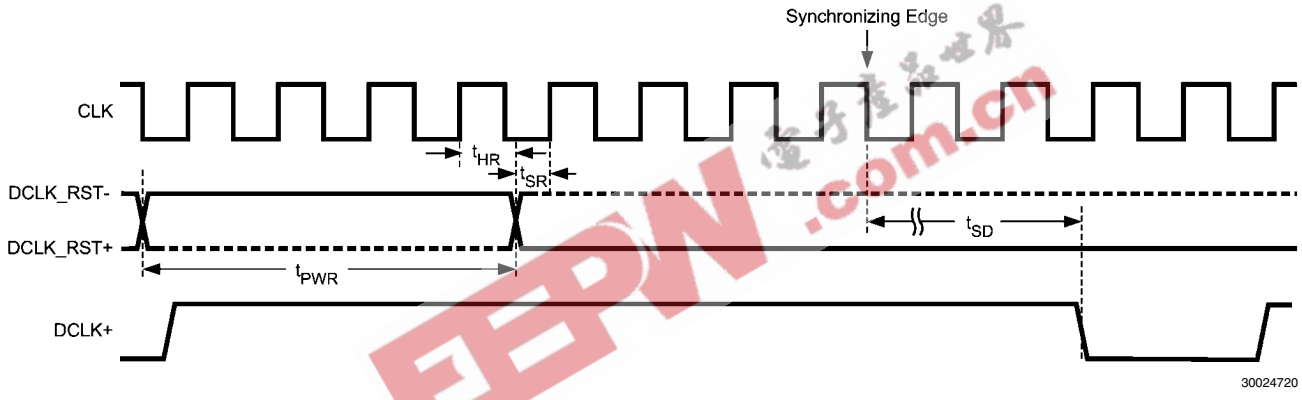


FIGURE 7. Clock Reset Timing in DDR Mode

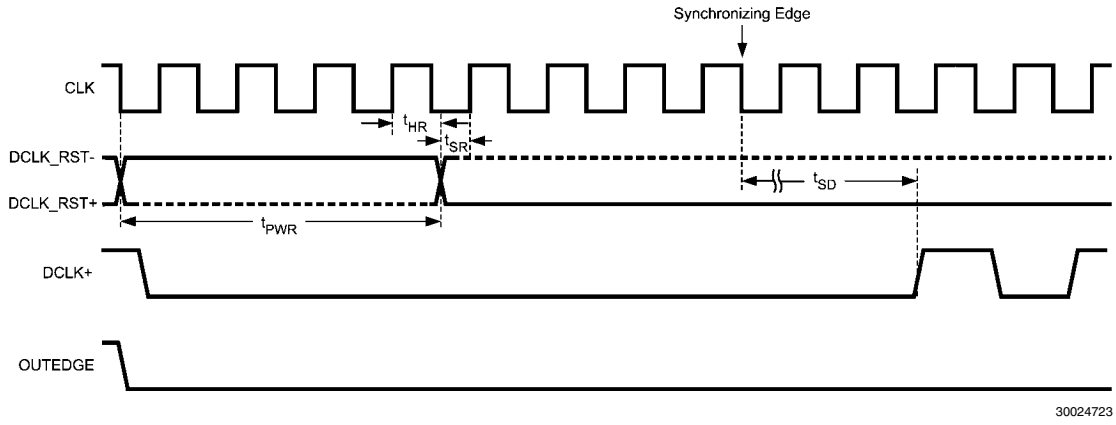


FIGURE 8. Clock Reset Timing in SDR Mode with OUTEDGE Low

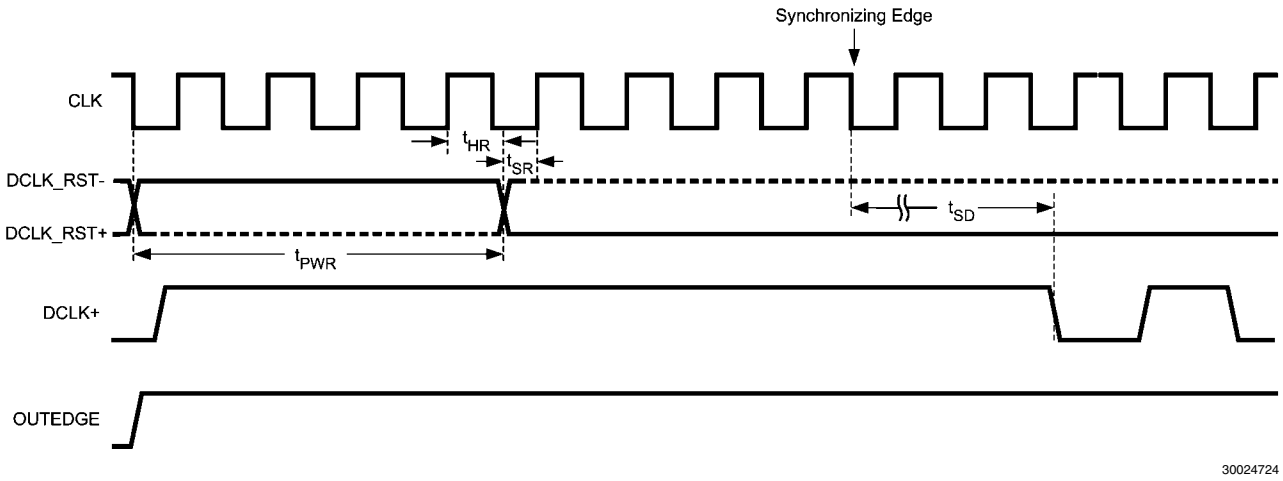


FIGURE 9. Clock Reset Timing in SDR Mode with OUTEDGE High

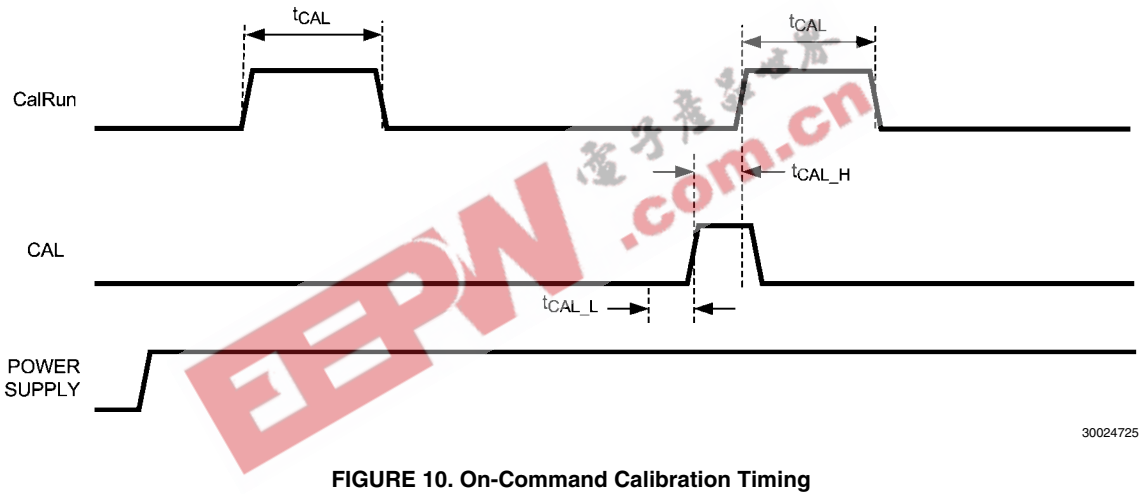
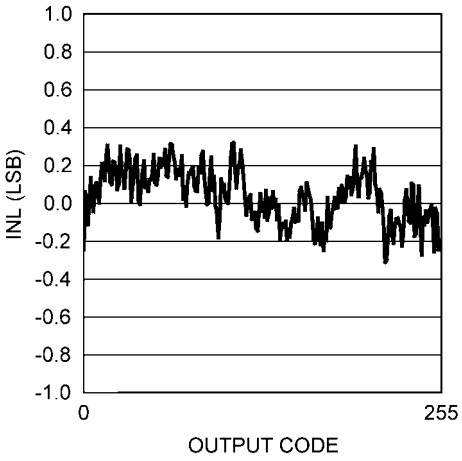


FIGURE 10. On-Command Calibration Timing

Typical Performance Characteristics

$V_A = V_{DR} = 1.9V$, $f_{CLK} = 1500$ MHz, $T_A = 25°C$, 1:2 Demux mode, Non-DES Mode unless otherwise stated.

INL vs CODE



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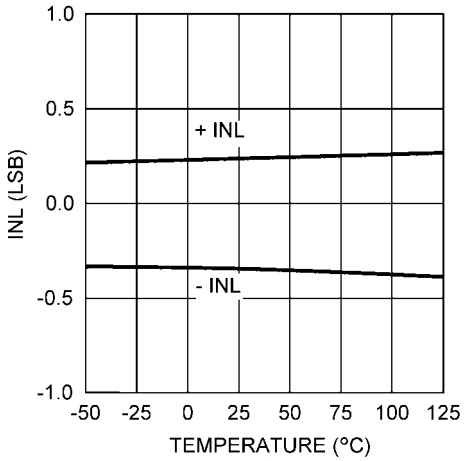
INL vs TEMPERATURE



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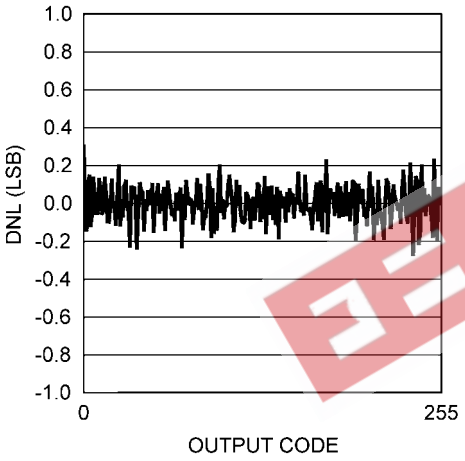
DNL vs. CODE



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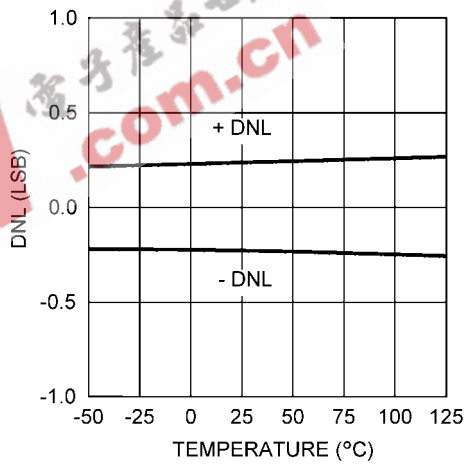
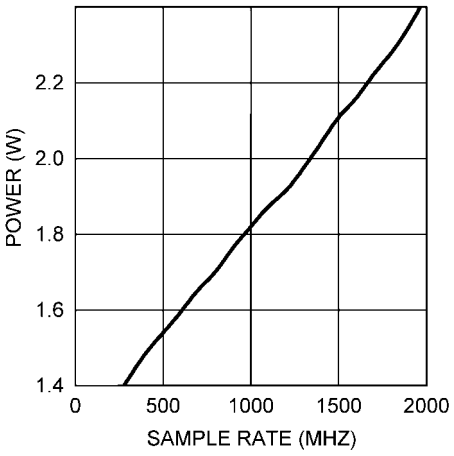
DNL vs. TEMPERATURE



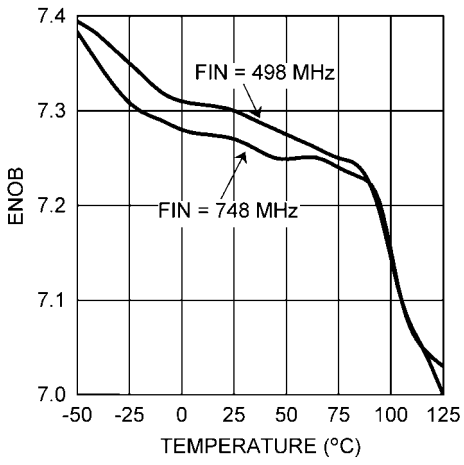
30024767

POWER DISSIPATION vs. SAMPLE RATE



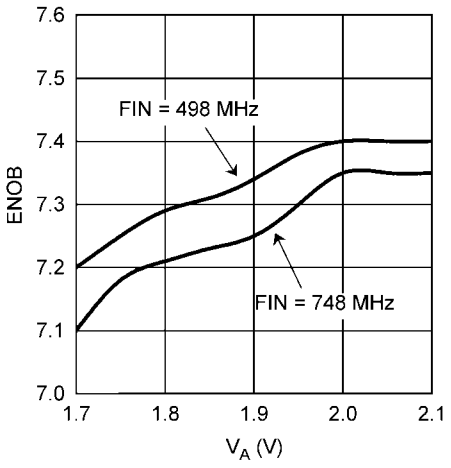
30024781

ENOB vs. TEMPERATURE



30024776

ENOB vs. SUPPLY VOLTAGE



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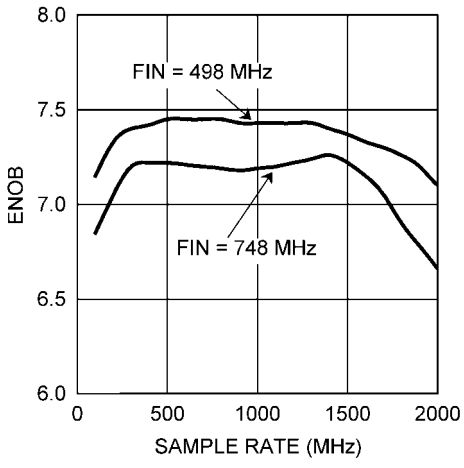
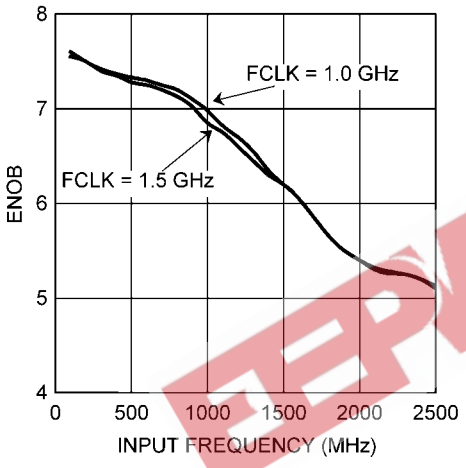
ENOB vs. SAMPLE RATE



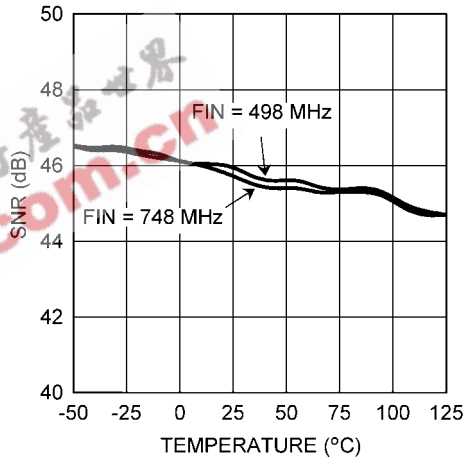
30024778

ENOB vs. INPUT FREQUENCY



30024779

SNR vs. TEMPERATURE



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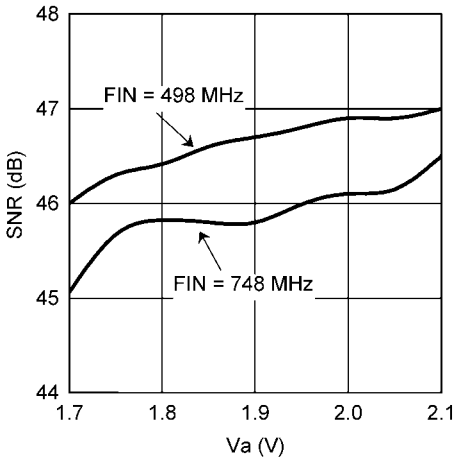
SNR vs. SUPPLY VOLTAGE



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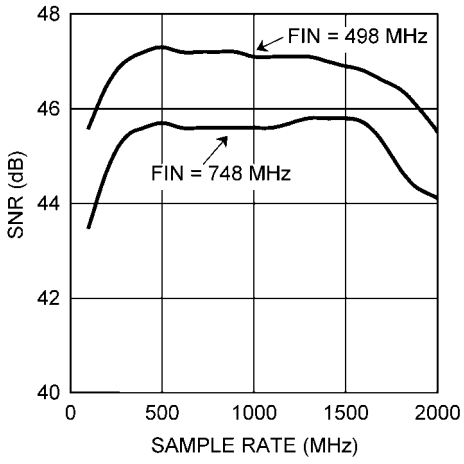
SNR vs. SAMPLE RATE



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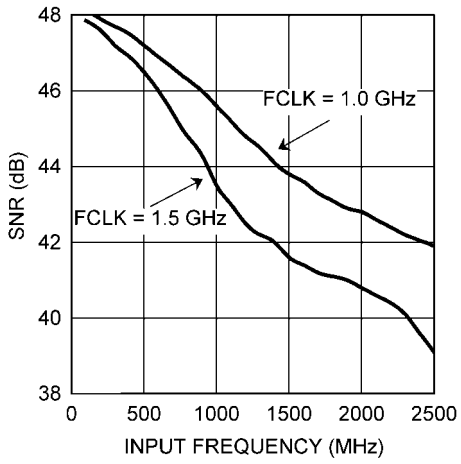
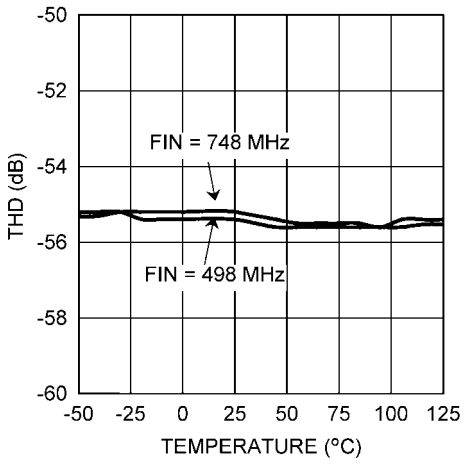
SNR vs. INPUT FREQUENCY



30024771

THD vs. TEMPERATURE



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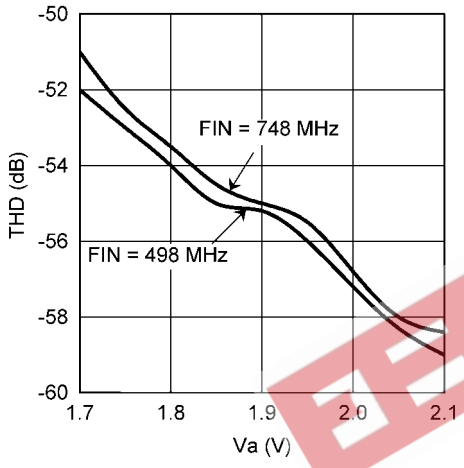
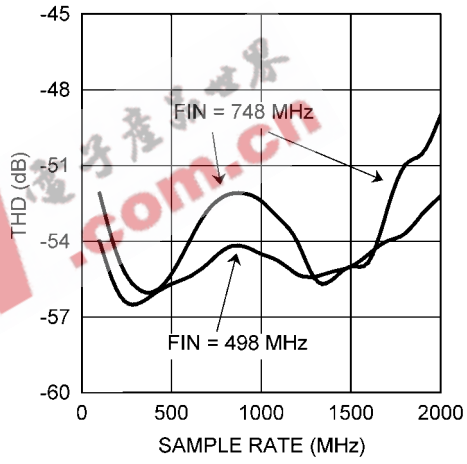
THD vs. SUPPLY VOLTAGE



30024773

THD vs. SAMPLE RATE



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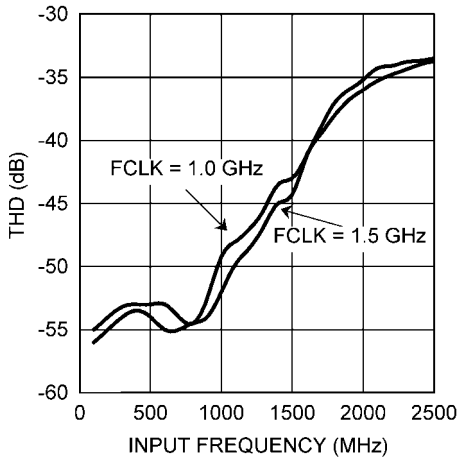
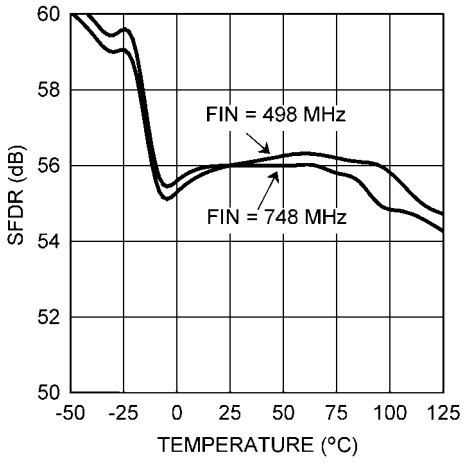
THD vs. INPUT FREQUENCY



30024775

SFDR vs. TEMPERATURE



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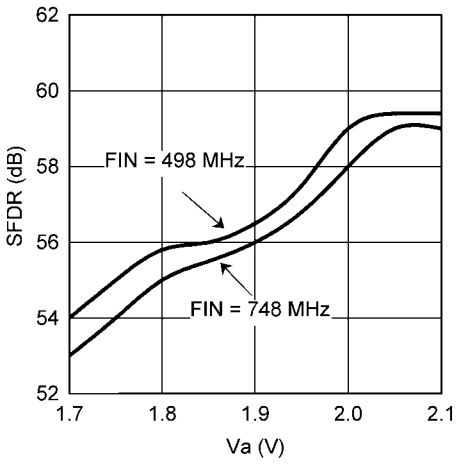
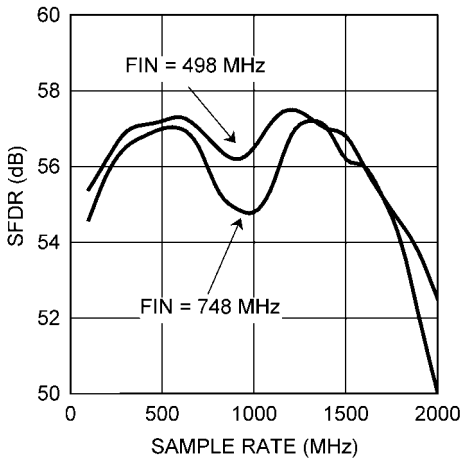
SFDR vs. SUPPLY VOLTAGE



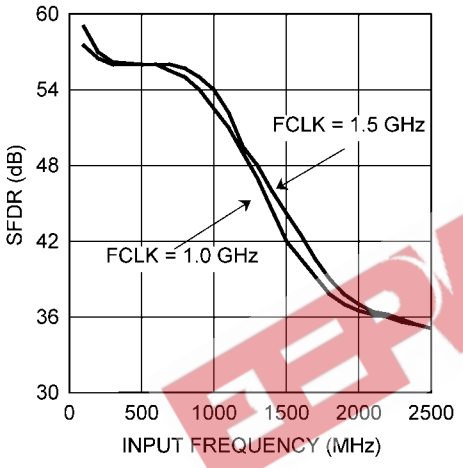
30024784

SFDR vs. SAMPLE RATE



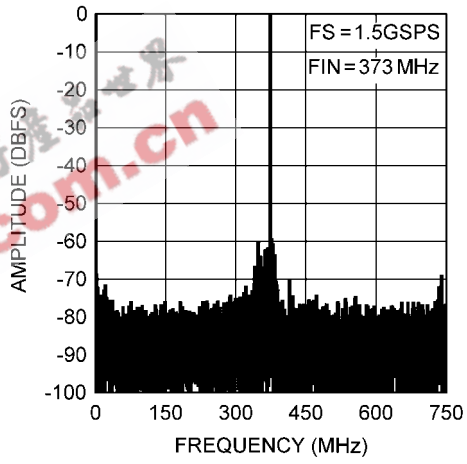
30024782

SFDR vs. INPUT FREQUENCY



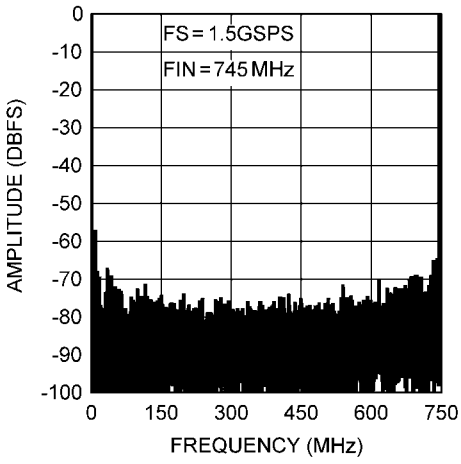
30024783

Spectral Response at FIN = 373 MHz



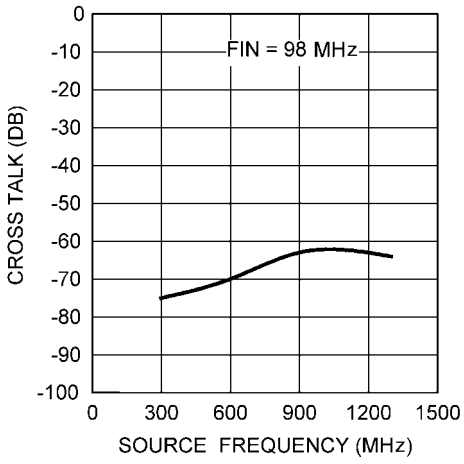
30024787

Spectral Response at FIN = 745 MHz



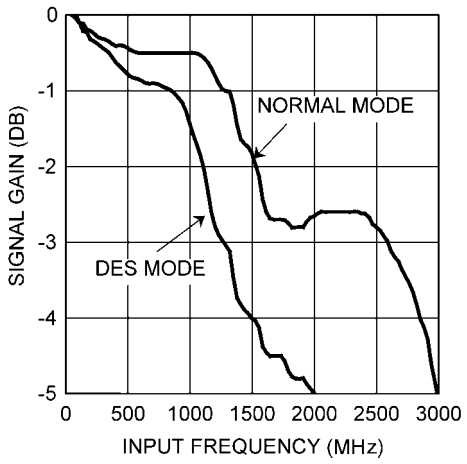
30024788

CROSSTALK vs SOURCE FREQUENCY



30024763

FULL POWER BANDWIDTH



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1.0 Functional Description

The ADC08D1520QML is a versatile A/D Converter with an innovative architecture permitting very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the Applications Information Section.

While it is not recommended in radiation environments to allow an active pin to float, pins 4, 14, 52 and 127 of the ADC08D1520QML are designed to be left floating without jeopardy in non radiation environments. In all discussions throughout this data sheet, whenever a function is called by allowing a control pin to float, connecting that pin to a potential of one half the V_A supply voltage is recommended for radiation environments.

1.1 OVERVIEW

The ADC08D1520QML uses a calibrated folding and interpolating architecture that achieves over 7.25 effective bits. The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to other things, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter.

The analog input signal that is within the converter's input voltage range is digitized to eight bits at speeds of 200 MSPS to 1.7 GSPS, typical. Differential input voltages below negative full-scale will cause the output word to consist of all zeroes. Differential input voltages above positive full-scale will cause the output word to consist of all ones. Either of these conditions at either the I- or Q- Channel input will cause the OR (Out of Range) output to be activated. This single OR output indicates when the output code from one or both of the channels is below negative full scale or above positive full scale.

Each converter has a selectable output demultiplexer which feeds two LVDS buses. If the 1:2 Demultiplexed Mode is selected, the output data rate is reduced to half the input sample rate on each bus. When Non-Demultiplexed Mode is selected, that output data rate on channels DI and DQ are at the same rate as the input sample clock.

The output levels may be selected to be normal or reduced. Using reduced levels saves power but could result in erroneous data capture of some or all of the bits, especially at higher sample rates and in marginally designed systems.

1.1.1 Calibration

The ADC08D1520QML has a calibration feature which must be invoked by the user. If the device is powered-up in the Extended Control Mode, the registers will be in an unknown state and no calibration is performed. For the initial calibration after power-up, we recommend that the registers first be programmed to a known state before performing a calibration or the part be calibrated in the pin control mode. All subsequent calibrations can be run in either the Non-Extended Control Mode or the Extended Control Mode.

The calibration algorithm consists of two portions. The first portion is calibrating the analog input. This calibration trims the 100 Ω analog input differential termination resistor and minimizes full-scale error, offset error, DNL and INL, resulting in maximizing SNR, THD, SINAD (SNDR) and ENOB. This portion of the calibration can be disabled by programming the Resistor Trim Disable (RTD) bit in the Extended Configuration register in the Extended Control Mode. Disabling the input termination resistor is not recommended for the initial calibration after power-up. The second portion of the calibration cycle is the ADC calibration in which internal bias currents are set. The ADC calibration is performed regardless of the RTD bit setting. Running the calibration is an important part of this chip's functionality and is required in order to obtain specified performance. In addition to the requirement that a calibration be run at power-up, a calibration must be run whenever the FSR pin is changed. For best performance, we recommend that a calibration be run after application of power once the power supplies have settled and the part temperature has stabilized. Further calibrations should be run whenever the operating temperature changes significantly relative to the specific system performance requirements. See *2.5.2.1 Initiating Calibration* for more information. Calibration can not be initiated or run while the device is in the Power-Down Mode. See *1.1.7 Power Down* for information on the interaction between Power down and calibration.

In normal operation, calibration should be performed just after application of power and whenever a valid calibration command is given. A calibration command can be issued using two methods. The first method is to hold the CAL pin low for at least t_{CAL_L} input clock cycles, then hold it high for at least another t_{CAL_H} input clock cycles as defined in the Converter Electrical Characteristics. The second method is to program the CAL bit in the Calibration register. The functionality of the CAL bit is exactly the same as using the CAL pin. The CAL bit must be programmed to 0b for t_{CAL_L} input clock cycles and then programmed to 1b for at least t_{CAL_H} input clock cycles to initiate a calibration cycle. The time taken by the calibration procedure is specified as t_{CAL} in the Converter Electrical Characteristics.

The CAL bit does not reset itself to zero automatically, but must be manually reset before another calibration event is desired, the CAL bit may be left high indefinitely, with no negative consequences.

The RTD bit setting is critical for running a calibration event with the Clock Phase Adjust enabled. If initiating a calibration event while the Clock Phase Adjust is enabled, the RTD bit must be set to high, or no calibration will occur. If initiating a calibration event while the Clock Phase Adjust is not enabled, a normal calibration will occur, regardless of the setting of the RTD bit.

Calibration Operation Notes:

- During the calibration cycle, the OR output may be active as a result of the calibration algorithm. All data on the output pins and the OR output are invalid during the calibration cycle.
- During the calibration, all clocks are halted on chip, including internal clocks and DCLK, while the input termination resistor is trimmed to a value that is equal to R_{EXT} / 33. This is to reduce noise during the input resistor calibration portion of the calibration cycle. See for information on maintaining DCLK operation during on-command calibration.
  This external resistor is located between pin 32 and ground. R_{EXT} must be 3300 Ω ±0.1%. With this value, the input termination resistor is trimmed to be 100 Ω. Because R_{EXT} is also used to set the proper current for the Track and Hold amplifier, for the preamplifiers and for the comparators, other values of R_{EXT} should not be used.
- The CalRun output is high whenever the calibration procedure is running. This is true whether the calibration is done at power-up or on-command.

- It is important that no digital activity take place on any of the digital input lines during the calibration process, except that there must be a stable, constant frequency CLK signal present and that SCLK may be active if the Enhanced Mode is selected. Actions that are not allowed include but are not limited to:
  Changing OUTV
  Changing OutEdge or SDATA sense
  Changing between SDR and DDR
  Changing FSE or ECE
  Changing DCLK_RST
  Changing SCS
  Raising PD high
  Raising CAL high
- Doing any of these actions can cause faulty calibration.

1.1.2 Acquiring the Input

Data is acquired at the falling edge of CLK+ (pin 18) and the digital equivalent of that data is available at the digital outputs 13 input clock cycles later for the DI and DQ output buses and 14 input clock cycles later for the DId and DQd output buses. There is an additional internal delay called t_{OD} before the data is available at the outputs. See the Timing Diagram. The ADC08D1520QML will convert as long as the input clock signal is present. The fully differential comparator design and the innovative design of the sample-and-hold amplifier, together with self calibration, enables a very flat SINAD/ENOB response beyond 1.5 GHz. The ADC08D1520QML output data signaling is LVDS and the output format is offset binary.

1.1.3 Control Modes

Much of the user control can be accomplished with several control pins that are provided. Examples include initiation of the calibration cycle, Power Down Mode and full scale range setting. However, the ADC08D1520QML also provides an Extended Control mode whereby a serial interface is used to access register-based control of several advanced features. The Extended Control mode is not intended to be enabled and disabled dynamically. Rather, the user is expected to employ either the Non-Extended Control Mode or the Extended Control Mode at all times. When the device is in the Extended Control Mode, pin-based control of several features is replaced with register-based control and those pin-based controls are disabled. These pins are OutV (pin 3), OutEdge/DDR (pin 4), FSR (pin 14) and DES (pin 127). See *1.2 NON-EXTENDED CONTROL/EXTENDED CONTROL* for details on the Extended Control Mode.

1.1.4 The Analog Inputs

The ADC08D1520QML must be driven with a differential input signal. Operation with a single-ended signal is not recommended. It is important that the input signals are a.c. coupled to the inputs.

Two full-scale range settings are provided with pin 14 (FSR). A high on pin 14 causes an input full-scale range setting of a higher V_{IN} input level, while grounding pin 14 causes an input full-scale range setting of a reduced V_{IN} input level. The full-scale range setting operates equally on both ADCs.

In the Extended Control Mode, the Input Full-Scale Voltage Adjust register allows the input full-scale range to be adjusted as described in *1.4 REGISTER DESCRIPTION* and *2.3 THE ANALOG INPUT*.

1.1.5 Clocking

The ADC08D1520QML must be driven with an a.c. coupled, differential clock signal. *2.4 THE CLOCK INPUTS* describes the use of the clock input pins. A differential LVDS output clock is available for use in latching the ADC output data into whatever device is used to receive the data.

The ADC08D1520QML offers input and output clocking options. These options include a choice of Dual Edge Sampling (DES) or "interleaved mode" where the ADC08D1520QML performs as a single device converting at twice the input clock rate, a choice of which DCLK edge the output data transitions on, and a choice of Single Data Rate (SDR) or Double Data Rate (DDR) outputs.

The ADC08D1520QML also has the option to use a duty cycle corrected clock receiver as part of the input clock circuit. **This feature is enabled by default and provides improved ADC clocking especially in the Dual-Edge Sampling Mode (DES). This circuitry allows the ADC to be clocked with a signal source having a duty cycle ratio of 20%/80% (worst case) for both the Non-DES and the Dual Edge Sampling Modes.**

1.1.5.1 Dual-Edge Sampling

The DES Mode allows one of the ADC08D1520QML's inputs (I- or Q- Channel) to be sampled by both ADCs. One ADC samples the input on the positive edge of the input clock and the other ADC samples the same input on the other edge of the input clock. A single input is thus sampled twice per input clock cycle, resulting in an overall sample rate of twice the input clock frequency, or 3 GSPS with a 1.5 GHz input clock.

In this mode, the outputs must be carefully interleaved to reconstruct the sampled signal. If the device is programmed into the 1:2 Demultiplex Mode while in DES Mode, the data is effectively Demultiplexed 1:4. If the input clock is 1.5 GHz, the effective sampling rate is doubled to 3 GSPS and each of the 4 output buses have a 750 MHz output rate. All data is available in parallel. To properly reconstruct the sampled waveform, the four bytes of parallel data that are output with each clock are in the following sampling order from the earliest to the latest and must be interleaved as such: DQd, DId, DQ, DI. *Table 1* indicates what the outputs represent for the various sampling possibilities. If the device is programmed into the Non-Demultiplex Mode, two bytes of parallel data are output with each edge of the clock in the following sampling order, from the earliest to the latest: DQ, DI. See *Table 2*.

In the Non-Extended Control Mode of operation only the I-channel input can be sampled in the DES Mode. In the Extended Control Mode of operation, the user can select which input is sampled.

The ADC08D1520QML also includes an automatic clock phase background calibration feature which can be used in DES Mode to automatically and continuously adjust the clock phase of the I- and Q- channel. This feature removes the need to adjust the clock phase setting manually and provides optimal Dual-Edge Sampling ENOB performance.

IMPORTANT NOTE: The background calibration feature in DES Mode does not replace the requirement for calibration if a large swing in ambient temperature is experienced by the device.

TABLE 1. Input Channel Samples Produced at Data Outputs in 1:2 Demultiplexed Mode**

Data Outputs (Always sourced with respect to fall of DCLK+)	Non DES Sampling Mode	Dual-Edge Sampling Mode (DES)	
		I- Channel Selected	Q- Channel Selected *
DI	I- Channel Input Sampled with Fall of CLK 13 cycles earlier.	I- Channel Input Sampled with Fall of CLK 13 cycles earlier.	Q- Channel Input Sampled with Fall of CLK 13 cycles earlier.
DId	I- Channel Input Sampled with Fall of CLK 14 cycles earlier.	I- Channel Input Sampled with Fall of CLK 14 cycles earlier.	Q- Channel Input Sampled with Fall of CLK 14 cycles earlier.
DQ	Q- Channel Input Sampled with Fall of CLK 13 cycles earlier.	I- Channel Input Sampled with Rise of CLK 13.5 cycles earlier.	Q- Channel Input Sampled with Rise of CLK 13.5 cycles earlier.
DQd	Q- Channel Input Sampled with Fall of CLK 14 cycles earlier.	I- Channel Input Sampled with Rise of CLK 14.5 cycles earlier.	Q- Channel Input Sampled with Rise of CLK 14.5 cycles earlier.

* Note that, in DES + Non-DES Mode, only the I- Channel is sampled. In DES + Extended Control Mode, I- Channel or Q- Channel can be sampled.

** Note that, in the Non-Demultiplexed Mode, the DId and DQd outputs are disabled and are high impedance.

TABLE 2. Input Channel Samples Produced at Data Outputs in 1:1 Demultiplexed Mode

Data Outputs (Sourced with respect to fall of DCLK+)	Non-DES Mode	DES Mode
DI	I- Channel Input Sampled with Fall of CLK 13 cycles earlier.	I- Channel Input Sampled with Fall of CLK 13 cycles earlier.
DId	No output.	No output.
DQ	Q- Channel Input Sampled with Fall of CLK 13 cycles earlier.	Q- Channel Input Sampled with Fall of CLK 13.5 cycles earlier.
DQd	No output.	No output.

1.1.5.2 OutEdge and Demultiplex Control Setting

To help ease data capture in the SDR Mode, the output data may be caused to transition on either the positive or the negative edge of the output data clock (DCLK). In the Non-Extended Control Mode, this is chosen with the OutEdge input (pin 4). A high on the OutEdge input pin causes the output data to transition on the rising edge of DCLK+, while grounding this input causes the output to transition on the falling edge of DCLK. See *2.5.3 Output Edge Synchronization*. When in the Extended Control Mode, the OutEdge is selected using the OED bit in the Configuration Register. This bit has two functions. In the single data rate (SDR) Mode, the bit functions as OutEdge and selects the DCLK edge with which the data transitions. In the Double Data Rate (DDR) Mode, this bit selects whether the device is in Non-Demultiplex or 1:2 Demultiplex Mode. In the DDR case, the DCLK has a 0° phase relationship with the output data independent of the demultiplexer selection.

For 1:2 Demux DDR 0 deg Mode, there are five, as opposed to four cycles of CLK delay from the deassertion of DCLK_RST to the Synchronizing Edge. See *1.5 MULTIPLE ADC SYNCHRONIZATION*

1.1.5.3 Double Data Rate

A choice of single data rate (SDR) or double data rate (DDR) output is offered. With single data rate the output clock (DCLK) frequency is the same as the data rate of the two output buses. With double data rate the DCLK frequency is half the data rate and data is sent to the outputs on both edges of DCLK. DDR clocking is enabled in Non-Extended Control Mode by tying pin 4 to $V_A/2$.

1.1.5.4 Clocking Summary

The chip may be in one of four modes, depending on the Dual-Edge Sampling (DES) selection and the demultiplex selection. For the DES selection, there are two possibilities: Non-DES Mode and DES Mode. In Non-DES Mode, each of the channels (I-channel and Q-channel) functions independently, i.e. the chip is a dual 1.5 GSPS A/D converter. In DES Mode, the I- and Q-channels are interleaved and function together as one 3.0 GSPS A/D converter. For the demultiplex selection, there are also two possibilities: Demux Mode and Non-Demux Mode. The I-channel has two 8-bit output busses associated with it: DI and DId. The Q-channel also has two 8-bit output busses associated with it: DQ and DQd. In Demux Mode, the channel is demultiplexed by 1:2. In Non-Demux Mode, the channel is not demultiplexed. Note that Non-Demux Mode is also sometimes referred to as 1:1 Demux Mode. For example, if the I-channel was in Non-Demux Mode, the corresponding digital output data would be available on only the DI bus. If the I-channel was in Demux Mode, the corresponding digital output data would be available on both the DI and DId busses, but at half the rate of Non-Demux Mode.

Given that there are two DES Mode selections (DES Mode and Non-DES Mode) and two demultiplex selections (Demux Mode and Non-Demux Mode), this yields a total of four pos-

sible modes: (1) Non-Demux Mode, (2) Non-Demux DES Mode, (3) 1:2 Demux Non-DES Mode, and (4) 1:4 Demux DES Mode. The following is a brief explanation of the terms and modes:

1. Non-Demux Mode: This mode is when the chip is in Non-Demux Mode and Non-DES Mode, but it is shortened to simply "Non-Demux Mode." The I- and Q- channels function independently of one another. The digital output data is available for the I- channel on DI, and for the Q- channel on DQ.
2. Non-Demux DES Mode: This mode is when the chip is in Non-Demux Mode and DES Mode. The I- and Q- channels are interleaved and function together as one channel. The digital output data is available on the DI and DQ busses because although the chip is in Non-Demux Mode, both I- and Q- channels are functioning and passing data.
3. 1:2 Demux Non-DES Mode: This mode is when the chip is in Demux Mode and Non-DES Mode. The I- and Q- channels function independently of one another. The digital output data is available for the I- channel on DI and DId, and for the Q- channel on DQ and DQd. This is because each channel (I- channel and Q- channel) is providing digital data in a demultiplexed manner.
4. 1:4 Demux DES Mode: This mode is when the chip is in Demux Mode and DES Mode. The I- and Q- channels are interleaved and function together as one channel. The digital output data is available on the DI, DId, DQ and DQd busses because although the chip is in Demux Mode, both I- and Q- channels are functioning and passing data. To avoid confusion, this mode is labeled 1:4 because the analog input signal is provided on one channel and the digital output data is provided on four busses.

The choice of Dual Data Rate (DDR) and Single Data Rate (SDR) will only affect the speed of the output Data Clock (DCLK). Once the DES Modes and Demux Modes have been chosen, the data output rate is also fixed. In the case of SDR, the DCLK runs at the same rate as the output data; output data may transition with either the rising or falling edge of DCLK. In the case of DDR, the DCLK runs at half the rate of the output data; the output data transitions on both rising and falling edges of the DCLK.

1.1.6 The LVDS Outputs

The data outputs, the Out Of Range (OR) and DCLK, are LVDS. Output current sources provide 3 mA of output current to a differential 100 Ohm load when the OutV input (pin 14) is high or 2.2 mA when the OutV input is low. For short LVDS lines and low noise systems, satisfactory performance may be realized with the OutV input low, which results in lower power consumption. If the LVDS lines are long and/or the system in which the ADC08D1520QML is used is noisy, it may be necessary to tie the OutV pin high.

The LVDS data output have a typical common mode voltage of 800 mV when the V_{BG} pin is left floating. This common mode voltage can be increased to 1.1V by tying the V_{BG} pin to V_A if a higher common mode is required.

IMPORTANT NOTE: Tying the V_{BG} pin to V_A will also increase the differential LVDS output voltage by up to 40mV.

1.1.7 Power Down

The ADC08D1520QML is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the Power Down Mode. In this Power Down Mode the data output pins (positive and negative) are put into a high impedance state and the devices power consumption is reduced to a minimal level. The DCLK+/- and OR +/- are not tri-stated, they are weakly pulled down to ground internally. Therefore when both I- Channel and Q- Channel are powered down the DCLK +/- and OR +/- should not be terminated to a DC voltage.

A high on the PDQ pin will power down the Q- Channel and leave the I- channel active. There is no provision to power down the I- Channel independently of the Q- Channel. Upon return to normal operation, the pipeline will contain meaningless information.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is simultaneously ramped, the device will not calibrate until the PD input goes low. If a calibration is requested while the device is powered down, the calibration request will be completely ignored. Calibration will function with the Q- Channel powered down, but that channel will not be calibrated if PDQ is high. If the Q- Channel is subsequently to be used, it is necessary to perform a calibration after PDQ is brought low.

1.2 NON-EXTENDED CONTROL/EXTENDED CONTROL

The ADC08D1520QML may be operated in one of two modes. In the simpler Non-Extended Control Mode, the user affects available configuration and control of the device through several control pins. The "Extended Control Mode" provides additional configuration and control options through a serial interface and a set of 9 registers. Extended Control Mode is selected by setting pin 41 to logic low. The choice of control modes is required to be a fixed selection and is not intended to be switched dynamically while the device is operational.

Table 3 shows how several of the device features are affected by the control mode chosen.

TABLE 3. Features and Modes

Feature	Non-Extended Control Mode	Extended Control Mode
SDR or DDR Clocking	Selected with pin 4	Selected with bit 10 nDE in the Configuration Register (Addr-1h; bit-10)
DDR Clock Phase	Not Selectable (0° Phase Only)	Selected with DCP in the Configuration Register (Addr-1h; bit-11)
SDR Data transitions with rising or falling DCLK edge	SDR Data transitions with rising edge of DCLK+ when pin 4 is high and on falling edge when low.	Selected with OED in the Configuration Register (Addr-1h; bit-8)
LVDS output level	Normal differential data and DCLK amplitude selected when pin 3 is high and reduced amplitude selected when low.	Selected with OV in the Configuration Register (Addr-1h; bit-9)
Full-Scale Range	Normal input full-scale range selected when pin 14 is high and reduced range when low. Selected range applies to both channels.	Up to 512 step adjustments over a nominal range specified in *1.4 REGISTER DESCRIPTION*. Separate range selected for I-Channel and Q- Channels. Selected using Full Range Registers (Addr-3h and Bh; bit-7 thru 15)
Input Offset Adjust	Not possible	512 steps of adjustment using the input Offset register specified in *1.4 REGISTER DESCRIPTION* for each channel using Input Offset registers (Addr-2h and Ah; bit-7 thru 15)
Dual Edge Sampling Selection	Enabled with pin 127 set to $V_A/2$	Enabled by programming DEN in the Extended Configuration Register (Addr-9h; bit-13)
Dual Edge Sampling Input Channel Selection	Only I-Channel Input can be used	Either I- Channel or Q- Channel input may be sampled by both ADCs.
Test Pattern	Not possible	A test pattern can be made present at the data outputs by setting TPO to 1b in Extented Configuration Register (Addr-9h; bit-15)
Resistor Trim Disable	Not possible	The DCLK outputs will continuously be present when RTD is set to 1b in Extented Configuration Register (Addr-9h; bit-14)
Selectable Output Demultiplexer	Not possible	If the device is set in DDR, the output can be programmed to be non-demultiplex. When OED in Configuration Register is set 1b (Addr-1h; 8-bit), this selects non-demultiplex. If OED is set 0b, this selects 1:2 demultiplex.
Second DCLK Output	Not possible	The OR outputs can be programmed to become a second DCLK output when nSD is set 0b in Configuration Register (Addr-1h; bit-13).
Sampling Clock Phase Adjust	Not possible	The sampling clock phase can be manually adjusted through the Coarse and Intermediate Register (Addr-Fh; bit-14 to 7) and Fine register (Addr-Dh; bit-15 to 8)

When the device is powered up in the Extended Control Mode, the Registers are loaded with invalid data and the Registers come up on an unknown state. Before initiating a calibration the registers must be written to and programmed into a known state. If the device is powered up in the Non-Extended Control Mode and the user switches to the Extended Control Mode after the part has stabilized, the registers will load with the register default states described in Table 4.

TABLE 4. Extended Control Mode Operation (Pin 41 Logic Low)

Feature	Extended Control Mode Default State
SDR or DDR Clocking	DDR Clocking
DDR Clock Phase	Data changes with DCLK edge (0° phase)
LVDS Output Amplitude	Normal amplitude (V_{OD})
Full-Scale Range	700 mV nominal for both channels
Input Offset Adjust	No adjustment for either channel
Dual Edge Sampling (DES)	Not enabled
Test Pattern	Not present at output
Resistor Trim Disable	Trim enabled, DCLK not continuously present at output
Selectable Output Demultiplexer	1:2 demultiplex
Second DCLK Output	Not present, pin 79 and 80 function as OR+ and OR-.
Sampling Clock Phase Adjust	No adjustment for fine, intermediate or coarse

1.3 THE SERIAL INTERFACE

The 3-pin serial interface is enabled only when the device is in the Extended Control mode. The pins of this interface are Serial Clock (SCLK), Serial Data (SDATA) and Serial Interface Chip Select ($\overline{SCS}$). Nine write only registers are accessible through this serial interface.

$\overline{SCS}$: This signal should be asserted low while accessing a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

SCLK: Serial data input is accepted at the rising edge of this signal.

SDATA: Each register access requires a specific 32-bit pattern at this input. This pattern consists of a header, register address and register value. The data is shifted in MSB first. Setup and hold times with respect to the SCLK must be observed. See the Timing Diagram.

Each Register access consists of 32 bits, as shown in *Figure 6* of the Timing Diagrams. The fixed header pattern is 0000 0000 0001 (eleven zeros followed by a 1). The loading sequence is such that a "0" is loaded first. These 12 bits form the header. The next 4 bits are the address of the register that is to be written to and the last 16 bits are the data written to the addressed register. The addresses of the various registers are indicated in *Table 5*.

Refer to the Register Description (*1.4 REGISTER DESCRIPTION*) for information on the data to be written to the registers.

Subsequent register accesses may be performed immediately, starting with the 33rd SCLK. This means that the $\overline{SCS}$ input does not have to be de-asserted and asserted again between register addresses. It is possible, although not recommended, to keep the $\overline{SCS}$ input permanently enabled (at a logic low) when using extended control.

IMPORTANT NOTE: Do not write to the Serial Interface when calibrating the ADC. Doing so will impair the performance of the device until it is re-calibrated correctly. Programming the serial registers will also reduce dynamic performance of the ADC for the duration of the register access time.

TABLE 5. Register Addresses

4-Bit Address					
Loading Sequence: A3 loaded after H0, A0 loaded last					
A3	A2	A1	A0	Hex	Register Addressed
0	0	0	0	0h	Calibration
0	0	0	1	1h	Configuration
0	0	1	0	2h	I- Ch Offset
0	0	1	1	3h	I- Ch Full-Scale Voltage Adjust
0	1	0	0	4h	Reserved
0	1	0	1	5h	Reserved
0	1	1	0	6h	Reserved
0	1	1	1	7h	Reserved
1	0	0	0	8h	Reserved
1	0	0	1	9h	Extended Configuration
1	0	1	0	Ah	Q- Ch Offset
1	0	1	1	Bh	Q- Ch Full-Scale Voltage Adjust
1	1	0	0	Ch	Reserved
1	1	0	1	Dh	Reserved
1	1	1	0	Eh	Sampling Clock Phase Fine Adjust
1	1	1	1	Fh	Sample Clock Phase Intermediate and Coarse Adjust

1.4 REGISTER DESCRIPTION

Nine write-only registers provide several control and configuration options in the Extended Control Mode. These registers have no effect when the device is in the Non-Extended Control Mode. Each register description below also shows the Register Default State.

Calibration Register

Addr: 0h (0000b) **Write only (0x7FFF)**

D15	D14	D13	D12	D11	D10	D9	D8
CAL	1	1	1	1	1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15 CAL: Calibration Enable. When this bit is set 1b, a command calibration cycle is initiated. This function is exactly the same as issuing a calibration using the CAL pin. See section 2.5.2.1, Initiating Calibration for details for usage.

Default State: 0b

Bits 14:0 Must be set to 1b

Configuration Register

Addr: 1h (0001b) **Write only (0xB2FF)**

D15	D14	D13	D12	D11	D10	D9	D8
1	0	nSD	DCS	DCP	nDE	OV	OED

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15 Must be set to 1b

Bit 14 Must be set to 0b

Bit 13 nSD: Second DCLK Output. When this bit is 1b, the device only has one DCLK output and one OR output. When this output is 0b, the device has two identical DCLK outputs and no OR output.

Default State: 1b

Bit 12 DCS: Duty Cycle Stabilizer. When this bit is set to 1b, a duty cycle stabilization circuit is applied to the clock input. When this bit is set to 0b the stabilization circuit is disabled.

Default State: 1b

Bit 11 DCP: DDR Clock Phase. This bit only has an effect in the DDR Mode. When this bit is set to 0b, the DCLK edges are time-aligned with the data bus edges ("0° Phase"). When this bit is set to 1b, the DCLK edges are placed in the middle of the data bit-cells ("90° Phase"), using the one-half speed DCLK shown in *Figure 4* as the phase reference.

Default State: 0b

Bit 10 nDE: DDR Enable. When this bit is set to 0b, data bus clocking follows the DDR (Double Data Rate) Mode whereby a data word is output with each rising and falling edge of DCLK. When this bit is set to a 1b, data bus clocking follows the SDR (single data rate) Mode whereby each data word is output with either the rising or falling edge of DCLK , as determined by the OutEdge bit.

Default State: 0b

Bit 9 OV: Output Voltage. This bit determines the LVDS outputs' voltage amplitude and has the same function as the OutV pin that is used in the Non-Extended Control Mode. When this bit is set to 1b, the standard output amplitude of 780 mV_{P-P} is used. When this bit is set to 0b, the reduced output amplitude of 590 mV_{P-P} is used.

Default State: 1b

Bit 8 OED: Output Edge and Demultiplex Control. This bit has two functions. When the device is in SDR Mode, this bit selects the DCLK edge with which the data words transition in the SDR Mode and has the same effect as the OutEdge pin in the Non-Extended Control Mode. When this bit is set to 1b, the data outputs change with the rising edge of DCLK +. When this bit is set to 0b, the data output changes with the falling edge of DCLK+. When the device is in DDR Mode, this bit selects the Non-Demultiplexed Mode when set to 1b. When the bit set to 0b, the device is programmed into the 1:2 Demultiplexed Mode. The 1:2 Demultiplexed Mode is the default mode. In DDR Mode, DCLK has a 0° phase relationship with the data.

Default State: 0b

Bits 7:0 Must be set to 1b

I-Channel Offset

Addr: 2h (0010b) **Write only (0x007F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)			Offset Value				(LSB)

D7	D6	D5	D4	D3	D2	D1	D0
Sign	1	1	1	1	1	1	1

Bits 15:8 Offset Value. The input offset of the I-Channel ADC is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero offset, while FFh provides a nominal 45 mV of offset. Thus, each code step provides 0.176 mV of offset.

Default State: 0000 0000 b

Bit 7 Sign bit. 0b gives positive offset, 1b gives negative offset.

Default State: 0b

Bit 6:0 Must be set to 1b

I-Channel Full-Scale Voltage Adjust

Addr: 3h (0011b) **Write only (0x807F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)	Adjust Value						

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bit 15:7 Full Scale Voltage Adjust Value. The input full-scale voltage or gain of the I-Channel ADC is adjusted linearly and monotonically with a 9 bit data value. The adjustment range is ±20% of the nominal 700 mV_{P-P} differential value.

0000 0000 0 560mV_{P-P}

1000 0000 0 700mV_{P-P}
Default Value

1111 1111 1 840mV_{P-P}

For best performance, it is recommended that the value in this field be limited to the range of 0110 0000 0b to 1110 0000 0b. i.e., limit the amount of adjustment to ±15%. The remaining ±5% headroom allows for the ADC's own full scale variation. A gain adjustment does not require ADC re-calibration.

Default State: 1000 0000 0b (no adjustment)

Bits 6:0 Must be set to 1b

Extended Configuration Register

Addr: 9h (1001b) **Write only (0x03FF)**

D15	D14	D13	D12	D11	D10	D9	D8
TPO	RTD	DEN	IS	0	DLF	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15 TPO: Test Pattern Output. When this bit is set 1b, the ADC is disengaged and a test pattern generator is connected to the outputs including OR. This test pattern will work with the device in the SDR, DDR and the Non-Demultiplex output modes.

Default State: 0b

Bit 14 RTD: Resistor Trim Disable. When this bit is set to 1b, the input termination resistor is not trimmed during the calibration cycle and the DCLK output remains enabled. Note that the ADC is calibrated regardless of this setting.

Default State: 0b

Bit 13 DES: DES Enable. Setting this bit to 1b enables the Dual Edge Sampling Mode. In this mode the ADCs in this device are used to sample and convert the same analog input in a time-interleaved manner, accomplishing a sample rate of twice the input clock rate. When this bit is set to 0b, the device operates in the Non-DES Mode.

Default State: 0b

Bit 12 IS: Input Select. When this bit is set to 0b the I- Channel input is operated upon by both ADCs. When this bit is set to 1b the Q-Channel input is operated on by both ADCs.

Default State: 0b

Bit 11 Must be set to 0b

Bit 10 DLF: DES Low Frequency. When this bit is set 1b, the dynamic performance of the device is improved when the input clock is less than 900 MHz.

Default State: 0b

Bits 9:0 Must be set to 1b

Q- Channel Offset

Addr: Ah (1010b) **Write only (0x007F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)	Offset Value						(LSB)

D7	D6	D5	D4	D3	D2	D1	D0
Sign	1	1	1	1	1	1	1

Bit 15:8 Offset Value. The input offset of the Q-Channel ADC is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero offset, while FFh provides a nominal 45 mV of offset. Thus, each code step provides about 0.176 mV of offset.

Default State: 0000 0000 b

Bit 7 Sign bit. 0b gives positive offset, 1b gives negative offset.

Default State: 0b

Bit 6:0 Must be set to 1b

Q- Channel Full-Scale Voltage Adjust

Addr: Bh (1011b) **Write only (0x807F)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)	Adjust Value						

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bit 15:7 Full Scale Voltage Adjust Value. The input full-scale voltage or gain of the I- Channel ADC is adjusted linearly and monotonically with a 9 bit data value. The adjustment range is ±20% of the nominal 700 mV_{P-P} differential value.

0000 0000 0 560 mV_{P-P}

1000 0000 0 700 mV_{P-P}

1111 1111 1 840 mV_{P-P}

For best performance, it is recommended that the value in this field be limited to the range of 0110 0000 0b to 1110 0000 0b. i.e., limit the amount of adjustment to ±15%. The remaining ±5% headroom allows for the ADC's own full scale variation. A gain adjustment does not require ADC re-calibration.

Default State: 1000 0000 0b (no adjustment)

Bits 6:0 Must be set to 1b

Sample Clock Phase Fine Adjust

Addr: Eh (1110b) **Write only (0x00FF)**

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)	Fine Phase Adjust						(LSB)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bits 15:8 Fine Phase Adjust. The phase of the ADC sampling clock is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero phase adjustment, while FFh provides a nominal 50 ps of delay. Thus, each code step provides about 0.2 ps of delay.

Default State: 0000 0000b

Bits 7:0 Must be set to 1b

Sample Clock Phase Intermediate/Coarse Adjust

Addr: Fh (1111b) **Write only (0x007F)**

D15	D14	D13	D12	D11	D10	D9	D8
POL	(MSB) Coarse Phase Adjust					IPA	

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bit 15 Polarity Select. When this bit is selected, the polarity of the ADC sampling clock is inverted.
Default State: 0b

Bits 14:10 Coarse Phase Adjust. Each code value in this field delays the sample clock by approximately 65 ps. A value of 00000b in this field causes zero adjustment.
Default State: 00000b

Bits 9:7 Intermediate Phase Adjust. Each code value in this field delays the sample clock by approximately 11 ps. A value of 000b in this field causes zero adjustment. Maximum combined adjustment using Coarse Phase Adjust and Intermediate Phase adjust is approximately 2.1ns.
Default State: 000b

Bits 6:0 Must be set to 1b

Note Regarding Extended Mode Offset Correction

When using the I- Channel or Q- Channel Offset Adjust registers, the following information should be noted.

For offset values of +0000 0000 and -0000 0000, the actual offset is not the same. By changing only the sign bit in this case, an offset step in the digital output code of about 1/10th of an LSB is experienced. This is shown more clearly in the Figure below.

Note Regarding Clock Phase Adjust

This is a feature intended to help the system designer remove small imbalances in clock distribution traces at the board level when multiple ADCs are used. Please note, however, that enabling this feature will reduce the dynamic performance (ENOB, SNR SFDR) some finite amount. The amount of degradation increases with the amount of adjustment applied. The user is strongly advised to (a) use the minimal amount of adjustment: and (b) verify the net benefit of this feature in his system before relying on it.

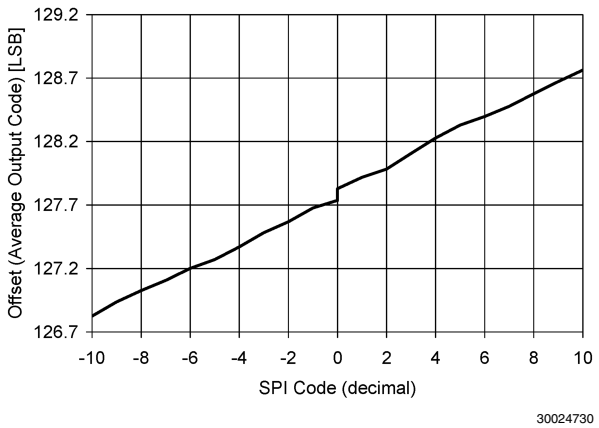


FIGURE 11. Extended Mode Offset Behavior

1.5 MULTIPLE ADC SYNCHRONIZATION

The ADC08D1520QML has the capability to precisely reset its sampling clock input to DCLK output relationship as determined by the user-supplied DCLK_RST pulse. This allows multiple ADCs in a system to have their DCLK (and data) outputs transition at the same time with respect to the shared CLK input that they all the ADCs use for sampling.

The DCLK_RST signal must observe some timing requirements that are shown in *Figure 7*, *Figure 8* and *Figure 9* of the Timing Diagrams. The DCLK_RST pulse must be of a minimum width and its deassertion edge must observe setup and hold times with respect to the CLK input rising edge. These timing specifications are listed as t_{RH}, t_{RS}, and t_{RPW} in the Converter Electrical Characteristics.

The DCLK_RST signal can be asserted asynchronous to the input clock. If DCLK_RST is asserted, the DCLK output is held in a designated state. The state in which DCLK is held during the reset period is determined by the mode of operation (SDR/DDR) and the setting of the Output Edge configuration pin or bit. (Refer to *Figure 7*, *Figure 8* and *Figure 9* for the DCLK reset state conditions). Therefore, depending upon when the DCLK_RST signal is asserted, there may be a narrow pulse on the DCLK line during this reset event. When the DCLK_RST signal is de-asserted in synchronization with the CLK rising edge, the 4th or 5th CLK falling edge synchronizes the DCLK output with those of other ADC08D1520QMLs in the system. The DCLK output is enabled again after a constant delay (relative to the input clock frequency) which is equal to the CLK input to DCLK output delay (t_{SD}). The device always exhibits this delay characteristic in normal operation.

As shown in *Figure 7*, *Figure 8* and *Figure 9*of the Timing Diagrams, there is a delay from the deassertion of DCLK_RST to the reappearance of DCLK, which is equal to several CLK cycles of delay plus t_{SD}. Note that the deassertion of DCLK_RST is not latched in until the next falling edge of CLK. For 1:2 Demux DDR 0 deg Mode, there are five CLK cycles of delay; for all other modes, there are four CLK cycles of delay.

If the device is not programmed to allow DCLK to run continuously, DCLK will become inactive during a calibration cycle. Therefore, it is strongly recommended that DCLK only be used as a data capture clock and not as a system clock.

The DCLK_RST pin should NOT be brought high while the calibration process is running (while CalRun is high). Doing so could cause a digital glitch in the digital circuitry, resulting in corruption and invalidation of the calibration. (See Application Information Section 2.4.3)

1.6 ADC TEST PATTERN

To aid in system debug, the ADC08D1520QML has the capability of providing a test pattern at the four output ports completely independent of the input signal. The ADC is disengaged and a test pattern generator is connected to the outputs including OR. The test pattern output is the same in DES Mode and Non-DES Mode. Each port is given a unique 8-bit word, alternating between 1's and 0's as described in the *Table 6*.

TABLE 6. Test Pattern by Output Port in 1:2 Demultiplex Mode

Time	Qd	Id	Q	I	OR	Comments
T0	01h	02h	03h	04h	0	Pattern Sequence n
T1	FEh	FDh	FCh	FBh	1	
T2	01h	02h	03h	04h	0	
T3	FEh	FDh	FCh	FBh	1	
T4	01h	02h	03h	04h	0	
T5	01h	02h	03h	04h	0	Pattern Sequence n+1
T6	FEh	FDh	FCh	FBh	1	
T7	01h	02h	03h	04h	0	
T8	FEh	FDh	FCh	FBh	1	
T9	01h	02h	03h	04h	0	
T10	01h	02h	03h	04h	0	Pattern Sequence n+2
T11	...	...	...	...	...	

With the part programmed into the Non-Demultiplex Mode, the test pattern's order will be as described in *Table 7*.

TABLE 7. Test Pattern by Output Port in Non-Demultiplex Mode

Time	Q	I	OR	Comments
T0	01h	02h	0	Pattern Sequence n
T1	FEh	FDh	1	
T2	01h	02h	0	
T3	01h	02h	0	
T4	FEh	FDh	1	
T5	FEh	FDh	1	
T6	01h	02h	0	
T7	01h	02h	0	
T8	FEh	FDh	1	
T9	01h	02h	0	
T10	01h	02h	0	Pattern Sequence n+1
T11	FEh	FDh	1	
T12	01h	02h	0	
T13	01h	02h	0	
T14	FEh	FDh	1	
T15	...	...	...	

To ensure that the test pattern starts synchronously in each port, set DCLK_RST while writing the Test Pattern Output bit in the Extended Configuration Register. The pattern appears at the data output ports when DCLK_RST is cleared low. The test pattern will work at speed and will work with the device in the SDR, DDR and the Non-Demultiplex output modes.

2.0 Applications Information

2.1 APPLICATIONS IN RADIATION ENVIRONMENTS

Applying the ADC08D1520QML in a radiation environment should be done with careful consideration to that environment. The QMLV version of this part has been rated to tolerate a high total dose of ionizing radiation by test method 1019 of MIL-STD-883. The part is also immune to SEE (Single Event Effects) hard errors such as Single Event Latch-up and Functional Interrupts. However, there are still some recommendations and cautions.

Floating pins. There are four tri-level pins which activate the following modes when left floating: FSR/DCLK_RST-, OutEdge/DDR/SDATA, DRST_SEL and DES/$\overline{SCS}$. If modes requiring a floating pin are needed to be used, then it is strongly recommended that the floating method of establishing Va/2 on these pins not be employed. Due to the potential of increased leakage of the input protection diodes after large ionizing doses, the midpoint voltage (Va/2 or 0.95V) should be voltage forced or formed with a resistor divider from the analog supply to ground with two 2K ohm resistors. The tolerance for this mid point voltage is 650mV ≥ $V_A/2$ ≤ 1.2V. The internal voltage divider resistors provide too little current to set the midpoint voltage reliably in radiation environments.

2.2 THE REFERENCE VOLTAGE

The voltage reference for the ADC08D1520QML is derived from a 1.254V bandgap reference, a buffered version of which is made available at pin 31, V_{BG}, for user convenience. This output has an output current capability of ±100 µA and should be buffered if more current is required.

The internal bandgap-derived reference voltage has a nominal value V_{IN}, as determined by the FSR pin and described in *1.1.4 The Analog Inputs*.

There is no provision for the use of an external reference voltage, but the full-scale input voltage can be adjusted through a Full Scale Register in the Extended Control Mode, as explained in *1.2 NON-EXTENDED CONTROL/EXTENDED CONTROL*.

Differential input signals up to the chosen full-scale level will be digitized to 8 bits. Signal excursions beyond the full-scale range will be clipped at the output. These large signal excursions will also activate the OR output for the time that the signal is out of range. See *2.3.2 Out Of Range (OR) Indication*.

One extra feature of the V_{BG} pin is that it can be used to raise the common mode voltage level of the LVDS outputs. The output offset voltage (V_{OS}) is typically 800 mV when the V_{BG} pin is used as an output or left unconnected. To raise the LVDS offset voltage to a typical value of 1100 mV the V_{BG} pin can be connected directly to the supply rails.

2.3 THE ANALOG INPUT

The analog input is a differential one to which the signal source must be a.c. coupled as shown in *Figure 12*. In the Non-Extended Control Mode, the full-scale input range is selected with the FSR pin as specified in the Converter Electrical Characteristics. In the Extended Control Mode, the full-scale input range is selected by programming the Full-Scale Voltage Adjust register through the Serial Interface. For best performance, when adjusting the input full-scale range in the Extended Control, refer to *1.4 REGISTER DESCRIPTION* for guidelines on limiting the amount of adjustment.

Table 8 gives the input to output relationship with the FSR pin high when the normal (Non-Extended) Mode is used. With the FSR pin grounded, the millivolt values in *Table 8* are reduced to 75% of the values indicated. In the Extended Control Mode, these values will be determined by the full scale range and offset settings in the Control Registers.

TABLE 8. Differential Input To Output Relationship (Non-Extended Control Mode, FSR High)

V_{IN}+	V_{IN}–	Output Code
V_{CM} – 225 mV	V_{CM} + 225 mV	0000 0000
V_{CM} – 113 mV	V_{CM} + 113 mV	0100 0000
V_{CM}	V_{CM}	0111 1111 / 1000 0000
V_{CM} + 109 mV	V_{CM} –109 mV	1100 0000
V_{CM} + 217.5 mV	V_{CM} – 217.5 mV	1111 1111

The buffered analog inputs simplify the task of driving these inputs and the RC pole that is generally used at sampling ADC inputs is not required. If it is desired to use an amplifier circuit before the ADC, use care in choosing an amplifier with adequate noise and distortion performance and adequate gain at the frequencies used for the application.

IMPORTANT NOTE: An Analog input channel that is not used (e.g. in DES Mode) should be left floating when the inputs are a.c. coupled. Do not connect an unused analog input to ground.

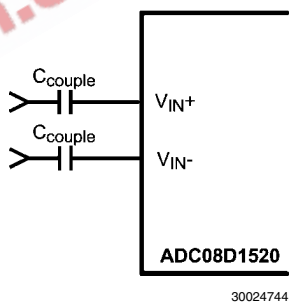


FIGURE 12. Differential Input Drive

2.3.1 Handling Single-Ended Input Signals

There is no provision for the ADC08D1520QML to adequately process single-ended input signals. The best way to handle single-ended signals is to convert them to differential signals before presenting them to the ADC. The easiest way to accomplish single-ended to differential signal conversion is with an appropriate balun-connected transformer, as shown in *Figure 13*.

2.3.1.1. a.c. Coupled Input

The easiest way to accomplish single-ended a.c. Input to differential a.c. signal is with an appropriate balun, as shown in *Figure 13*.

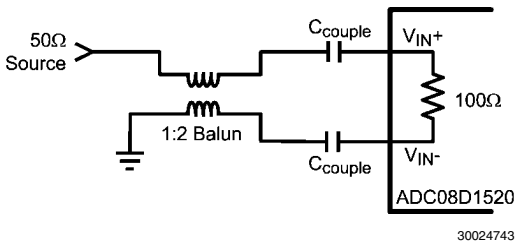


FIGURE 13. Single-Ended to Differential Signal Conversion using a Balun

Figure 13 is a generic depiction of a single-ended to differential signal conversion using a balun. The circuitry specific to the balun will depend upon the type of balun selected and the overall board layout. It is recommended that the system designer contact the manufacturer of the balun they have selected to aid in designing the best performing single-ended to differential conversion circuit using that particular balun.

When selecting a balun, it is important to understand the input architecture of the ADC. There are specific balun parameters of which the system designer should be mindful. A designer should match the impedance of the analog source to the ADC08D1520QML's on-chip 100Ω differential input termination resistor. The range of this input termination resistor is described in the Converter Electrical Characteristics as the specification R_{IN}.

Also, the phase and amplitude balance are important. The lowest possible phase and amplitude imbalance is desired when selecting a balun. The phase imbalance should be no more than ±2.5° and the amplitude imbalance should be limited to less than 1dB at the desired input frequency range.

Finally, when selecting a balun, the VSWR (Voltage Standing Wave Ratio), bandwidth and insertion loss of the balun should also be considered. The VSWR aids in determining the overall transmission line termination capability of the balun when interfacing to the ADC input. The insertion loss should be considered so that the signal at the balun output is within the specified input range of the ADC as described in the Converter Electrical Characteristics as the specification V_{IN}.

2.3.2 Out Of Range (OR) Indication

When the conversion result is clipped the Out of Range output is activated such that OR+ goes high and OR- goes low. This output is active as long as accurate data on either or both of the buses would be outside the range of 00h to FFh. Note that when the device is programmed to provide a second DCLK output, the OR signals become DCLK2. Refer to *1.4 REGISTER DESCRIPTION*.

2.3.3 Full-Scale Input Range

As with all A/D Converters, the input range is determined by the value of the ADC's reference voltage. The reference voltage of the ADC08D1520QML is derived from an internal band-gap reference. The FSR pin controls the effective reference voltage of the ADC08D1520QML such that the differential full-scale input range at the analog inputs is a normal amplitude with the FSR pin high, or a reduced amplitude with FSR pin low as defined by the specification V_{IN} in the Converter Electrical Characteristics. Best SNR is obtained with FSR high.

2.4 THE CLOCK INPUTS

The ADC08D1520QML has differential LVDS clock inputs, CLK+ and CLK-, which must be driven with an a.c. coupled, differential clock signal. Although the ADC08D1520QML is tested and its performance is guaranteed with a differential 1.5 GHz clock, it typically will function well with input clock frequencies indicated in the Converter Electrical Characteristics. The clock inputs are internally terminated and biased. The input clock signal must be capacitive coupled to the clock pins as indicated in *Figure 14*.

Operation up to the sample rates indicated in the Converter Electrical Characteristics is typically possible if the maximum ambient temperatures indicated are not exceeded. Operating at higher sample rates than indicated for the given ambient temperature may result in reduced device reliability and product lifetime. This is because of the higher power consumption and die temperatures at high sample rates. Important also for reliability is proper thermal management. See *2.7.2 Thermal Management*.

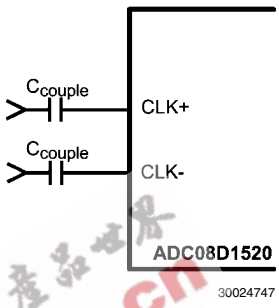


FIGURE 14. Differential (LVDS) Input Clock Connection

The differential input clock line pair should have a characteristic impedance of 100Ω and (when using a balun), be terminated at the clock source in that (100 Ω) characteristic impedance. The input clock line should be as short and as direct as possible. The ADC08D1520QML clock input is internally terminated with an untrimmed 100Ω resistor.

Insufficient input clock levels will result in poor dynamic performance. Excessively high input clock levels could cause a change in the analog input offset voltage. To avoid these problems, keep the input clock level within the range specified in the Converter Electrical Characteristics.

The low and high times of the input clock signal can affect the performance of any A/D Converter. The ADC08D1520QML features a duty cycle clock correction circuit which can maintain performance over temperature even in DES Mode. **The ADC will meet its performance specification if the input clock high and low times are maintained within the range (20/80% ratio).**

High speed, high performance ADCs such as the ADC08D1520QML require a very stable input clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{IN(P-P)}/V_{INFSR}) \times (1/(2^{(N+1)} \times \pi \times f_{IN}))$$

where $t_{J(MAX)}$ is the rms total of all jitter sources in seconds, $V_{IN(P-P)}$ is the peak-to-peak analog input signal, V_{INFSR} is the full-scale range of the ADC, "N" is the ADC resolution in bits and f_{IN} is the maximum input frequency, in Hertz, at the ADC analog input.

Note that the maximum jitter described above is the RSS sum of the jitter from all sources, including that in the ADC input clock, that added by the system to the ADC input clock and

input signals and that added by the ADC itself. Since the effective jitter added by the ADC is beyond user control, the best the user can do is to keep the sum of the externally added input clock jitter and the jitter added by the analog circuitry to the analog signal to a minimum.

Input clock amplitudes above those specified in the Converter Electrical Characteristics may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 127/128 when both input pins are at the same potential.

2.5 CONTROL PINS

Six control pins (without the use of the serial interface) provide a wide range of possibilities in the operation of the ADC08D1520QML and facilitate its use. These control pins provide Full-Scale Input Range setting, Self Calibration, Output Edge Synchronization choice, LVDS Output Level choice and a Power Down feature.

2.5.1 Full-Scale Input Range Setting

The input full-scale range can be selected with the FSR control input (pin 14) in the Normal Mode of operation. The input full-scale range is specified as V_{IN} in the Converter Electrical Characteristics. In the Extended Control Mode, the input full-scale range may be programmed using the Full-Scale Adjust Voltage register. See *2.3 THE ANALOG INPUT* for more information.

2.5.2 Calibration

The ADC08D1520QML calibration must be run to achieve specified performance. The calibration must be initiated by the user. The calibration procedure is exactly the same whether there is an input clock present upon power up or if the clock begins some time after application of power. The CalRun output indicator is high while a calibration is in progress. Note that the DCLK outputs are not active during a calibration cycle by default, therefore it is not recommended for use as a system clock. The DCLK outputs are continuously present at the output only when the Resistor Trim Disable is activated.

2.5.2.1 Initiating Calibration

A calibration may be run at any time in both the Non-DES and DES Modes. After power-up, we recommend that the part be calibrated with the Resistor Trim Disable inactive once the power supplies have stabilized and the temperature of the chip has stabilized. When a calibration is run with the Resistor Trim Disable inactive, both the ADC and the input termination resistor are calibrated. However, since the input termination resistance changes only marginally with temperature, the user has the option to disable the input termination resistor calibration for subsequent calibrations, which will guarantee that the DCLK is continuously present at the output. The Resistor Trim Disable can be programmed in the Extended Configuration register (Addr: 9h) when in the Extended Control Mode. Refer to *Extended Configuration Register* for register programming information.

As dynamic performance changes slightly with junction temperature, a calibration may be executed to bring the performance of the ADC in line. Two methods can be used initiate a calibration. The first method is to hold the CAL pin low for at least t_{CAL_L} input clock cycles, then hold it high for at least another t_{CAL_H} input clock cycles. The second method is to program the CAL bit in the Calibration register while in Extended Control Mode. The functionality of the CAL bit is exactly the same as using the CAL pin. The CAL bit must be programmed to 0b for a minimum of t_{CAL_L}input clock cycles and then programmed to 1b for a minimum of t_{CAL_H} input clock cycles to initiate a calibration cycle. The CalRun signal should be monitored to determine when the calibration cycle has completed. The CalRun pin will become a logic high indicating an active calibration cycle regardless of which method was used to initiate the calibration cycle. Note that the DCLK outputs are not active during a calibration cycle; therefore, it is not recommended for use as a system clock.

The minimum number of t_{CAL_L} and t_{CAL_H} input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. As mentioned in *1.1 OVERVIEW*, for best performance, a calibration should be performed 20 seconds or more after power up and repeated when the operating temperature changes significantly relative to the specific system design performance requirements. Dynamic performance changes slightly with increasing junction temperature and can be easily corrected by performing a calibration.

2.5.3 Output Edge Synchronization

DCLK signals are available to help latch the converter output data into external circuitry. The output data can be synchronized with either edge of these DCLK signals. That is, the output data transition can be set to occur with either the rising edge or the falling edge of the DCLK signal, so that either edge of that DCLK signal can be used to latch the output data into the receiving circuit.

When OutEdge (pin 4) is high, the output data is synchronized with (changes with) the rising edge of the DCLK+ (pin 82). When OutEdge is low, the output data is synchronized with the falling edge of DCLK+.

At the very high speeds of which the ADC08D1520QML is capable, slight differences in the lengths of the DCLK and data lines can mean the difference between successful and erroneous data capture. The OutEdge pin is used to capture data on the DCLK edge that best suits the application circuit and layout.

2.5.4 LVDS Output Level Control

The output level can be set to one of two levels with OutV (pin3). The strength of the output drivers is greater with OutV high. With OutV low there is less power consumption in the output drivers, but the lower output level means decreased noise immunity.

For short LVDS lines and low noise systems, satisfactory performance may be realized with the OutV input low. If the LVDS lines are long and/or the system in which the ADC08D1520QML is used is noisy, it may be necessary to tie the OutV pin high.

2.5.5 Dual Edge Sampling

The Dual Edge Sampling (DES) feature causes one of the two input pairs to be routed to both ADCs. The other input pair is deactivated. One of the ADCs samples the input signal on the rising input clock edge (duty cycle corrected), the other samples the input signal on the falling input clock edge (duty cycle corrected). If the device is in the 1:4 Demux DES Mode, the result is an output data rate 1/4 that of the interleaved sample rate which is twice the input clock frequency. Data is presented in parallel on all four output buses in the following order: DQd, DId, DQ, DI. If the device is the Non-Demultiplex output mode, the result is an output data rate 1/2 that of the interleaved sample rate. Data is presented in parallel on two output buses in the following order: DQ, DI.

To use this feature in the Non-Extended Control Mode, tie pin 127 to $V_A/2$ and the signal at the I- channel input will be sampled by both converters.

In the Extended Control Mode, either input may be used for dual edge sampling. See *1.1.5.1 Dual-Edge Sampling*.

2.5.6 Power Down Feature

The Power Down pins (PD and PDQ) allow the ADC08D1520QML to be entirely powered down (PD) or the Q-Channel channel to be powered down and the I- Channel to remain active. See *1.1.7 Power Down* for details on the power down feature.

The digital data (+/-) output pins are put into a high impedance state when the PD pin for the respective channel is high. Upon return to normal operation, the pipeline will contain meaningless information and must be flushed.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is simultaneously ramped, the device will not calibrate until the PD input goes low. When PD is high and a calibration is initiated, the request for calibration is completely ignored. Refer to *1.1.7 Power Down*

2.6 THE DIGITAL OUTPUTS

The ADC08D1520QML demultiplexes the output data of each of the two ADCs on the die onto two LVDS output buses (total of four buses, two for each ADC). For each of the two converters, the results of successive conversions started on the odd falling edges of the CLK+ pin are available on one of the two LVDS buses, while the results of conversions started on the even falling edges of the CLK+ pin are available on the other LVDS bus. This means that, the word rate at each LVDS bus is 1/2 the ADC08D1520QML input clock rate and the two buses must be multiplexed to obtain the entire 1.5 GSPS conversion result.

Since the minimum recommended input clock rate for this device is 200 MSPS (Non DES Mode), the effective rate can be reduced to as low as 100 MSPS by using the results available on just one of the two LVDS buses and a 200 MHz input clock, decimating the 200 MSPS data by two.

There is one LVDS output clock pair (DCLK+/-) available for use to latch the LVDS outputs on all buses. Whether the data is sent at the rising or falling edge of DCLK is determined by the sense of the OutEdge pin, as described in *2.5.3 Output Edge Synchronization*.

DDR (Double Data Rate) clocking can also be used. In this mode a word of data is presented with each edge of DCLK, reducing the DCLK frequency to 1/4 the input clock frequency. See the Timing Diagram section for details.

The OutV pin is used to set the LVDS differential output levels. See *2.5.4 LVDS Output Level Control*.

The output format is Offset Binary. Accordingly, a full-scale input level with V_{IN}+ positive with respect to V_{IN}– will produce an output code of all ones, a full-scale input level with V_{IN}– positive with respect to V_{IN}+ will produce an output code of all zeros and when V_{IN}+ and V_{IN}– are equal, the output code will vary between codes 127 and 128.

2.7 POWER CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 33 µF capacitor should be placed within an inch (2.5 cm) of the A/D converter power pins. A 0.1 µF capacitor should be placed as close as possible to each V_A pin, preferably within one-half centimeter. Leadless chip capacitors are preferred because they have low lead inductance.

The V_A and V_{DR} supply pins should be isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A ferrite choke, such as the JW Miller FB20009-3B, is recommended between these supply lines when a common source is used for them.

As is the case with all high speed converters, the ADC08D1520QML should be assumed to have little power supply noise rejection. Any power supply used for digital circuitry in a system where a lot of digital power is being consumed should not be used to supply power to the ADC08D1520QML. The ADC supplies should be the same supply used for other analog circuitry, if not a dedicated supply.

2.7.1 Supply Voltage

The ADC08D1520QML is specified to operate with a supply voltage of 1.9V ±0.1V. It is very important to note that, while this device will function with slightly higher supply voltages, these higher supply voltages may reduce product lifetime.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 150 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC08D1520QML power pins.

The Absolute Maximum Ratings should be strictly observed, even during power up and power down. A power supply that produces a voltage spike at turn-on and/or turn-off of power can destroy the ADC08D1520QML. The circuit of *Figure 15* will provide supply overshoot protection.

Many linear regulators will produce output spiking at power-on unless there is a minimum load provided. Active devices draw very little current until their supply voltages reach a few hundred millivolts. The result can be a turn-on spike that can destroy the ADC08D1520QML, unless a minimum load is provided for the supply. The 100Ω resistor at the regulator output provides a minimum output current during power-up to ensure there is no turn-on spiking.

In the circuit of *Figure 15*, an LM317 linear regulator is satisfactory if its input supply voltage is 4V to 5V . If a 3.3V supply is used, an LM1086 linear regulator is recommended.

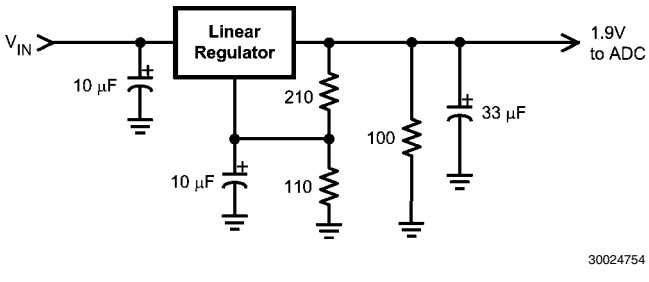


FIGURE 15. Non-Spiking Power Supply

The output drivers should have a supply voltage, V_{DR}, that is within the range specified in the Operating Ratings table. This voltage should not exceed the V_A supply voltage.

If the power is applied to the device without an input clock signal present, the current drawn by the device might be below 200 mA. This is because the ADC08D1520QML gets reset through clocked logic and its initial state is unknown. If the reset logic comes up in the "on" state, it will cause most of the analog circuitry to be powered down, resulting in less

than 100 mA of current draw. This current is greater than the power down current because not all of the ADC is powered down. The device current will be normal after the input clock is established.

2.7.2 Thermal Management

The ADC08D1520QML is capable of impressive speeds and performance at very low power levels for its speed. However, the power consumption is still high enough to require attention to thermal management. For reliability reasons, the die temperature should be kept to a maximum of 150°C. That is, T_A (ambient temperature) plus ADC power consumption times θ_{JA} (junction to ambient thermal resistance) should not exceed 150°C.

Please note that the following are recommendations for mounting this device onto a PCB. This should be considered the starting point in PCB and assembly process development. It is recommended that the process be developed based upon past experience in package mounting.

The bottom of the package of the ADC08D1520QML provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. The land pattern design for lead attachment to the PCB should be the same as for a conventional LQFP, but the bottom of the package must be attached to the board to remove the maximum amount of heat from the package, as well as to ensure best product parametric performance.

To maximize the removal of heat from the package, a thermal land pattern must be incorporated on the PC board within the footprint of the package. The bottom of the device must be soldered down to ensure adequate heat conduction out of the package. The land pattern for this exposed pad should be as large as the 600 x 600 mil bottom of the package and be located such that the bottom of the device is entirely over that thermal land pattern. This thermal land pattern should be electrically connected to ground.

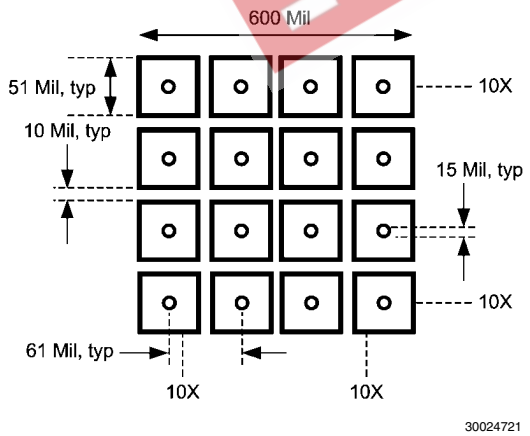


FIGURE 16. Recommended Package Land Pattern

Since a large aperture opening may result in poor release, the aperture opening should be subdivided into an array of smaller openings, similar to the land pattern of *Figure 16*.

To minimize junction temperature, it is recommended that a simple heat sink be built into the PCB. This is done by including a copper area of about 2.25 square inches (14.52 square cm) on the opposite side of the PCB. This copper area may be plated or solder coated to prevent corrosion, but should not have a conformal coating, which could provide some thermal insulation. Thermal vias should be used to connect these top and bottom copper areas. These thermal vias act as "heat pipes" to carry the thermal energy from the device side of the board to the opposite side of the board where it can be more effectively dissipated. The use of approximately 100 thermal vias is recommended. Use of a higher weight copper on the internal ground plane is recommended, (i.e. 2_{OZ} instead of 1_{OZ}, for thermal considerations only.

The thermal vias should be placed on a 61mil grid spacing and have a diameter of 15 mil typically. These vias should be barrel plated to avoid solder wicking into the vias during the soldering process as this wicking could cause voids in the solder between the package exposed pad and the thermal land on the PCB. Such voids could increase the thermal resistance between the device and the thermal land on the board, which would cause the device to run hotter.

If it is desired to monitor die temperature, a temperature sensor may be mounted on the heat sink area of the board near the thermal vias. Allow for a thermal gradient between the temperature sensor and the ADC08D1520QML die of $\theta_{J\text{-}PAD}$ times typical power consumption.

2.8 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A single ground plane should be used, instead of splitting the ground plane into analog and digital areas.

Since digital switching transients are composed largely of high frequency components, the skin effect tells us that total ground plane copper weight will have little effect upon the logic-generated noise. Total surface area is more important than is total ground plane volume. Coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High power digital components should not be located on or near any linear component or power supply trace or plane that services analog or mixed signal components as the resulting common return current path could cause fluctuation in the analog input “ground” return of the ADC, causing excessive noise in the conversion result.

Generally, we assume that analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. The input clock lines should be isolated from ALL other lines, analog AND digital. The generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. This is especially important with the low level drive required of the ADC08D1520QML. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane. All analog circuitry (input amplifiers, filters, etc.) should be separated from any digital components.

2.9 DYNAMIC PERFORMANCE

The ADC08D1520QML is a.c. tested and its dynamic performance is guaranteed. To meet the published specifications and avoid jitter-induced noise, the clock source driving the CLK input must exhibit low rms jitter. The allowable jitter is a function of the input frequency and the input signal level, as described in *2.4 THE CLOCK INPUTS*.

It is good practice to keep the ADC input clock line as short as possible, to keep it well away from any other signals and to treat it as a transmission line. Other signals can introduce jitter into the input clock signal. The clock signal can also introduce noise into the analog path if not isolated from that path.

Best dynamic performance is obtained when the exposed pad at the back of the package has a good connection to ground. This is because this path from the die to ground is a lower impedance than offered by the package pins.

2.10 USING THE SERIAL INTERFACE

The ADC08D1520QML may be operated in the Non-Extended Control (non-Serial Interface) Mode or in the extended control mode. *Table 9* and *Table 10* describe the functions of pins 3, 4, 14 and 127 in the Non-Extended Control Mode and the Extended Control Mode, respectively.

2.10.1 Non-Extended Control Mode Operation

Non-extended Control Mode operation means that the Serial Interface is not active and all controllable functions are controlled with various pin settings. Pin 41 is the primary control of the extended control enable function. When pin 41 is logic high, the device is in the Non-Extended Control Mode. If pin 41 is tied to $V_A/2$ and pin 52 connected to $V_A/2$ or logic high, the extended control enable function is controlled by pin 14. The device has functions which are pin programmable when in the Non-Extended Control Mode. An example is the full-scale range is controlled in the Non-Extended Control Mode by setting pin 14 high or low. *Table 9* indicates the pin functions of the ADC08D1520QML in the Non-Extended Control Mode.

TABLE 9. Non-Extended Control Mode Operation (Pin 41 $V_A/2$ and Pin 52 $V_A/2$ or Logic High)

Pin	Low	High	$V_A/2$
3	Reduced V_{OD}	Normal V_{OD}	n/a
4	OutEdge = Neg	OutEdge = Pos	DDR
127	N/A	N/A	DES
14	Reduced V_{IN}	Normal V_{IN}	Extended Control Mode

Pin 3 can be either high or low in the Non-Extended Control Mode. See *1.2 NON-EXTENDED CONTROL/EXTENDED CONTROL* for more information.

Pin 4 can be high or low in the Non-Extended Control Mode. In the Non-Extended Control Mode, pin 4 high or low defines the edge at which the output data transitions. See *2.5.3 Output Edge Synchronization* for more information. If this pin is tied to $V_A/2$, the output clock (DCLK) is a DDR (Double Data Rate) clock (see *1.1.5.3 Double Data Rate*) and the output edge synchronization is irrelevant since data is clocked out on both DCLK edges.

When in Normal Mode, Pin 127 must be tied high. If pin 127 is tied to $V_A/2$, the converter performs dual edge sampling (DES).

TABLE 10. Extended Control Mode Operation (Pin 41 Logic Low and Pin 52 $V_A/2$ or Logic High)

Pin	Function
3	SCLK (Serial Clock)
4	SDATA (Serial Data)
127	$\overline{SCS}$ (Serial Interface Chip Select)

2.11 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For device reliability, no input should go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits on even a transient basis may not only cause faulty or erratic operation, but may impair device reliability. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground. Controlling the impedance of high speed lines and terminating these lines in their characteristic impedance should control overshoot.

Care should be taken not to overdrive the inputs of the ADC08D1520QML. Such practice may lead to conversion inaccuracies and even to device damage.

Driving the V_{BG} pin to change the reference voltage. As mentioned in *2.2 THE REFERENCE VOLTAGE*, the reference voltage is intended to be fixed to provide one of two different full-scale values (650 mV_{P-P} and 870 mV_{P-P}). Over driving this pin will not change the full scale value, but can be used to change the LVDS common mode voltage from 0.8V to 1.2V by tying the V_{BG} pin to V_A.

Driving the clock input with an excessively high level signal. The ADC input clock level should not exceed the level described in the Operating Ratings Table or the input offset could change.

Inadequate input clock levels. As described in *2.4 THE CLOCK INPUTS*, insufficient input clock levels can result in poor performance. Excessive input clock levels could result in the introduction of an input offset.

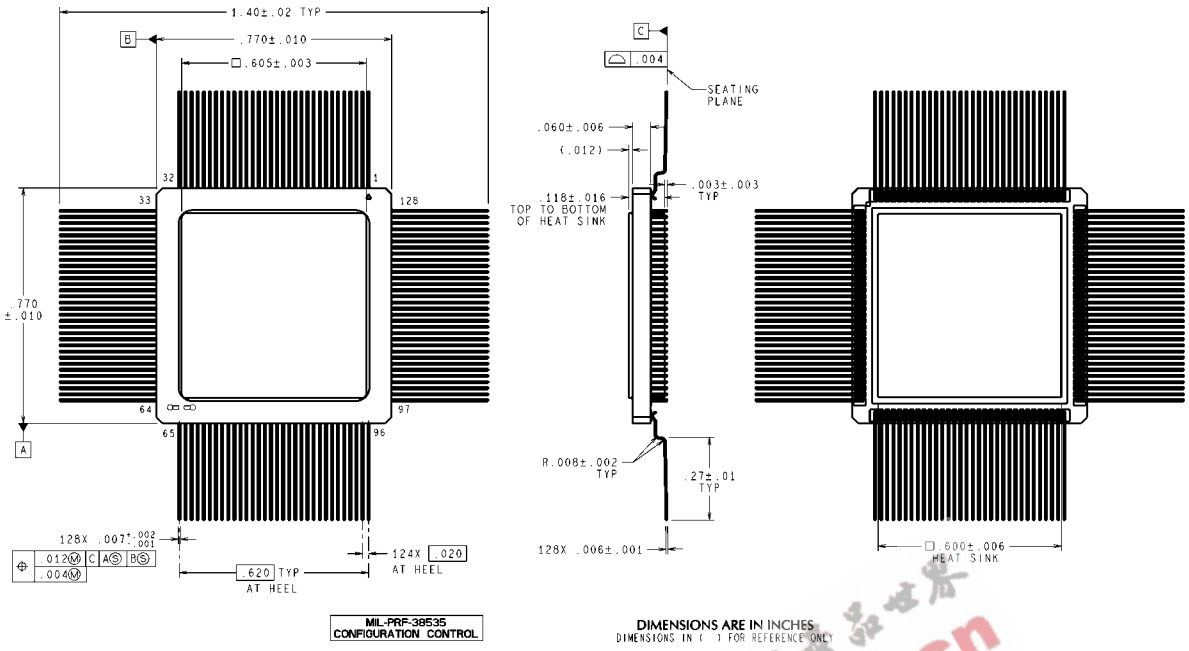
Using a clock source with excessive jitter, using an excessively long input clock signal trace, or having other signals coupled to the input clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

Failure to provide adequate heat removal. As described in *2.7.2 Thermal Management*, it is important to provide adequate heat removal to ensure device reliability. This can be done either with adequate air flow or the use of a simple heat sink built into the board. The backside pad should be grounded for best performance.

Revision History

Date Released	Revision	Section	Originator	Changes
01/09/08	A	Initial Release, New Product	R. Eddy/R. Rennie	New Product Data Sheet, Released at Edit 16
03/05/08	B	Whole data sheet	R. Rennie	Edit clarification Updates, Revision A will be Archived.

Physical Dimensions inches (millimeters) unless otherwise noted



EM128A (Rev B)

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE JEDEC REGISTRATION MS-026, VARIATION BFB.

128-Lead Ceramic Quad
(Gold Lead Finish)
NS Package Number EL128A

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
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LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

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National Semiconductor Americas Technical Support Center
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Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
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National Semiconductor Asia Pacific Technical Support Center
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