Am4IPDS3224D

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **26085** Revision **A** Amendment **+1** Issue Date **May 13, 2003**

PRELIMINARY

AMD

Am41PDS3224D

Stacked Multi-Chip Package (MCP) Flash Memory and SRAM

Am29PDS322D 32 Megabit (2 M x 16-Bit) CMOS 1.8 Volt-only, Simultaneous Operation, Page Mode Flash Memory and 4 Mbit (512 K x 8-Bit/256 K x 16-Bit) Static RAM

DISTINCTIVE CHARACTERISTICS

MCP Features

- **Power supply voltage of 1.8 to 2.2 volt**
- **High performance**
  - Access time as fast as 100 ns flash, 70 ns SRAM
- **Package**
  - 73-Ball FBGA
- **Operating Temperature**
  - –40°C to +85°C

Flash Memory Features

ARCHITECTURAL ADVANTAGES

- **Simultaneous Read/Write operations**
  - Data can be continuously read from one bank while executing erase/program functions in other bank.
  - Zero latency between read and write operations
- **Page Mode Operation**
  - 4 word page allows fast asynchronous reads
- **Dual Bank architecture**
  - One 4 Mbit bank and one 28 Mbit bank
- **SecSi (Secured Silicon) Sector: Extra 64 KByte sector**
  - *Factory locked and identifiable:* 16 byte Electronic Serial Number available for factory secure, random ID; verifiable as factory locked through autoselect function. ExpressFlash option allows entire sector to be available for factory-secured data
  - *Customer lockable:* Can be read, programmed, or erased just like other sectors. Once locked, data cannot be changed
- **Zero Power Operation**
  - Sophisticated power management circuits reduce power consumed during inactive periods to nearly zero.
- **Top or bottom boot block**
- **Manufactured on 0.23 µm process technology**
- **Compatible with JEDEC standards**
  - Pinout and software compatible with single-power-supply flash standard

PERFORMANCE CHARACTERISTICS

- **High performance**
  - Random access time of 100 ns at 1.8 V to 2.2 V V_{CC}
- **Ultra low power consumption (typical values)**
  - 2.5 mA active read current at 1 MHz for initial page read
  - 24 mA active read current at 10 MHz for initial page read
  - 0.5 mA active read current at 10 MHz for intra-page read
  - 1 mA active read current at 20 MHz for intra-page read
  - 200 nA in standby or automatic sleep mode
- **Minimum 1 million write cycles guaranteed per sector**
- **20 year data retention at 125°C**
  - Reliable operation for the life of the system

SOFTWARE FEATURES

- **Data Management Software (DMS)**
  - AMD-supplied software manages data programming, enabling EEPROM emulation
  - Eases historical sector erase flash limitations
- **Erase Suspend/Erase Resume**
- **Data# Polling and Toggle Bits**
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

HARDWARE FEATURES

- **Any combination of sectors can be erased**
- **Ready/Busy# output (RY/BY#)**
- **Hardware reset pin (RESET#)**
- **WP#/ACC input pin**
  - Write protect (WP#) function allows protection of two outermost boot sectors, regardless of sector protect status
  - Acceleration (ACC) function accelerates program timing
- **Sector protection**
  - Hardware method of locking a sector, either in-system or using programming equipment, to prevent any program or erase operation within that sector
  - Temporary Sector Unprotect allows changing data in protected sectors in-system

SRAM Features

- **Power dissipation**
  - Operating: 2 mA typical
  - Standby: 0.5 µA typical
- **CE1s# and CE2s Chip Select**
- **Power down features using CE1s# and CE2s**
- **Data retention supply voltage: 1.0 to 2.2 volt**
- **Byte data control: LB#s (DQ7–DQ0), UB#s (DQ15–DQ8)**

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GENERAL DESCRIPTION

The Am29PDS322D is a 32 Mbit, 1.8 V-only Flash memory organized as 2,097,152 words of 16 bits each. The device is designed to be programmed in system with standard system 1.8 V V_{CC} supply. This device can also be reprogrammed in standard EPROM programmers.

The Am29PDS322D offers fast page access time of 40 ns with random access time of 100 ns (at 1.8 V to 2.2 V V_{CC}), allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable (CE), write enable (WE), and output enable (OE) controls. The page size is 4 words.

The device requires only a **single 1.8 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into two banks. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The device is divided as shown in the following table:

Bank 1 Sectors		Bank 2 Sectors	
Quantity	**Size**	**Quantity**	**Size**
8	4 Kwords	56	32 Kwords
7	32 Kwords		
4 Mbits total		28 Mbits total	

Am29PDS322D Features

The **SecSi (Secured Silicon) Sector** is an extra 64 KByte sector capable of being permanently locked by AMD or customers. The **SecSi Indicator Bit** (DQ7) is permanently set to a 1 if the part is **factory locked**, and set to a 0 if **customer lockable**. This way, customer lockable parts can never be used to replace a factory locked part.

Factory locked parts provide several options. The SecSi Sector may store a secure, random 16 byte ESN (Electronic Serial Number), customer code (programmed through AMD's ExpressFlash service), or both. Customer Lockable parts may utilize the SecSi Sector as bonus space, reading and writing like any other flash sector, or may permanently lock their own code there.

DMS (Data Management Software) allows systems to easily take advantage of the advanced architecture of the simultaneous read/write product line by allowing removal of EEPROM devices. DMS will also allow the system software to be simplified, as it will perform all functions necessary to modify data in file structures, as opposed to single-byte modifications. To write or update a particular piece of data (a phone number or configuration data, for example), the user only needs to state which piece of data is to be updated, and where the updated data is located in the system. This is an advantage compared to systems where user-written software must keep track of the old data location, status, logical to physical translation of the data onto the Flash memory device (or memory devices), and more. Using DMS, user-written software does not need to interface with the Flash memory directly. Instead, the user's software accesses the Flash memory by calling one of only six functions. AMD provides this software to simplify system design and software integration efforts.

The device offers complete compatibility with the **JEDEC single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device **status bits:** RY/BY# pin, DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to the read mode.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

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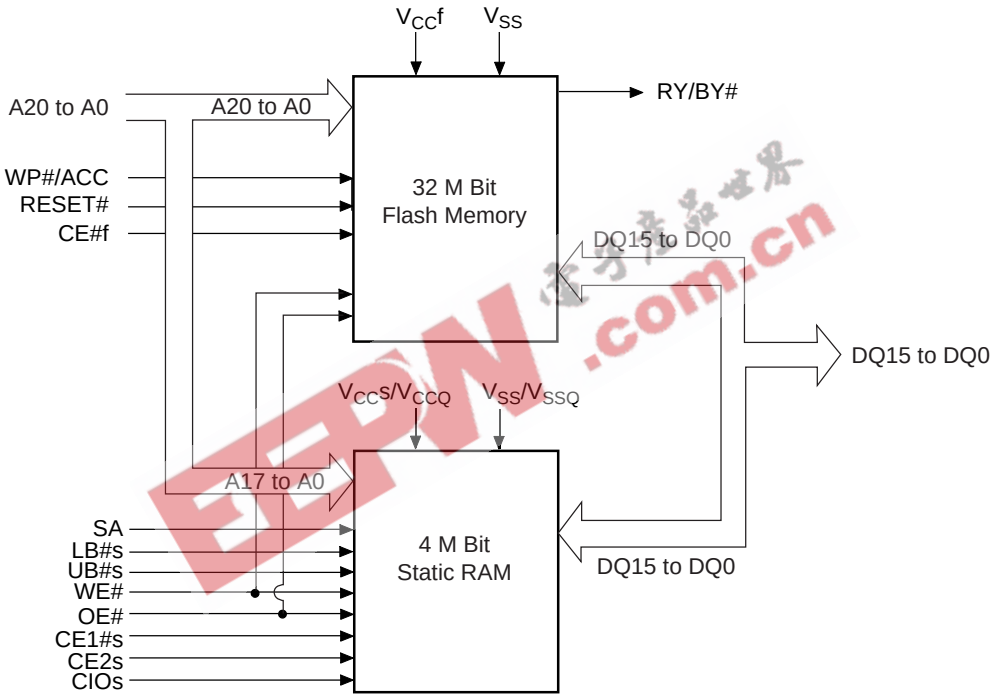
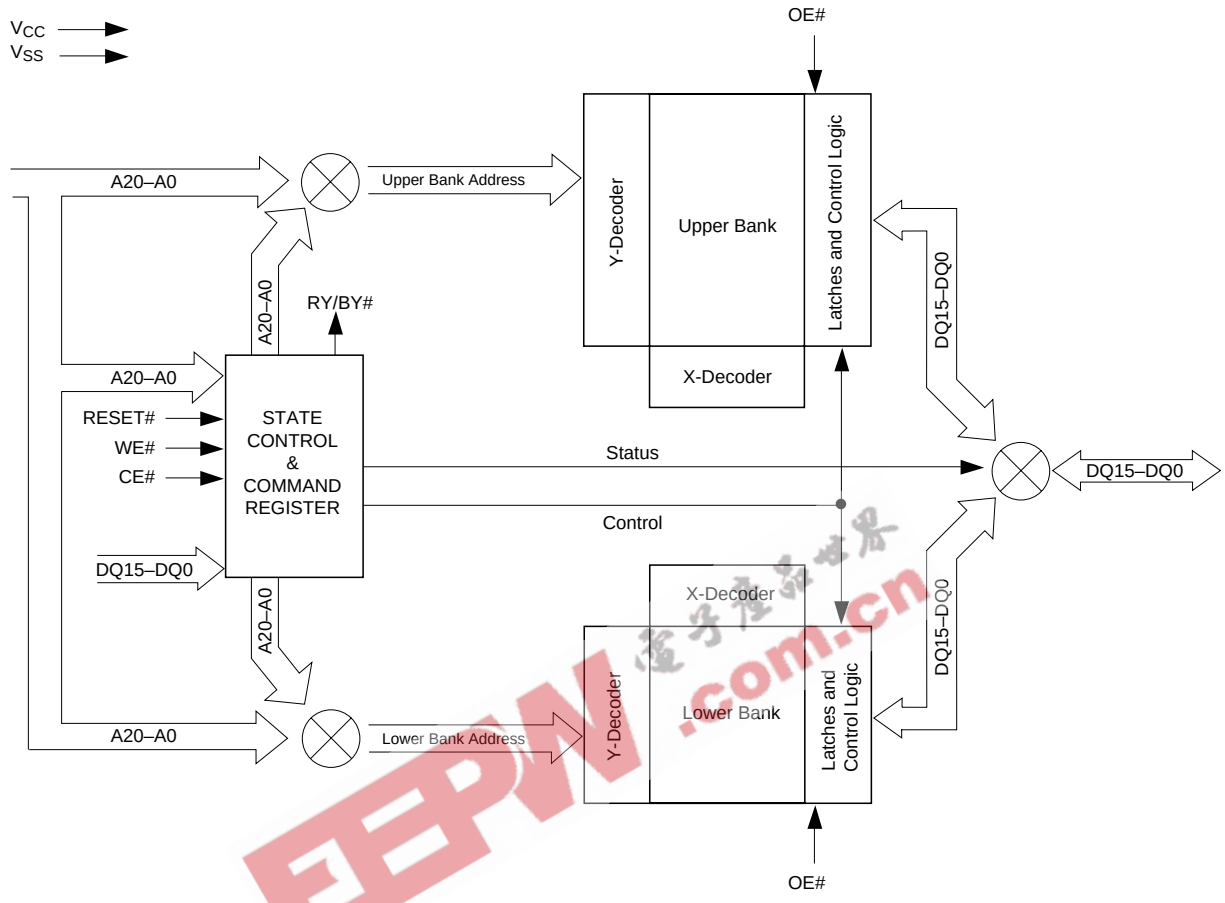
PRODUCT SELECTOR GUIDE

Part Number		Am41PDS3224D		
Speed Options	Standard Voltage Range: V_{CC} = 1.8–2.2 V	Flash Memory		SRAM
		10	11	10, 11
Max Access Time (ns)		100	110	70
CE# Access (ns)		100	110	70
OE# Access (ns)		35	40	35
Max Page Address Access Time (ns)		40	45	N/A

MCP BLOCK DIAGRAM

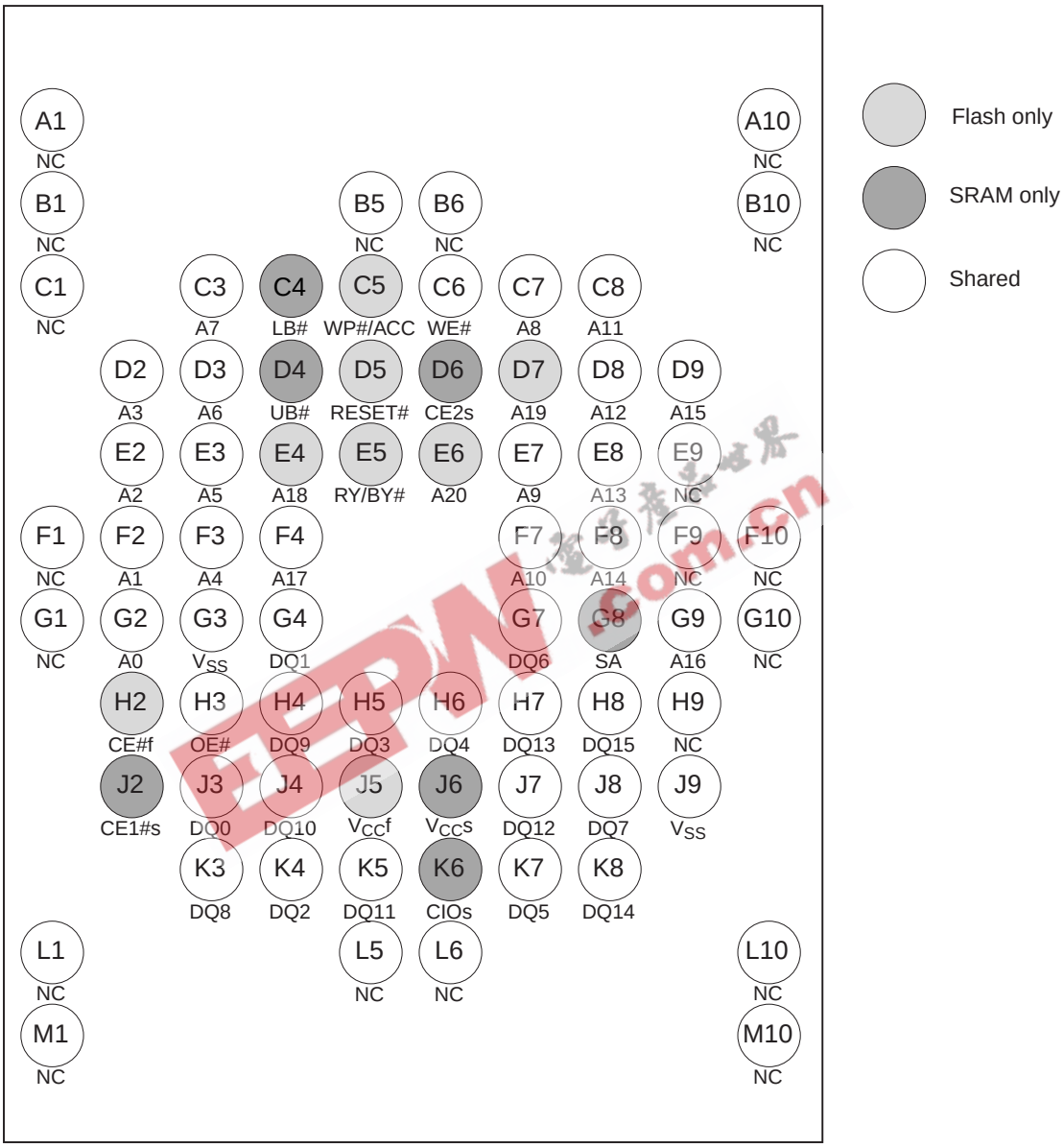


FLASH MEMORY BLOCK DIAGRAM



CONNECTION DIAGRAM

73-Ball FBGA
Top View



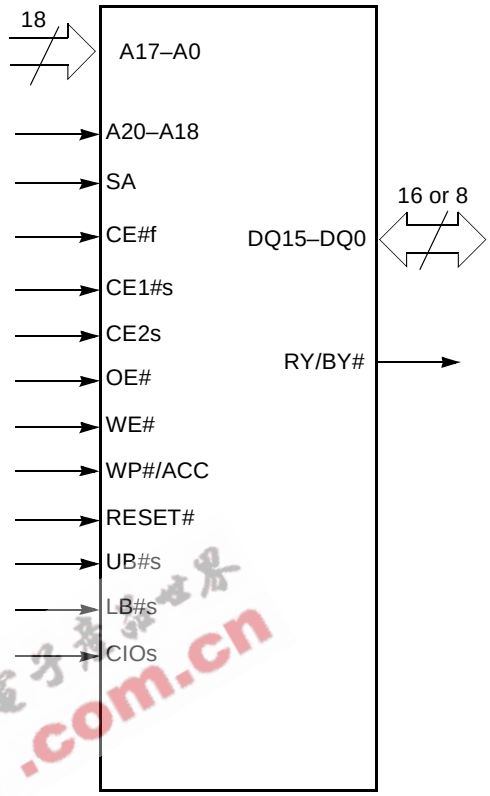
Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (TSOP, BGA, PLCC, PDIP, SSOP). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

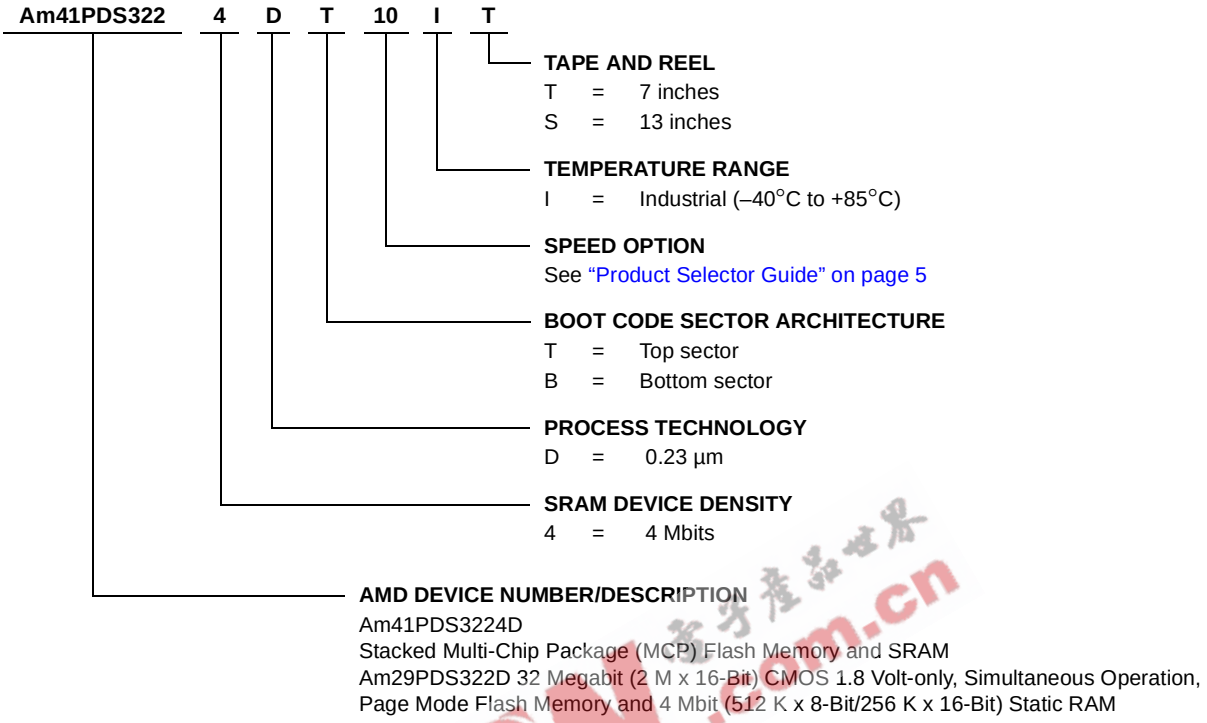
A17–A0	=	18 Address Inputs (Common)
A20–A18	=	3 Address Inputs (Flash)
SA	=	Highest Order Address Pin (SRAM) Byte mode
DQ15–DQ0	=	16 Data Inputs/Outputs (Common)
CE#f	=	Chip Enable (Flash)
CE1#s	=	Chip Enable 1 (SRAM)
CE2s	=	Chip Enable 2 (SRAM)
OE#	=	Output Enable (Common)
WE#	=	Write Enable (Common)
RY/BY#	=	Ready/Busy Output (Flash)
UB#s	=	Upper Byte Control (SRAM)
LB#s	=	Lower Byte Control (SRAM)
CIOs	=	I/O Configuration (SRAM) CIOs = V_{IH} = Word mode (x16), CIOs = V_{IL} = Byte mode (x8)
RESET#	=	Hardware Reset Pin, Active Low
WP#/ACC	=	Hardware Write Protect/ Acceleration Pin (Flash)
V_{CC}f	=	Flash 1.8 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{CC}s	=	SRAM Power Supply
V_{SS}	=	Device Ground (Common)
NC	=	Pin Not Connected Internally

LOGIC SYMBOL



ORDERING INFORMATION

The order number (Valid Combination) is formed by the following:



Valid Combinations		
Order Number		**Package Marking**
Am41PDS3224DT10I Am41PDS3224DB10I	T, S	M410000077 M410000078
Am41PDS3224DT11I Am41PDS3224DB11I		M410000079 M41000007A

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations

MCP DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Tables 1–2 list the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations—SRAM Word Mode, CIOs = V_{CC}

Operation (Notes 1, 2)	CE#f	CE1#s	CE2s	OE#	WE#	SA	Addr.	LB#s (Note 3)	UB#s (Note 3)	RESET#	WP#/ACC (Note 4)	DQ7–DQ0	DQ15–DQ8
Read from Flash	L	H	X	L	H	X	A_{IN}	X	X	H	L/H	D_{OUT}	D_{OUT}
		X	L										
Write to Flash	L	H	X	H	L	X	A_{IN}	X	X	H	(Note 4)	D_{IN}	D_{IN}
		X	L										
Standby	V_{CC} ± 0.3 V	H	X	X	X	X	X	X	X	V_{CC} ± 0.3 V	H	High-Z	High-Z
		X	L										
Output Disable	L	L	H	H	H	X	X	L	X	H	L/H	High-Z	High-Z
				H	H	X	X	X	L				
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	L	L/H	High-Z	High-Z
		X	L										
Sector Protect (Note 5)	L	H	X	H	L	X	SADD, A6 = L, A1 = H, A0 = L	X	X	V_{ID}	L/H	D_{IN}	X
		X	L										
Sector Unprotect (Note 5)	L	H	X	H	L	X	SADD, A6 = H, A1 = H, A0 = L	X	X	V_{ID}	(Note 6)	D_{IN}	X
		X	L										
Temporary Sector Unprotect	X	H	X	X	X	X	X	X	X	V_{ID}	(Note 6)	D_{IN}	High-Z
		X	L										
Read from SRAM	H	L	H	L	H	X	A_{IN}	L	L	H	X	D_{OUT}	D_{OUT}
								H	L			High-Z	D_{OUT}
								L	H			D_{OUT}	High-Z
Write to SRAM	H	L	H	X	L	X	A_{IN}	L	L	H	L/H	D_{IN}	D_{IN}
								H	L			High-Z	D_{IN}
								L	H			D_{IN}	High-Z

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 9–11 V, V_{HH} = 9.0 ± 0.5 V, X = Don't Care, SA = SRAM Address Input, Byte Mode, SADD = Flash Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Other operations except for those indicated in this column are inhibited.*
2. *Do not apply CE#f = V_{IL}, CE1#s = V_{IL} and CE2s = V_{IH} at the same time.*
3. *Don't care or open LB#s or UB#s.*
4. *If WP#/ACC = V_{IL} , the boot sectors will be protected. If WP#/ACC = V_{IH} the boot sectors protection will be removed. If WP#/ACC = V_{ACC} (9V), the program time will be reduced by 40%.*
5. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector/Sector Block Protection and Unprotection" section.*
6. *If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If WP#/ACC = $V_{HH,}$ all sectors will be unprotected.*

Table 2. Device Bus Operations—SRAM Byte Mode, CIOs = V_{SS}

Operation (Notes 1, 2)	CE#f	CE1#s	CE2s	OE#	WE#	SA	Addr.	LB#s (Note 3)	UB#s (Note 3)	RESET#	WP#/ACC (Note 4)	DQ7–DQ0	DQ15–DQ8
Read from Flash	L	H	X	L	H	X	A_{IN}	X	X	H	L/H	D_{OUT}	D_{OUT}
		X	L										
Write to Flash	L	H	X	H	L	X	A_{IN}	X	X	H	(Note 3)	D_{IN}	D_{IN}
		X	L										
Standby	V_{CC} ± 0.3 V	H	X	X	X	X	X	X	X	V_{CC} ± 0.3 V	H	High-Z	High-Z
		X	L										
Output Disable	L	L	H	H	H	SA	X	DNU	DNU	H	L/H	High-Z	High-Z
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	L	L/H	High-Z	High-Z
		X	L										
Sector Protect (Note 5)	L	H	X	H	L	X	SADD, A6 = L, A1 = H, A0 = L	X	X	V_{ID}	L/H	D_{IN}	X
		X	L										
Sector Unprotect (Note 5)	L	H	X	H	L	X	SADD, A6 = H, A1 = H, A0 = L	X	X	V_{ID}	(Note 6)	D_{IN}	X
		X	L										
Temporary Sector Unprotect	X	H	X	X	X	X	A_{IN}	X	X	V_{ID}	(Note 6)	D_{IN}	High-Z
		X	L										
Read from SRAM	H	L	H	L	H	SA	A_{IN}	X	X	H	X	D_{OUT}	High-Z
Write to SRAM	H	L	H	X	L	SA	A_{IN}	X	X	H	X	D_{IN}	High-Z

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 9–11 V, V_{HH} = 9.0 ± 0.5 V, X = Don't Care, SA = SRAM Address Input, Byte Mode, SADD = Flash Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out, DNU = Do Not Use*

Notes:

1. *Other operations except for those indicated in this column are inhibited.*
2. *Do not apply CE#f = V_{IL}, CE1#s = V_{IL} and CE2s = V_{IH} at the same time.*
3. *Don't care or open LB#s or UB#s.*
4. *If WP#/ACC = V_{IL} , the boot sectors will be protected. If WP#/ACC = V_{IH} the boot sectors protection will be removed. If WP#/ACC = V_{ACC} (9V), the program time will be reduced by 40%.*
5. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector/Sector Block Protection and Unprotection" section.*
6. *If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If WP#/ACC = $V_{HH,}$ all sectors will be unprotected.*

FLASH DEVICE BUS OPERATIONS

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE#f and OE# pins to V_{IL}. CE#f is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

See “Requirements for Reading Array Data” for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 15 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Read Mode

Random Read (Non-Page Mode Read)

The device has two control functions which must be satisfied in order to obtain data at the outputs. CE# is the power control and should be used for device selection. OE# is the output control and should be used to gate data to the output pins if the device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output pins. The output enable access time is the delay from the falling edge of OE# to valid data at the output pins (assuming the addresses have been stable for at least $t_{ACC}–t_{OE}$ time).

Page Mode Read

The device is capable of fast Page mode read and is compatible with the Page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The Page size of the device is 4 words. The appropriate Page is selected by the higher address bits A20–A0 and the LSB bits A1–A0 determine the specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent Page read accesses (as long as the locations specified by the microprocessor fall within that Page) are equivalent to t_{PACC}. When CE# is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Here again, CE# selects the device and OE# is the output control and should be used to gate data to the output pins if the device is selected. Fast Page mode accesses are obtained by keeping A20–A2 constant and changing A1–A0 to select the specific word within that page. See Figure 16 for timing specifications.

The following table determines the specific word within the selected page:

Table 3. Page Word Mode

Word	A1	A0
Word 0	0	0
Word 1	0	1
Word 2	1	0
Word 3	1	1

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. The “Word Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 3 indicates the address space that each sector occupies.

I_{CC2}f in the DC Characteristics table represents the active current specification for the write mode. The Measurements performed by placing a 50Ω termination on the data pin with a bias of $V_{CC}/2$. The time from OE# high to the data bus driven to $V_{CC}/2$ is taken as t_{DF}AC Characteristics. section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors,

and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the ACC pin returns the device to normal operation.

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in the other bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 21 shows how read and write cycles may be initiated for simultaneous operation with zero latency. I_{CC6} and I_{CC7} in the Flash DC Characteristics table represent the current specifications for read-while-program and read-while-erase, respectively.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE#f and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE#f and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the Flash DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system.

Automatic sleep mode current is drawn when CE# = $V_{SS} \pm 0.3$ V and *all inputs* are held at $V_{CC} \pm 0.3$ V. If CE# and RESET# voltages are not held within these tolerances, the automatic sleep mode current will be greater.

I_{CC5}f in the Flash DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3$ V, the device draws CMOS standby current (I_{CC3}f). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.3$ V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 17 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 4. Am29PDS322DT Top Boot Sector Addresses

Bank	Sector	Sector Address A20–A12	Sector Size (Kwords)	(x16) Address Range
Bank 2	SA0	000000xxx	32	000000h–07FFFh
	SA1	000001xxx	32	008000h–0FFFFh
	SA2	000010xxx	32	010000h–17FFFh
	SA3	000011xxx	32	018000h–01FFFFh
	SA4	000100xxx	32	020000h–027FFFh
	SA5	000101xxx	32	028000h–02FFFFh
	SA6	000110xxx	32	030000h–037FFFh
	SA7	000111xxx	32	038000h–03FFFFh
	SA8	001000xxx	32	040000h–047FFFh
	SA9	001001xxx	32	048000h–04FFFFh
	SA10	001010xxx	32	050000h–057FFFh
	SA11	001011xxx	32	058000h–05FFFFh
	SA12	001100xxx	32	060000h–067FFFh
	SA13	001101xxx	32	068000h–06FFFFh
	SA14	001110xxx	32	070000h–077FFFh
	SA15	001111xxx	32	078000h–07FFFFh
	SA16	010000xxx	32	080000h–087FFFh
	SA17	010001xxx	32	088000h–08FFFFh
	SA18	010010xxx	32	090000h–097FFFh
	SA19	010011xxx	32	098000h–09FFFFh
	SA20	010100xxx	32	0A0000h–0A7FFFh
	SA21	010101xxx	32	0A8000h–0AFFFFh
	SA22	010110xxx	32	0B0000h–0B7FFFh
	SA23	010111xxx	32	0B8000h–0BFFFFh
	SA24	011000xxx	32	0C0000h–0C7FFFh
	SA25	011001xxx	32	0C8000h–0CFFFFh
	SA26	011010xxx	32	0D0000h–0D7FFFh
	SA27	011011xxx	32	0D8000h–0DFFFFh
	SA28	011100xxx	32	0E0000h–0E7FFFh
	SA29	011101xxx	32	0E8000h–0EFFFFh
	SA30	011110xxx	32	0F0000h–0F7FFFh
	SA31	011111xxx	32	0F8000h–0FFFFFh
	SA32	100000xxx	32	100000h–107FFFh
	SA33	100001xxx	32	108000h–10FFFFh
	SA34	100010xxx	32	110000h–117FFFh
	SA35	100011xxx	32	118000h–11FFFFh
	SA36	100100xxx	32	120000h–127FFFh
	SA37	100101xxx	32	128000h–12FFFFh
	SA38	100110xxx	32	130000h–137FFFh
	SA39	100111xxx	32	138000h–13FFFFh
	SA40	101000xxx	32	140000h–147FFFh
	SA41	101001xxx	32	148000h–14FFFFh
	SA42	101010xxx	32	150000h–157FFFh
	SA43	101011xxx	32	158000h–15FFFFh

Table 4. Am29PDS322DT Top Boot Sector Addresses (Continued)

Bank	Sector	Sector Address A20–A12	Sector Size (Kwords)	(x16) Address Range
Bank 2	SA44	101100xxx	32	160000h–167FFFh
	SA45	101101xxx	32	168000h–16FFFFh
	SA46	101110xxx	32	170000h–177FFFh
	SA47	101111xxx	32	178000h–17FFFFh
	SA48	110000xxx	32	180000h–187FFFh
	SA49	110001xxx	32	188000h–18FFFFh
	SA50	110010xxx	32	190000h–197FFFh
	SA51	110011xxx	32	198000h–19FFFFh
	SA52	110100xxx	32	1A0000h–1A7FFFh
	SA53	110101xxx	32	1A8000h–1AFFFFh
	SA54	110110xxx	32	1B0000h–1B7FFFh
	SA55	110111xxx	32	1B8000h–1BFFFFh
Bank 1	SA56	111000xxx	32	1C0000h–1C7FFFh
	SA57	111001xxx	32	1C8000h–1CFFFFh
	SA58	111010xxx	32	1D0000h–1D7FFFh
	SA59	111011xxx	32	1D8000h–1DFFFFh
	SA60	111100xxx	32	1E0000h–1E7FFFh
	SA61	111101xxx	32	1E8000h–1EFFFFh
	SA62	111110xxx	32	1F0000h–1F7FFFh
	SA63	111111000	4	1F8000h–1F8FFFh
	SA64	111111001	4	1F9000h–1F9FFFh
	SA65	111111010	4	1FA000h–1FAFFFh
	SA66	111111011	4	1FB000h–1FBFFFh
	SA67	111111100	4	1FC000h–1FCFFFh
	SA68	111111101	4	1FD000h–1FDFFFh
	SA69	111111110	4	1FE000h–1FEFFFh
	SA70	111111111	4	1FF000h–1FFFFFh

Table 5. Am29PDS322DT Top Boot SecSi Sector Address

Sector Address A20–A12	Sector Size	(x16) Address Range
111111xxx	32	1F8000h–1FFFFh

Table 6. Am29PDS322DB Bottom Boot Sector Addresses

Bank	Sector	Sector Address A20–A12	Sector Size (Kwords)	(x16) Address Range
Bank 1	SA0	000000000	4	000000h–000FFFh
	SA1	000000001	4	001000h–001FFFh
	SA2	000000010	4	002000h–002FFFh
	SA3	000000011	4	003000h–003FFFh
	SA4	000000100	4	004000h–004FFFh
	SA5	000000101	4	005000h–005FFFh
	SA6	000000110	4	006000h–006FFFh
	SA7	000000111	4	007000h–007FFFh
	SA8	000001xxx	32	008000h–00FFFFh
	SA9	000010xxx	32	010000h–017FFFh
	SA10	000011xxx	32	018000h–01FFFFh
	SA11	000100xxx	32	020000h–027FFFh
	SA12	000101xxx	32	028000h–02FFFFh
	SA13	000110xxx	32	030000h–037FFFh
	SA14	000111xxx	32	038000h–03FFFFh

Table 6. Am29PDS322DB Bottom Boot Sector Addresses (Continued)

Bank	Sector	Sector Address A20–A12	Sector Size (Kwords)	(x16) Address Range
Bank 2	SA15	001000xxx	32	040000h–047FFFh
	SA16	001001xxx	32	048000h–04FFFFh
	SA17	001010xxx	32	050000h–057FFFh
	SA18	001011xxx	32	058000h–05FFFFh
	SA19	001100xxx	32	060000h–067FFFh
	SA20	001101xxx	32	068000h–06FFFFh
	SA21	001110xxx	32	070000h–077FFFh
	SA22	001111xxx	32	078000h–07FFFFh
	SA23	010000xxx	32	080000h–087FFFh
	SA24	010001xxx	32	088000h–08FFFFh
	SA25	010010xxx	32	090000h–097FFFh
	SA26	010011xxx	32	098000h–09FFFFh
	SA27	010100xxx	32	0A0000h–0A7FFFh
	SA28	010101xxx	32	0A8000h–0AFFFFh
	SA29	010110xxx	32	0B0000h–0B7FFFh
	SA30	010111xxx	32	0B8000h–0BFFFFh
	SA31	011000xxx	32	0C0000h–0C7FFFh
	SA32	011001xxx	32	0C8000h–0CFFFFh
	SA33	011010xxx	32	0D0000h–0D7FFFh
	SA34	011011xxx	32	0D8000h–0DFFFFh
	SA35	011100xxx	32	0E0000h–0E7FFFh
	SA36	011101xxx	32	0E8000h–0EFFFFh
	SA37	011110xxx	32	0F0000h–0F7FFFh
	SA38	011111xxx	32	0F8000h–0FFFFFh
	SA39	100000xxx	32	100000h–107FFFh
	SA40	100001xxx	32	108000h–10FFFFh
	SA41	100010xxx	32	110000h–117FFFh
	SA42	100011xxx	32	118000h–11FFFFh
	SA43	100100xxx	32	120000h–127FFFh
	SA44	100101xxx	32	128000h–12FFFFh
	SA45	100110xxx	32	130000h–137FFFh
	SA46	100111xxx	32	138000h–13FFFFh
	SA47	101000xxx	32	140000h–147FFFh
	SA48	101001xxx	32	148000h–14FFFFh
	SA49	101010xxx	32	150000h–157FFFh
	SA50	101011xxx	32	158000h–15FFFFh
	SA51	101100xxx	32	160000h–167FFFh
	SA52	101101xxx	32	168000h–16FFFFh
	SA53	101110xxx	32	170000h–177FFFh
	SA54	101111xxx	32	178000h–17FFFFh
	SA55	111000xxx	32	180000h–187FFFh
	SA56	110001xxx	32	188000h–18FFFFh
	SA57	110010xxx	32	190000h–197FFFh
	SA58	110011xxx	32	198000h–19FFFFh
	SA59	110100xxx	32	1A0000h–1A7FFFh
	SA60	110101xxx	32	1A8000h–1AFFFFh
	SA61	110110xxx	32	1B0000h–1B7FFFh
	SA62	110111xxx	32	1B8000h–1BFFFFh

Table 6. Am29PDS322DB Bottom Boot Sector Addresses (Continued)

Bank	Sector	Sector Address A20–A12	Sector Size (Kwords)	(x16) Address Range
Bank 2	SA63	111000xxx	32	1C0000h–1C7FFFh
	SA64	111001xxx	32	1C8000h–1CFFFFh
	SA65	111010xxx	32	1D0000h–1D7FFFh
	SA66	111011xxx	32	1D8000h–1DFFFFh
	SA67	111100xxx	32	1E0000h–1E7FFFh
	SA68	111101xxx	32	1E8000h–1EFFFFh
	SA69	111110xxx	32	1F0000h–1F7FFFh
	SA70	111111xxx	32	1F8000h–1FFFFFh

Table 7. Am29PDS322DB Bottom Boot SecSi Sector Address

Sector Address A20–A12	Sector Size	(x16) Address Range
000000xxx	32	00000h-07FFFh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ15–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm.

The autoselect codes can also be accessed in-system through the command register. The host system can issue the autoselect command via the command register, as shown in Table 10. This method does not require V_{ID}. Refer to the Autoselect Command Sequence section for more information.

Sector/Sector Block Protection and Unprotection

(Note: For the following discussion, the term “sector” applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Tables 8 and 9).

Table 8. Top Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector Group	Sectors	A20–A12	Sector/ Sector Block Size
SGA0	SA0	000000XXX	64 (1x64) Kbytes
SGA1	SA1–SA3	00001XXXX	192 (3x64) Kbytes
SGA2	SA4–SA7	0001XXXXX	256 (4x64) Kbytes
SGA3	SA8–SA11	0010XXXXX	256 (4x64) Kbytes
SGA4	SA12–SA15	0011XXXXX	256 (4x64) Kbytes
SGA5	SA16–SA19	0100XXXXX	256 (4x64) Kbytes
SGA6	SA20–SA23	0101XXXXX	256 (4x64) Kbytes
SGA7	SA24–SA27	0110XXXXX	256 (4x64) Kbytes
SGA8	SA28–SA31	0111XXXXX	256 (4x64) Kbytes
SGA9	SA32–SA35	1000XXXXX	256 (4x64) Kbytes
SGA10	SA36–SA39	1001XXXXX	256 (4x64) Kbytes
SGA11	SA40–SA43	1010XXXXX	256 (4x64) Kbytes
SGA12	SA44–SA47	1011XXXXX	256 (4x64) Kbytes
SGA13	SA48–SA51	1100XXXXX	256 (4x64) Kbytes
SGA14	SA52–SA55	1101XXXXX	256 (4x64) Kbytes
SGA15	SA56–SA59	1110XXXXX	256 (4x64) Kbytes
SGA16	SA60–SA62	111100XXX	192 (3x64) Kbytes
SGA17	SA63	111111000	8 Kbytes
SGA18	SA64	111111001	8 Kbytes
SGA19	SA65	111111010	8 Kbytes
SGA20	SA66	111111011	8 Kbytes
SGA21	SA67	111111100	8 Kbytes
SGA22	SA68	111111101	8 Kbytes
SGA23	SA69	111111110	8 Kbytes
SGA24	SA70	111111111	8 Kbytes

Table 9. Bottom Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector Group	Sectors	A20–A12	Sector/Sector Block Size
SGA0	SA70	111111XXX	64 (1x64) Kbytes
SGA1	SA69–SA67	11110XXXX	192 (3x64) Kbytes
SGA2	SA66–SA63	1110XXXXX	256 (4x64) Kbytes
SGA3	SA62–SA59	1101XXXXX	256 (4x64) Kbytes
SGA4	SA58–SA55	1100XXXXX	256 (4x64) Kbytes
SGA5	SA54–SA51	1011XXXXX	256 (4x64) Kbytes
SGA6	SA50–SA47	1010XXXXX	256 (4x64) Kbytes
SGA7	SA46–SA43	1001XXXXX	256 (4x64) Kbytes
SGA8	SA42–SA39	1000XXXXX	256 (4x64) Kbytes
SGA9	SA38–SA35	0111XXXXX	256 (4x64) Kbytes
SGA10	SA34–SA31	0110XXXXX	256 (4x64) Kbytes
SGA11	SA30–SA27	0101XXXXX	256 (4x64) Kbytes
SGA12	SA26–SA23	0100XXXXX	256 (4x64) Kbytes
SGA13	SA22–SA19	0011XXXXX	256 (4x64) Kbytes
SGA14	SA18–SA15	0010XXXXX	256 (4x64) Kbytes
SGA15	SA14–SA11	0001XXXXX	256 (4x64) Kbytes
SGA16	SA10–SA8	000011XXX	192 (3x64) Kbytes
SGA17	SA7	000000111	8 Kbytes
SGA18	SA6	000000110	8 Kbytes
SGA19	SA5	000000101	8 Kbytes
SGA20	SA4	000000100	8 Kbytes
SGA21	SA3	000000011	8 Kbytes
SGA22	SA2	000000010	8 Kbytes
SGA23	SA1	000000001	8 Kbytes
SGA24	SA0	000000000	8 Kbytes

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

Sector protection and unprotection requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 26 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See the Autoselect Mode section for details.

Write Protect (WP#)

The Write Protect function provides a hardware method of protecting certain boot sectors without using V_{ID}. This function is one of two provided by the WP#/ACC pin.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the two "outermost" 8 Kbyte boot sectors independently of whether those sectors were protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". The two outermost 8 Kbyte boot sectors are the two sectors containing the lowest addresses in a top-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

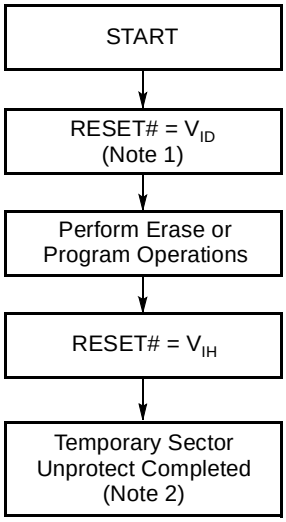
If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the two outermost 8 Kbyte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection".

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Temporary Sector/Sector Block Unprotect

(Note: For the following discussion, the term "sector" applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table 8).

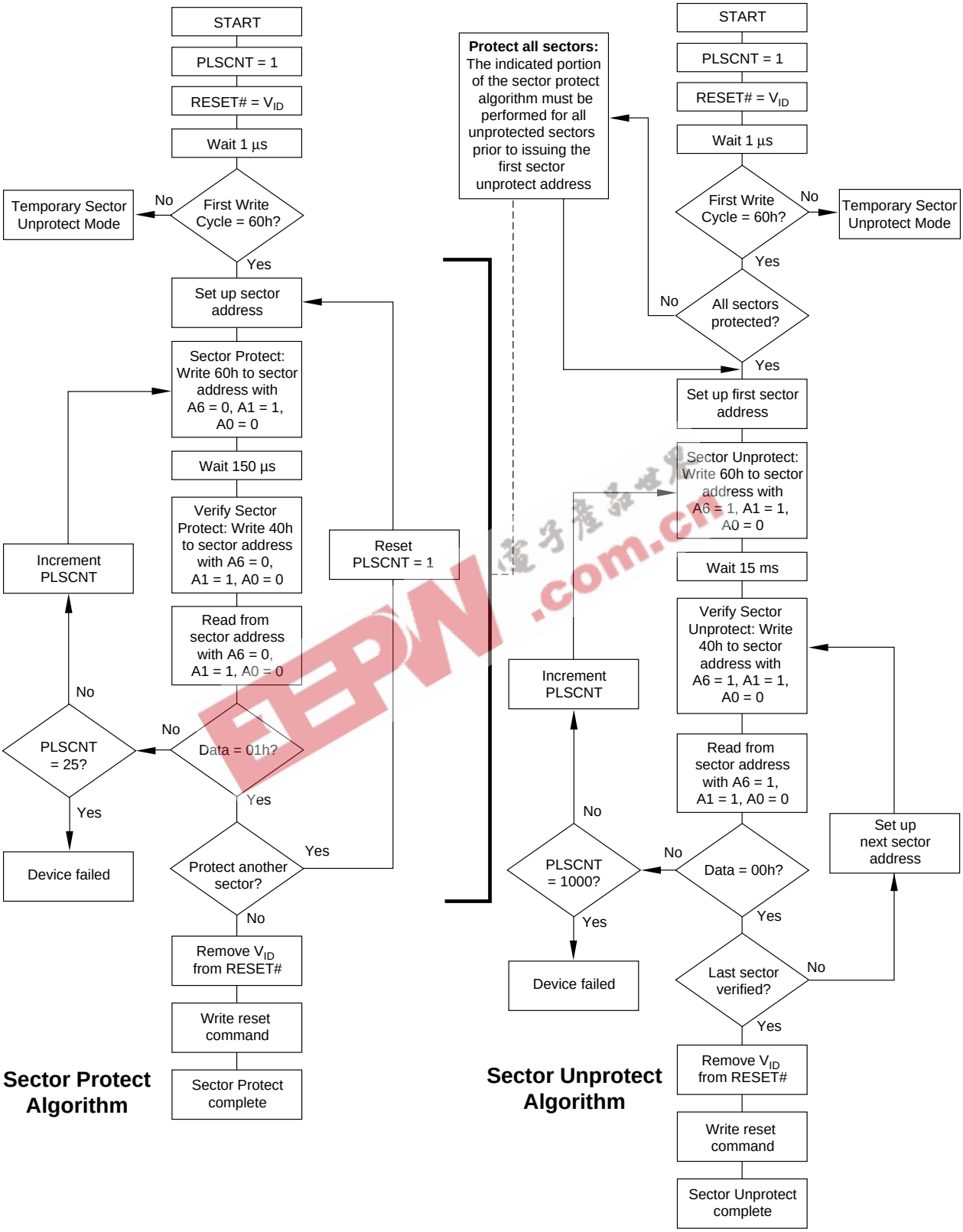
This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID} (9 V – 11 V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 1 shows the algorithm, and Figure 25 shows the timing diagrams, for this feature.



Notes:

1. *All protected sectors unprotected (If WP#/ACC = V_{IL}, outermost boot sectors will remain protected).*
2. *All previously protected sectors are protected once again.*

Figure 1. Temporary Sector Unprotect Operation



Note: *The term "sector" in the figure applies to both sectors and sector blocks.*

Figure 2. In-System Sector/Sector Block Protect and Unprotect Algorithms

SecSi (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is 64 KBytes in length, and uses a SecSi Sector Indicator Bit (DQ7) to indicate whether or not the SecSi Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

AMD offers the device with the SecSi Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory, and has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a "1." The customer-lockable version is shipped with the SecSi Sector unprotected, allowing customers to utilize that sector in any manner they choose. The customer-lockable version also has the SecSi Sector Indicator Bit permanently set to a "0." Thus, the SecSi Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The system accesses the SecSi Sector through a command sequence (see "Enter SecSi Sector/Exit SecSi Sector Command Sequence"). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the boot sectors instead of the SecSi sector

Factory Locked: SecSi Sector Programmed and Protected at the Factory

In a factory locked device, the SecSi Sector is protected when the device is shipped from the factory. The SecSi Sector cannot be modified in any way. The device is available preprogrammed with one of the following:

- A random, secure ESN only
- Customer code through the ExpressFlash service
- Both a random, secure ESN and customer code through the ExpressFlash service.

In devices that have an ESN, a Bottom Boot device will have the 16-byte ESN in the lowest addressable memory area at addresses 000000h–000007h. In the Top Boot device the starting address of the ESN will be at the bottom of the lowest 8 Kbyte boot sector at addresses 1F8000h–1F8007h.

Customers may opt to have their code programmed by AMD through the AMD ExpressFlash service. AMD programs the customer's code, with or without the random ESN. The devices are then shipped from AMD's factory with the permanently locked. Contact an AMD representative for details on using AMD's ExpressFlash service.

Customer Lockable: SecSi Sector NOT Programmed or Protected at the Factory

If the security feature is not required, the SecSi Sector can be treated as an additional Flash memory space, expanding the size of the available Flash array by 64 Kbytes. The SecSi Sector can be read, programmed, and erased as often as required. The SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the SecSi Sector without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.
- Write the three-cycle Enter SecSi Sector Region command sequence, and then use the alternate method of sector protection described in the "Sector/Sector Block Protection and Unprotection" section.

Once the SecSi Sector is locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing the remainder of the array.

The SecSi Sector protection must be used with caution since, once protected, there is no procedure available for unprotecting the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 10 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}.

The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE#f or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE#f = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE#f and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE#f = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

FLASH COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 10 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the MCP Device Bus Operations section for more information. The Read-Only Operations table provides the read parameters, and Figure 15 shows the timing diagram.

Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 10 shows the address and data requirements. The autoselect command sequence may be written to an address that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read any number of autoselect codes without reinitiating the command sequence.

Table 10 shows the address and data requirements for the command sequence. To determine sector protection information, the system must write to the appropriate sector group address (SGA). Tables 4 and 6 show the address range associated with each sector.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

Enter SecSi Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing an 16-byte random Electronic Serial Number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. Table 10 shows the address and data requirements for both command sequences. See also “SecSi (Secured Silicon) Sector Flash Memory Region” for further information. Note that a hardware reset (RESET#=V_{IL}) will reset the device to reading array data.

Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 10 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the Flash Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from “0” back to a “1.”** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still “0.” Only erase operations can convert a “0” to a “1.”

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 10 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h. The second cycle must contain the data 00h. The device then returns to reading array data. See Figure 3 for the unlock bypass algorithm.

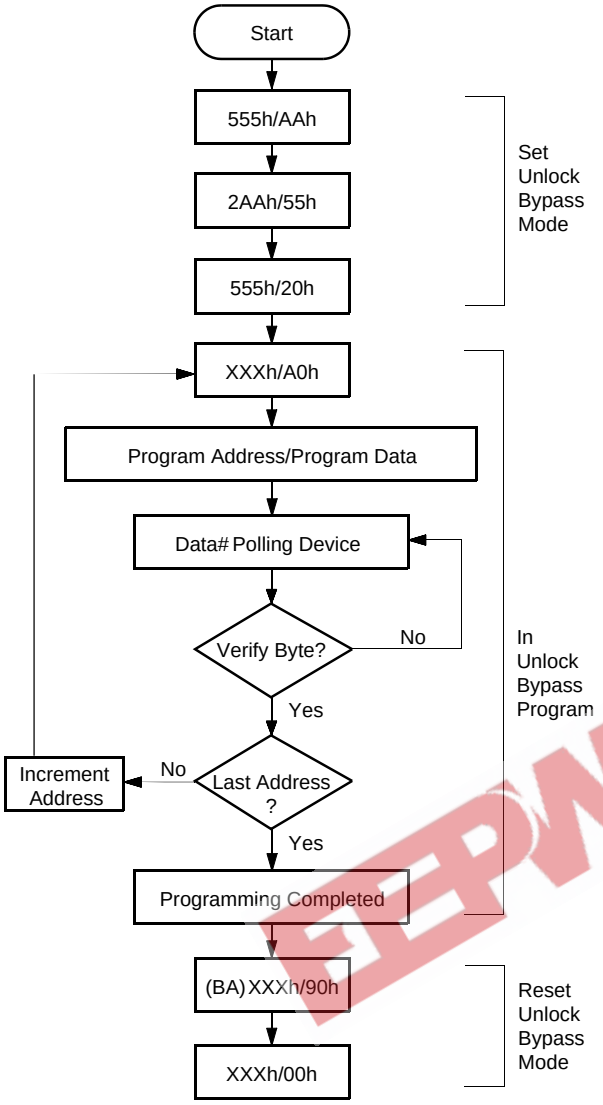
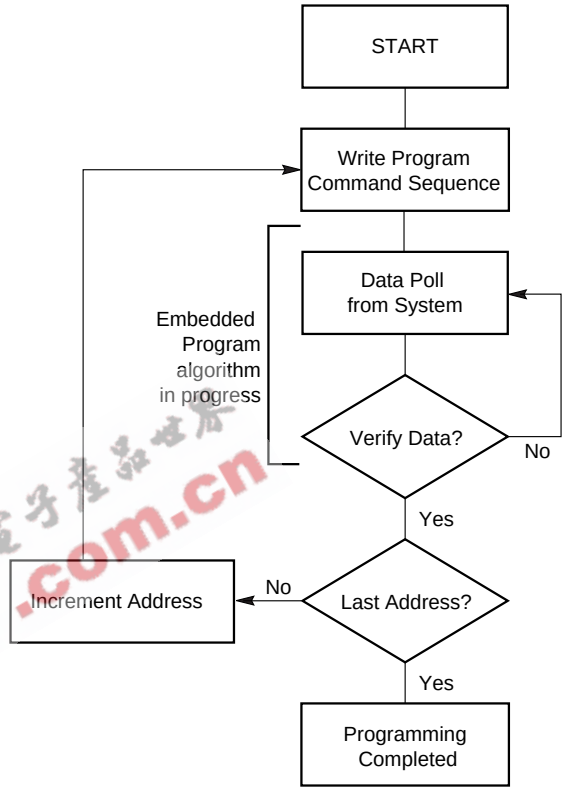


Figure 3. Unlock Bypass Algorithm

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. Note that the WP#/ACC pin must not be at V_{HH} any operation other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Figure 4 illustrates the algorithm for the program operation. Refer to the Flash Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 18 for timing diagrams.



Note: *See Table 10 for program command sequence.*

Figure 4. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 10 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Flash Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 5 illustrates the algorithm for the erase operation. Refer to the Flash Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 20 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 10 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing sector. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing sector. Refer to the Flash Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 5 illustrates the algorithm for the erase operation. Refer to the Flash Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 20 section for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Note that unlock bypass programming is not allowed when the device is erase-suspended.

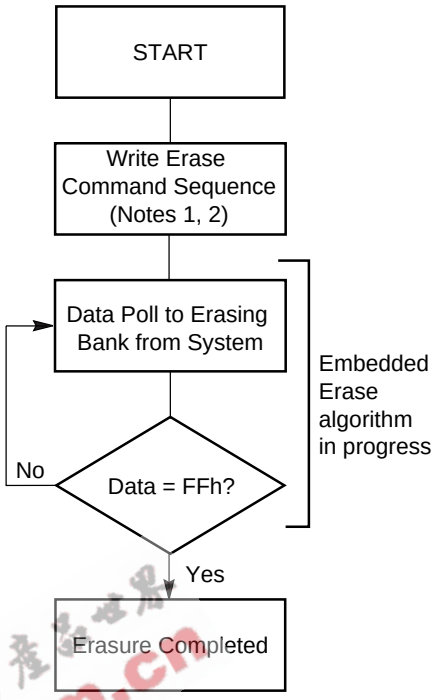
Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is

erase-suspended. Refer to the Flash Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard word program operation. Refer to the Flash Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Mode and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The address of the erase-suspended sector is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Notes:
1. *See Table 10 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 5. Erase Operation

Table 10. Am29PDS322D Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	0001				
	Device ID (Note 9)	4	555	AA	2AA	55	555	90	X01	227E	X0E	2206	X0F	2201/ 2200
	SecSi Sector Factory Protect (Note 10)	4	555	AA	2AA	55	555	90	X03	80/00				
	Sector Group Protect Verify (Note 11)	4	555	AA	2AA	55	555	90	(SGA) X02	XX00/ XX01				
Enter SecSi Sector Region		3	555	AA	2AA	55	555	88						
Exit SecSi Sector Region		4	555	AA	2AA	55	555	90	XXX	00				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 12)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 13)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 14)		1	BA	B0										
Erase Resume (Note 15)		1	BA	30										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SGA = Address of the sector group to be verified (in autoselect mode) or erased. Address bits A20–A12 uniquely select any sector.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth and fifth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.*
5. *Unless otherwise noted, address bits A20–A12 are don't cares in unlock sequence.*
6. *No unlock or command cycles required when device is in read mode.*
7. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the autoselect mode, or if DQ5 goes high (while the device is providing status information).*
8. *The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address to obtain the manufacturer ID, device ID, or SecSi Sector factory protect information. Data bits DQ15–DQ8 are don't care. See the Autoselect Command Sequence section for more information.*
9. *The device ID must be read across the fourth, fifth and sixth cycles. The sixth cycle specifies 2201h for top boot or 2200h for bottom boot.*
10. *The data is 80h for factory locked and 00h for not factory locked.*
11. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*
12. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
13. *The Unlock Bypass Reset command is required to return to the read mode when the device is in the unlock bypass mode.*
14. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase*
15. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*

FLASH WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 11 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

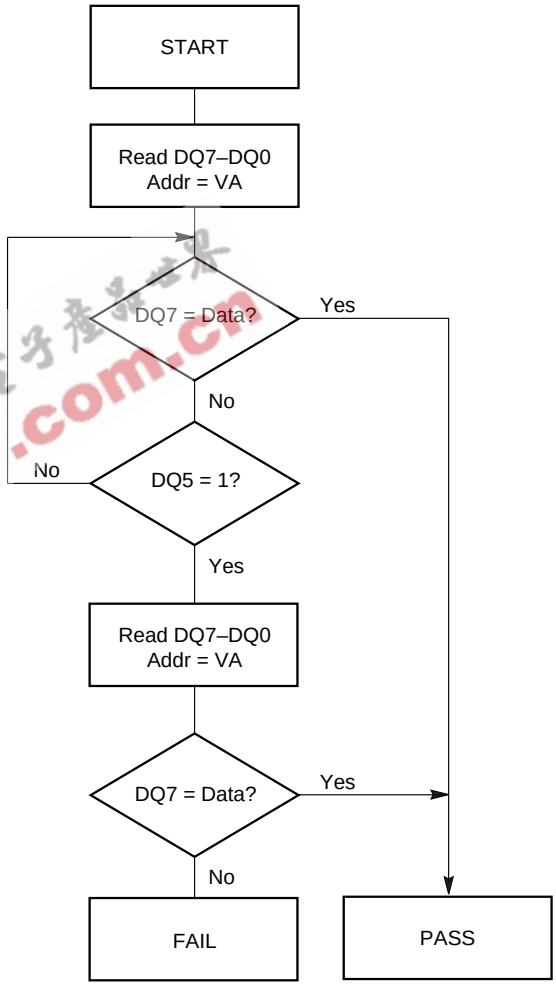
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the bank returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6–DQ0 may be still invalid. Valid data on DQ7–DQ0 will appear on successive read cycles.

Table 11 shows the outputs for Data# Polling on DQ7. Figure 6 shows the Data# Polling algorithm. Figure 22 in the Flash AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 6. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or the device is in the erase-suspend-read mode.

Table 11 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

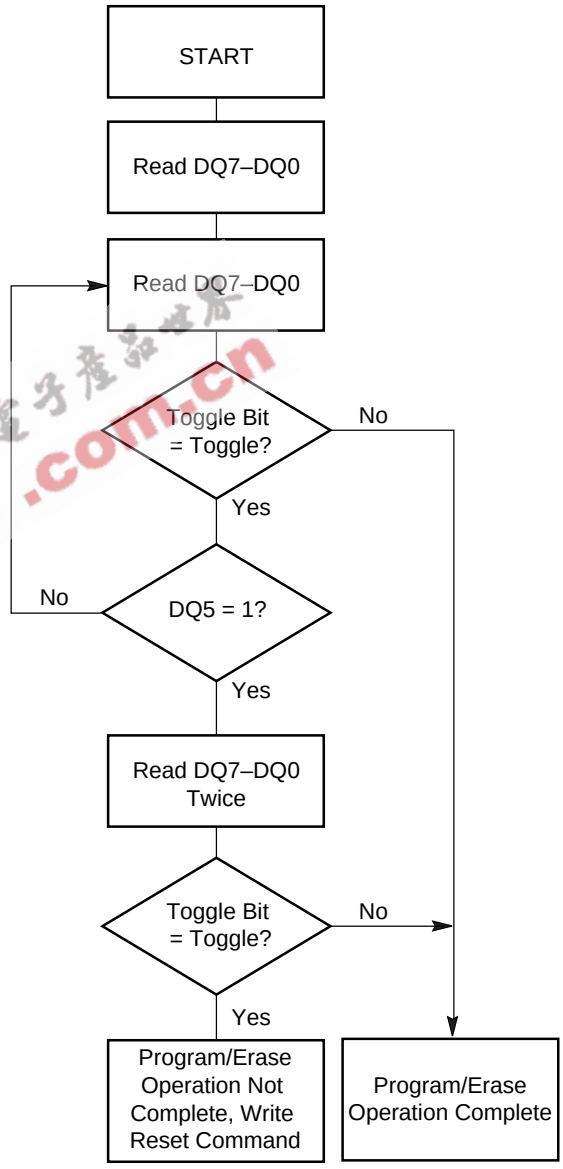
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 11 shows the outputs for Toggle Bit I on DQ6. Figure 7 shows the toggle bit algorithm. Figure 23 in the “Measurements performed by placing a 50Ω termination on the data pin with a bias of $V_{CC}/2$. The time from OE# high to the data bus driven to $V_{CC}/2$ is taken as t_{DF}AC Characteristics.” section shows the toggle bit timing diagrams. Figure 24 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.



Note: *The system should recheck the toggle bit even if DQ5 = “1” because the toggle bit may stop toggling as DQ5 changes to “1.” See the subsections on DQ6 and DQ2 for more information.*

Figure 7. Toggle Bit Algorithm

DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 11 to compare outputs for DQ2 and DQ6.

Figure 7 shows the toggle bit algorithm in flowchart form, and the section “DQ2: Toggle Bit II” explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 23 shows the toggle bit timing diagram. Figure 24 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 7 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 7).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed.

The device may output a “1” on DQ5 if the system tries to program a “1” to a location that was previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a “1.”

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if the device was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 11 shows the status of DQ3 relative to the other status bits.

Table 11. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –55°C to +125°C

Ambient Temperature
with Power Applied . . . . . –40°C to +85°C

Voltage with Respect to Ground

V_{CC}f/V_{CC}s (Note 1) . . . . . –0.3 V to +2.5 V

RESET# (Note 2) . . . . . –0.5 V to +11 V

WP#/ACC . . . . . –0.5 V to +10.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . 100 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 8. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 9.*
2. *Minimum DC input voltage on pins OE#, RESET#, and WP#/ACC is –0.5 V. During voltage transitions, OE#, WP#/ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 8. Maximum DC input voltage on pin RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage on WP#/ACC is +9.5 V which may overshoot to +12.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

V_{CC}f/V_{CC}s Supply Voltage

V_{CC}f/V_{CC}s for standard voltage range . . 1.8 V to 2.2 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

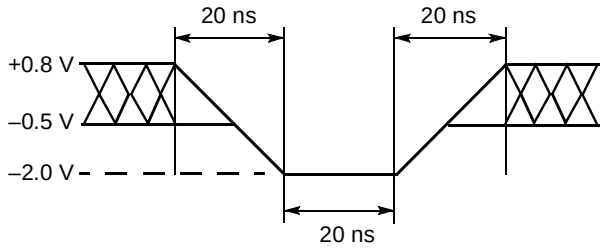


Figure 8. Maximum Negative Overshoot Waveform

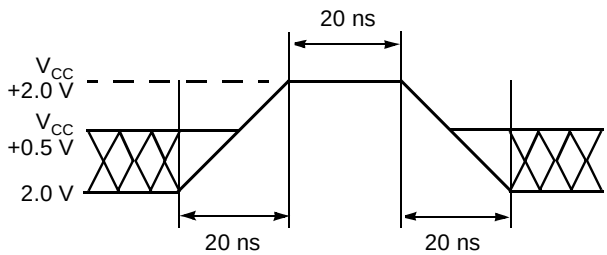


Figure 9. Maximum Positive Overshoot Waveform

FLASH DC CHARACTERISTICS

CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	RESET# Input Load Current	$V_{CC} = V_{CC\ max}$; RESET# = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIA}	ACC Input Leakage Current	$V_{CC} = V_{CC\ max}$, WP#/ACC = $V_{ACC\ max}$				35	µA
$I_{CC1}f$	Flash V_{CC} Active Inter-Page Read Current (Notes 1, 2)	CE#f = V_{IL}, OE# = V_{IH},	1 MHz		2.5	3	mA
			10 MHz		24	28	
$I_{CC2}f$	Flash V_{CC} Active Write Current (Notes 2, 3)	CE#f = V_{IL}, OE# = V_{IH}			15	30	mA
$I_{CC3}f$	Flash V_{CC} Standby Current (Note 2)	$V_{CC}f = V_{CC\ max}$, CE#f, RESET# = $V_{CC} \pm 0.3$ V			0.2	5	µA
$I_{CC4}f$	Flash V_{CC} Reset Current (Note 2)	$V_{CC}f = V_{CC\ max}$, WP#/ACC = $V_{CC}f \pm 0.3$ V, RESET# = $V_{SS} \pm 0.3$ V			0.1	5	µA
$I_{CC5}f$	Flash V_{CC} Automatic Sleep Mode Current (Notes 2, 4)	$V_{CC}f = V_{CC\ max}$, CE#f = $V_{SS} \pm 0.3$ V; RESET# = $V_{CC} \pm 0.3$ V, $V_{IN} = V_{CC} \pm 0.3$ V or $V_{SS} \pm 0.3$ V			0.2	5	µA
$I_{CC6}f$	Flash V_{CC} Active Read-While-Program Current (Notes 1, 2, 5)	CE#f = V_{IL}, OE# = V_{IH}			30	55	mA
$I_{CC7}f$	Flash V_{CC} Active Read-While-Erase Current (Notes 1, 2, 5)	CE#f = V_{IL}, OE# = V_{IH}			30	55	mA
$I_{CC8}f$	Flash V_{CC} Active Program-While-Erase-Suspended Current (Note 2)	CE#f = V_{IL}, OE# = V_{IH}			17	35	mA
$I_{CC9}f$	Flash V_{CC} Active Intra-Page Read Current	CE#f = V_{IL}, OE# = V_{IH}	10 MHz		0.5	1	mA
			20 MHz		1	2	
I_{ACC}	WP#/ACC Accelerated Program Current	$V_{CC} = V_{CCMax}$, WP#/ACC = V_{ACCMax}			12	20	mA
V_{IL}	Input Low Voltage			–0.5		0.2 x V_{CC}	V
V_{IH}	Input High Voltage			0.8 x V_{CC}		V_{CC} + 0.3	V
V_{ACC}/V_{HH}	Voltage for WP#/ACC Program Acceleration and Sector Protection/Unprotection			8.5		9.5	V
V_{ID}	Voltage for Sector Protection, Autoselect and Temporary Sector Unprotect			9		11	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC}f = V_{CC}s = V_{CC\ min}$				0.1	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC}f = V_{CC}s = V_{CC\ min}$		0.85 x V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.1			
V_{LKO}	Flash Low V_{CC} Lock-Out Voltage (Note 5)			1.2		1.5	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.*
5. *Not 100% tested.*

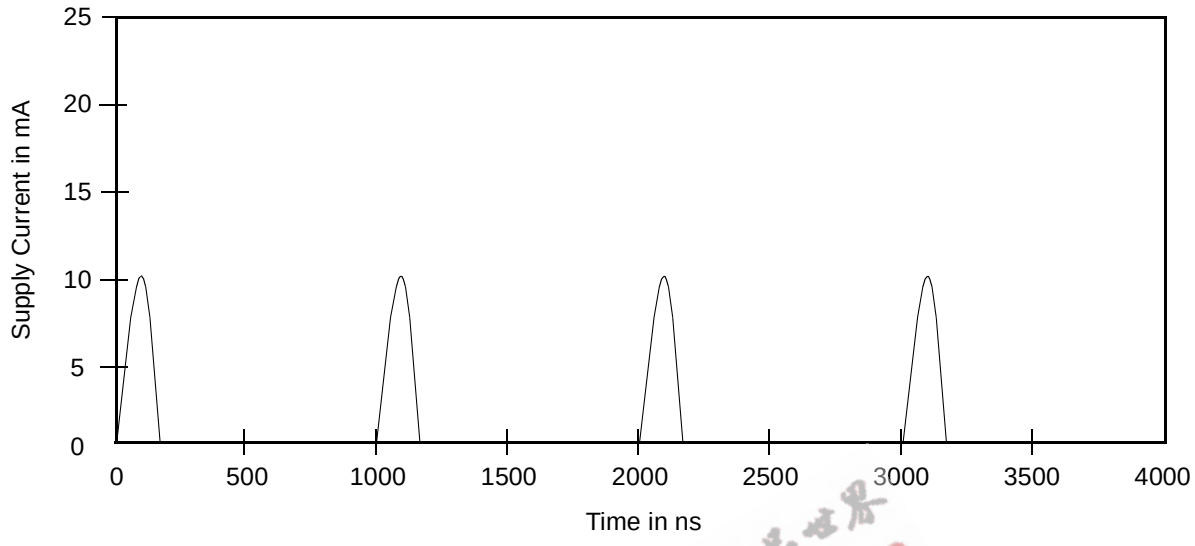
SRAM DC AND OPERATING CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}	–1.0		1.0	µA
I_{LO}	Output Leakage Current	CE1#s = V_{IH}, CE2s = V_{IL} or OE# = V_{IH} or WE# = V_{IL}, V_{IO}= V_{SS} to V_{CC}	–1.0		1.0	µA
I_{CC}	Operating Power Supply Current	I_{IO} = 0 mA, CE1#s = V_{IL}, CE2s = WE# = V_{IH}, V_{IN} = V_{IH} or V_{IL}			2	mA
$I_{CC1}s$	Average Operating Current	Cycle time = 1 µs, 100% duty, I_{IO} = 0 mA, CE1#s ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V			2	mA
$I_{CC2}s$	Average Operating Current	Cycle time = Min., I_{IO} = 0 mA, 100% duty, CE1#s = V_{IL}, CE2s = V_{IH}, V_{IN} = V_{IL} = or V_{IH}			17	mA
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA	1.4			V
I_{SB1}	Standby Current (CMOS)	CE1#s ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V (CE1#s controlled) or CE2 ≤ 0.2 V (CE2s controlled), CIOs = V_{SS} or V_{CC}, Other input = 0 ~ V_{CC}	0.5		8	µA

Note: *Typical values measured at V_{CC} = 2.0 V, T_A = 25°C. Not 100% tested.*

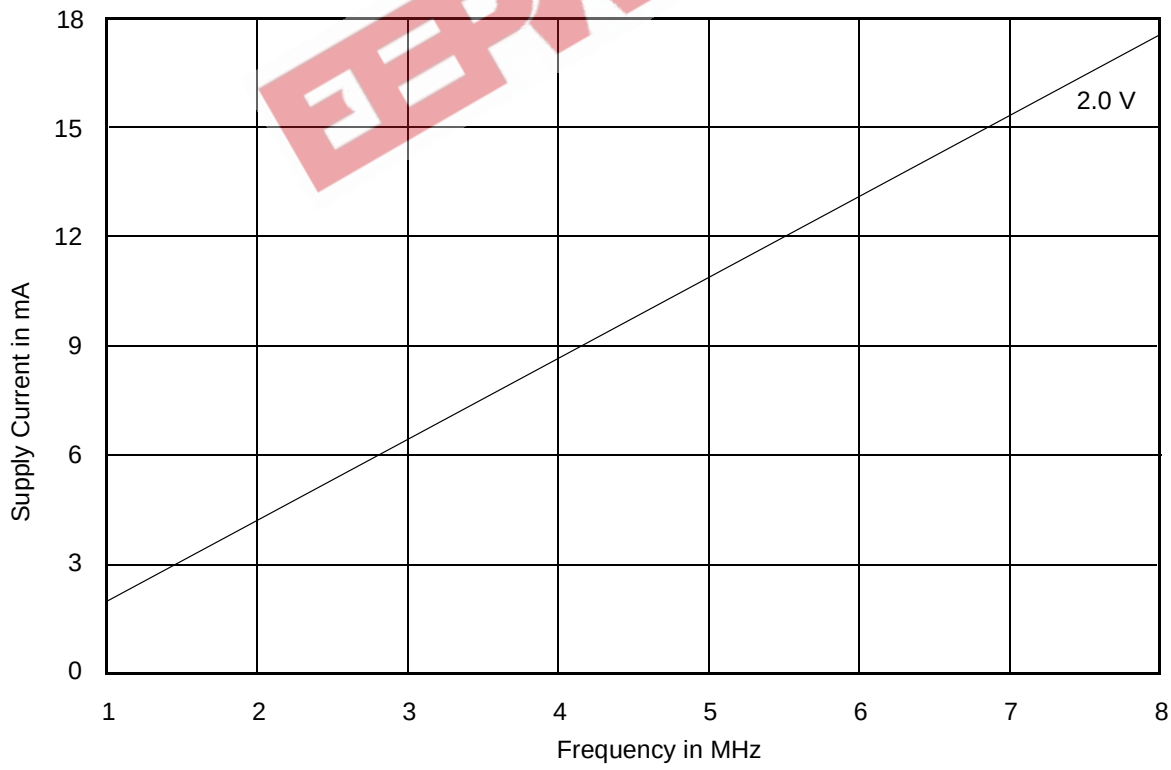
FLASH DC CHARACTERISTICS

Zero-Power Flash



Note: *Addresses are switching at 1 MHz*

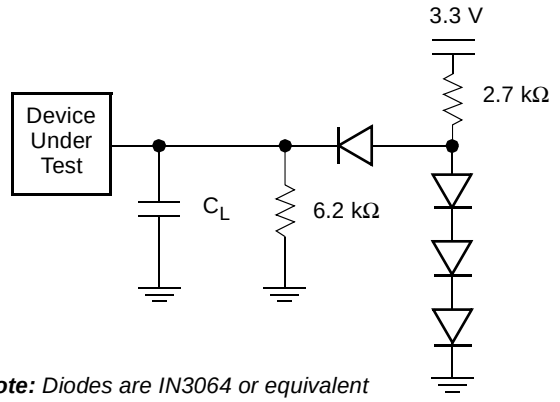
Figure 10. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: *T = 25 °C*

Figure 11. Typical I_{CC1} vs. Frequency

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

Figure 12. Test Setup

Table 12. Test Specifications

Test Condition	100, 110 ns	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	2.0	V
Input timing measurement reference levels	1.0	V
Output timing measurement reference levels	1.0	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

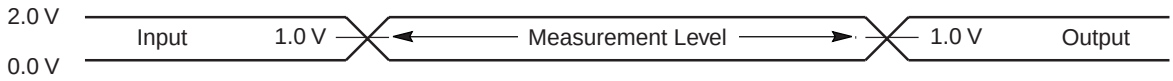


Figure 13. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

SRAM CE#s Timing

Parameter		Description	Test Setup		All Speeds	Unit
JEDEC	Std					
—	t_{CCR}	CE#s Recover Time	—	Min	0	ns

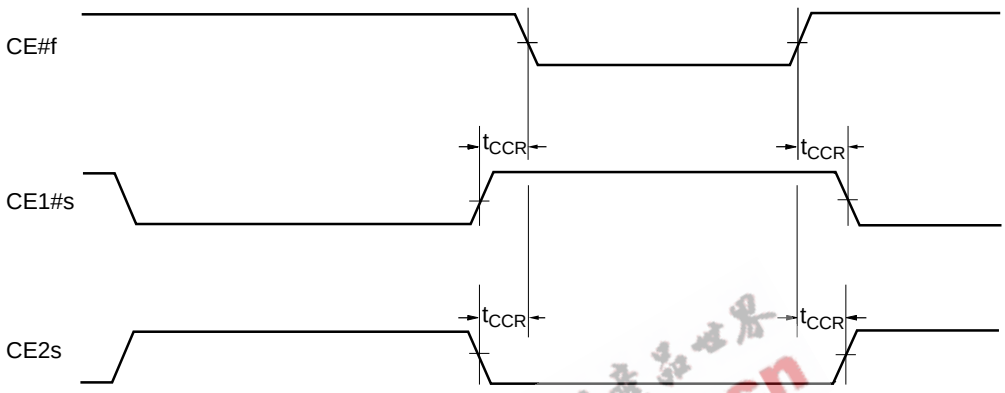


Figure 14. Timing Diagram for Alternating Between SRAM to Flash

FLASH AC CHARACTERISTICS

Read-Only Operations

Parameter		Description		Test Setup		Speed Option		Unit
JEDEC	Std					10	11	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	100	110	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	100	110	ns
	t_{PRC}	Page Read Cycle			Min	40	45	ns
	t_{PACC}	Page Address to Output Delay		CE#, OE# = V_{IL}	Max	40	45	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	100	110	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	35	45	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 1, 3)			Max	16		ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1, 3)			Max	16		ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0		ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0		ns
			Toggle and Data# Polling		Min	10		ns

Notes:

1. *Not 100% tested.*
2. *See Figure 12 and Table 12 for test specifications.*
3. *Measurements performed by placing a 50Ω termination on the data pin with a bias of $V_{CC}/2$. The time from OE# high to the data bus driven to $V_{CC}/2$ is taken as t_{DF} AC Characteristics.*

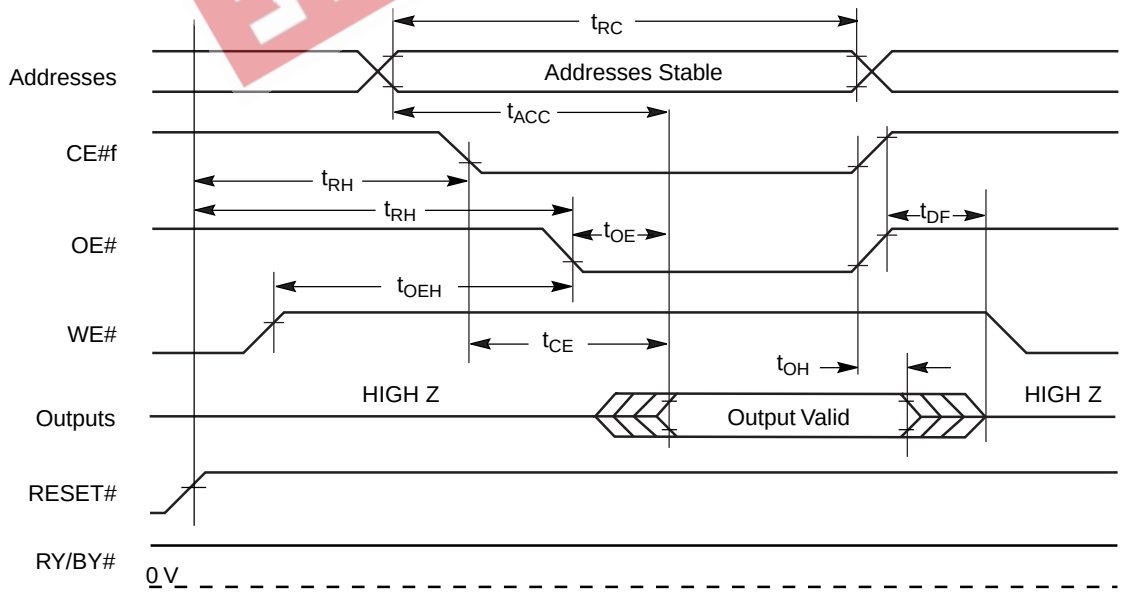


Figure 15. Conventional Read Operation Timings

FLASH AC CHARACTERISTICS

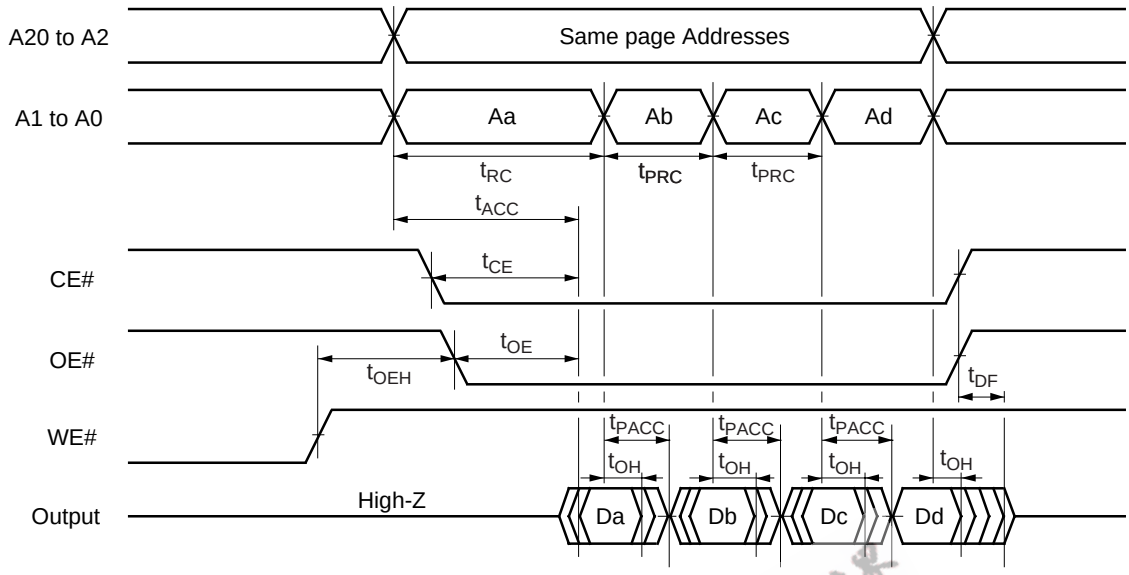


Figure 16. Page Mode Read Timings

FLASH AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speeds	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	200	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: *Not 100% tested.*

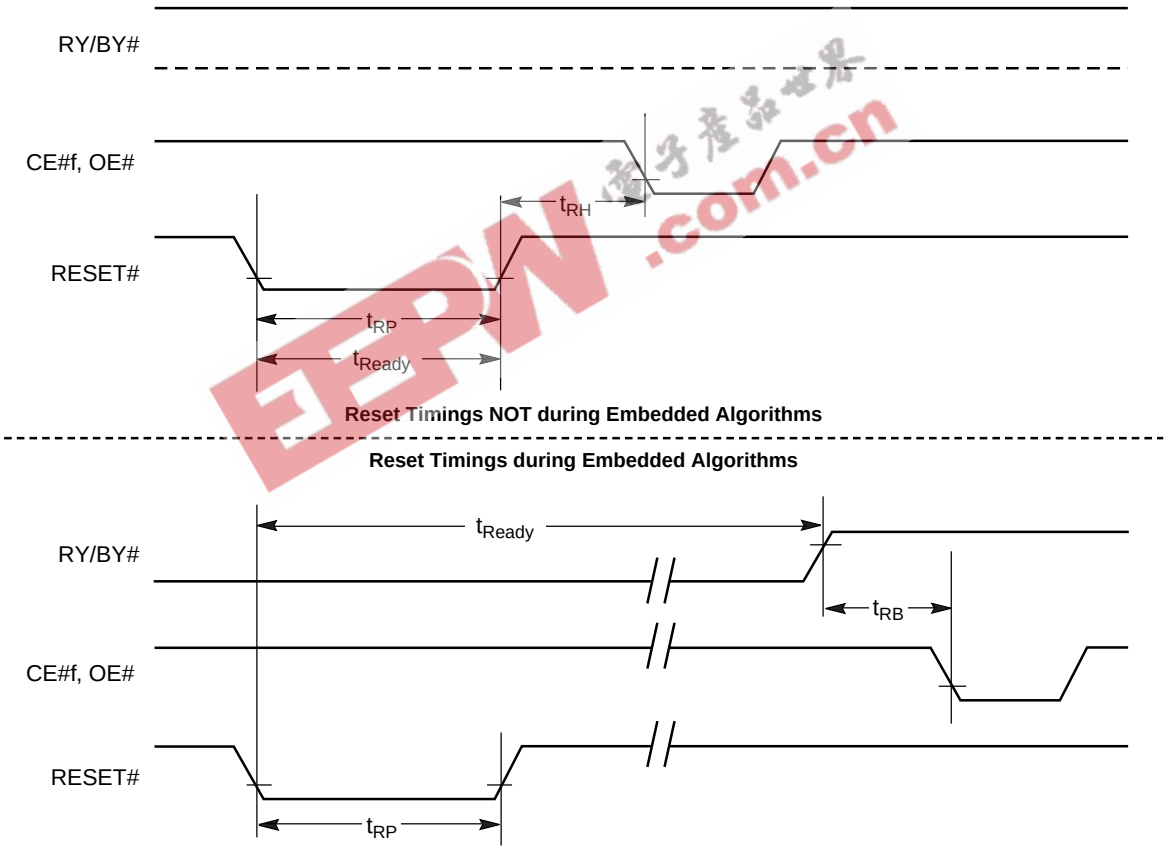


Figure 17. Reset Timings

FLASH AC CHARACTERISTICS

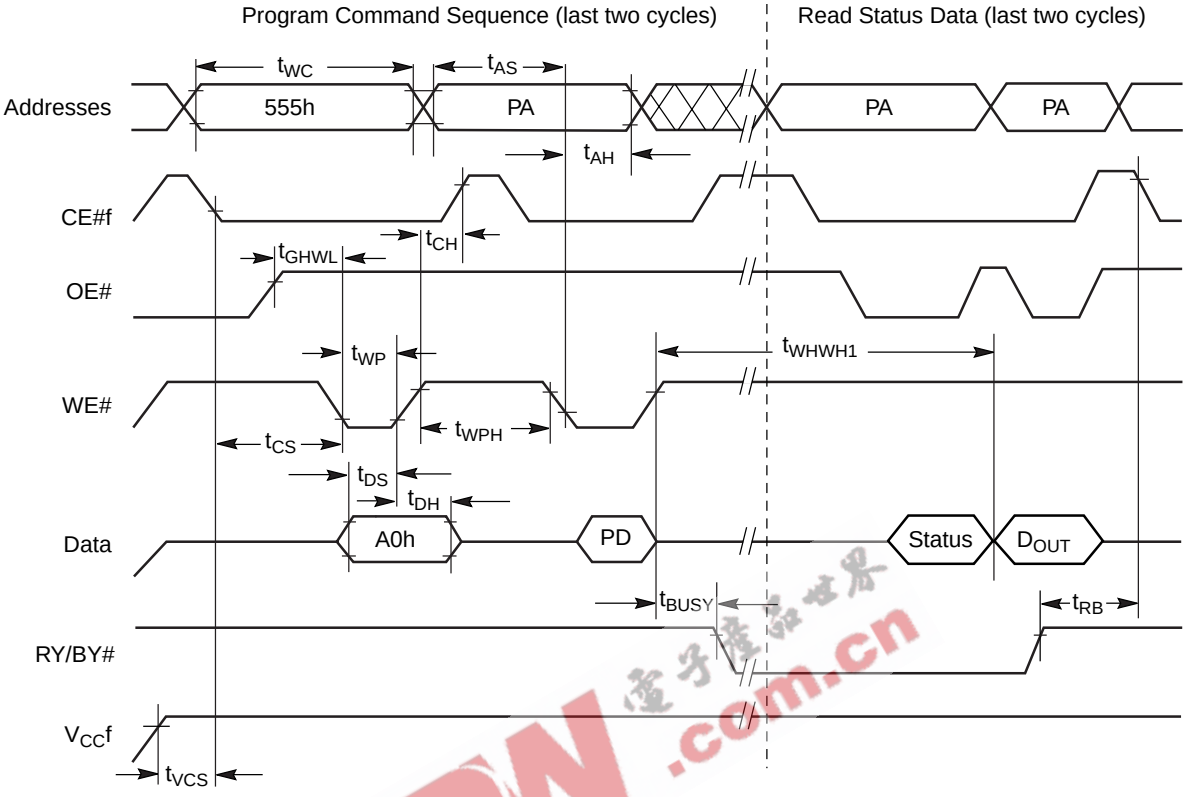
Flash Erase and Program Operations

Parameter		Description			Speed Options		Unit
JEDEC	Std				10	11	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	100	110	ns
t_{AVWL}	t_{AS}	Address Setup Time (WE# to Address)		Min	0		ns
	t_{ASO}	Address Setup Time to OE# or CE#f Low During Toggle Bit Polling		Min	15		ns
t_{WLAX}	t_{AH}	Address Hold Time (WE# to Address)		Min	60		ns
	t_{AHT}	Address Hold Time From CE#f or OE# High During Toggle Bit Polling		Min	0		ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	60		ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OEH}	OE# Hold Time	Read	Min	0		ns
			Toggle and Data# Polling	Min	20		ns
	t_{OEPH}	Output Enable High During Toggle Bit Polling		Min	20		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to CE#f Low)		Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time (CE#f to WE#)		Min	0		ns
t_{ELWL}	t_{CS}	CE#f Setup Time (WE# to CE#f)		Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time (CE#f to WE#)		Min	0		ns
t_{WHEH}	t_{CH}	CE#f Hold Time (CE#f to WE#)		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	60		ns
t_{ELEH}	t_{CP}	CE#f Pulse Width		Min	60		ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	60		ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)		Typ	11		µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte (Note 2)		Typ	5		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	1		sec
	t_{VCS}	V_{CC}f Setup Time (Note 1)		Min	50		µs
	t_{RB}	Write Recovery Time From RY/BY#		Min	0		ns
	t_{BUSY}	Program/Erase Valid To RY/BY# Delay		Max	90		ns

Notes:

1. *Not 100% tested.*
2. *See the "Flash Erase And Programming Performance" section for more information.*

FLASH AC CHARACTERISTICS



Notes:

1. PA = program address, PD = program data, D_{OUT} is the true data at the program address.

Figure 18. Program Operation Timings

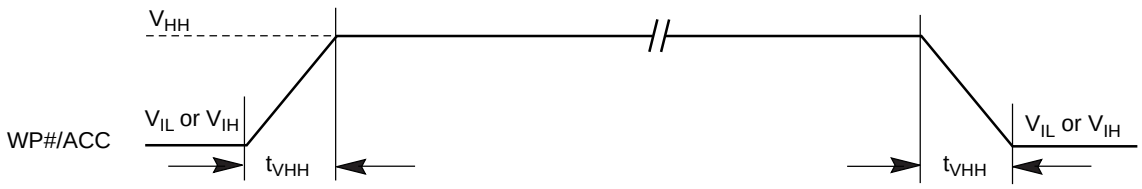
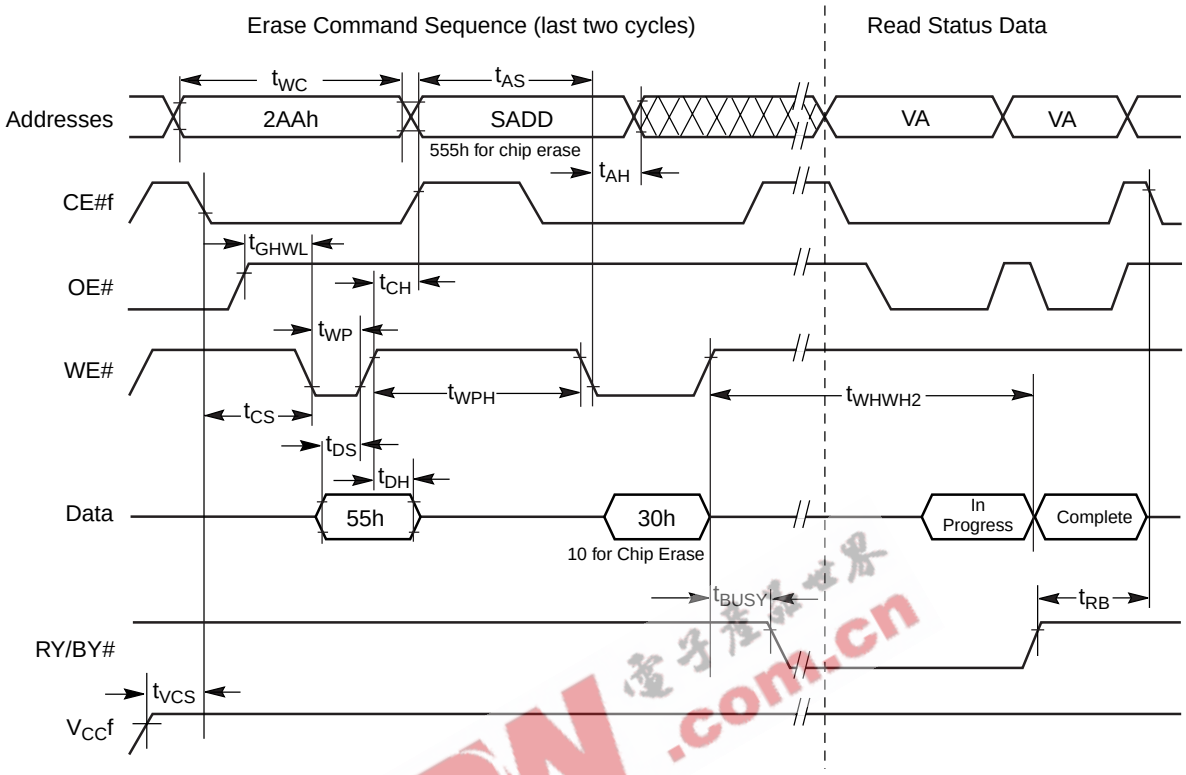


Figure 19. Accelerated Program Timing Diagram

FLASH AC CHARACTERISTICS



Notes:

1. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Flash Write Operation Status").

Figure 20. Chip/Sector Erase Operation Timings

FLASH AC CHARACTERISTICS

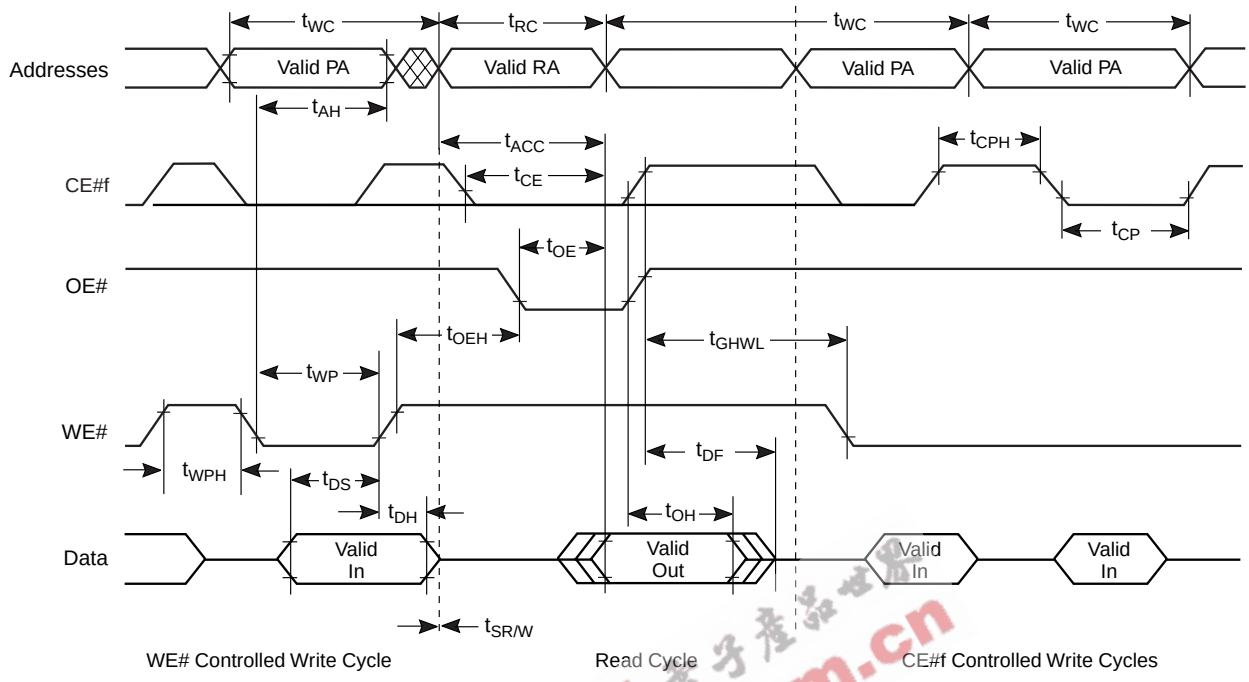
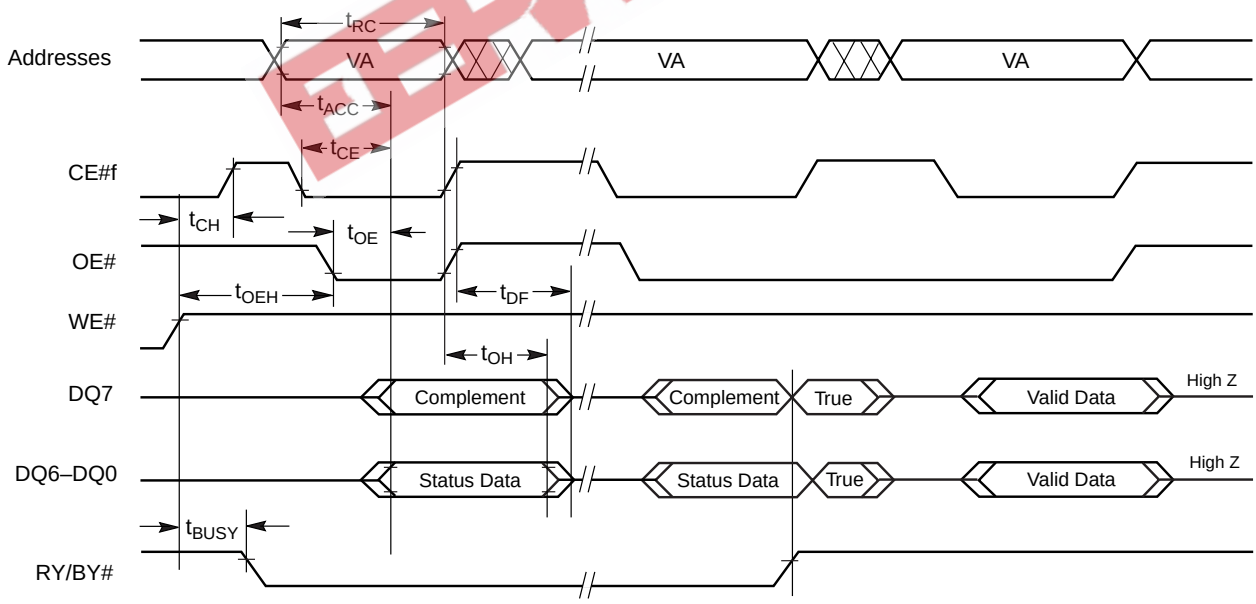


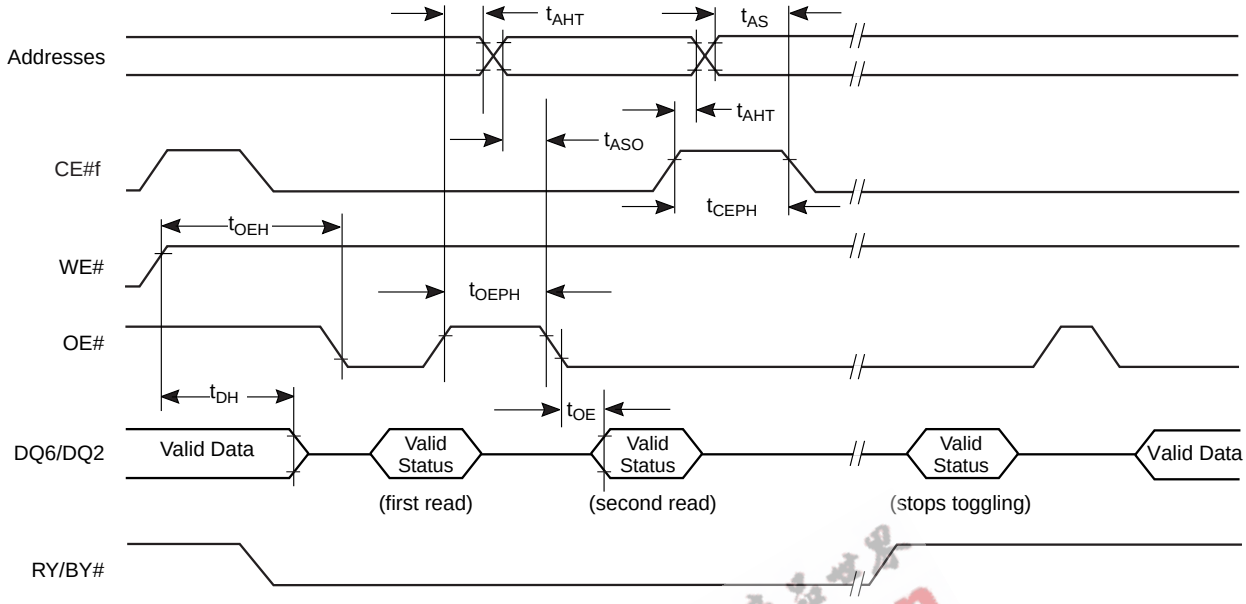
Figure 21. Back-to-back Read/Write Cycle Timings



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

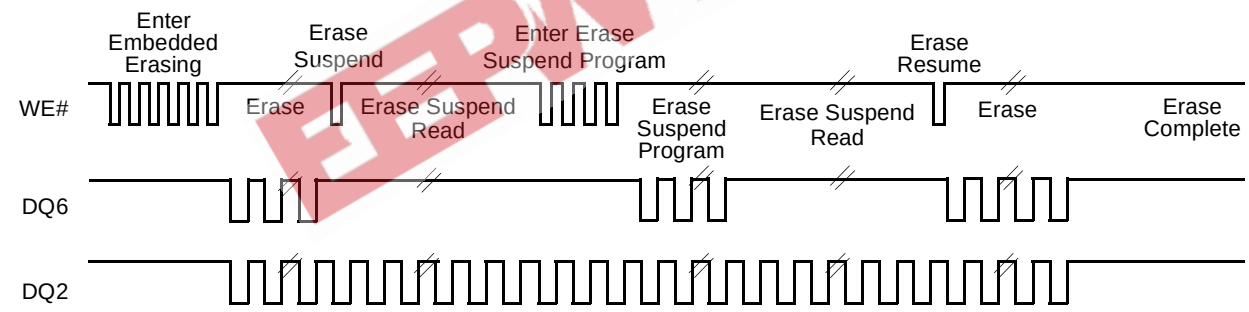
Figure 22. Data# Polling Timings (During Embedded Algorithms)

FLASH AC CHARACTERISTICS



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 23. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE#f to toggle DQ2 and DQ6.*

Figure 24. DQ2 vs. DQ6

FLASH AC CHARACTERISTICS

Temporary Sector/Sector Block Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector/Sector Block Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector/Sector Block Unprotect	Min	4	µs

Note: *Not 100% tested.*

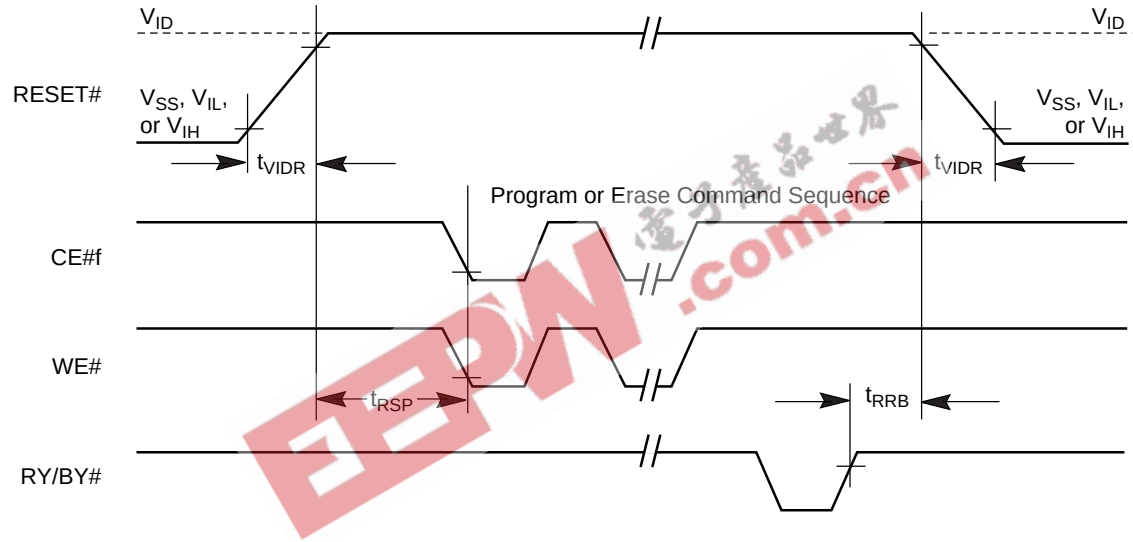
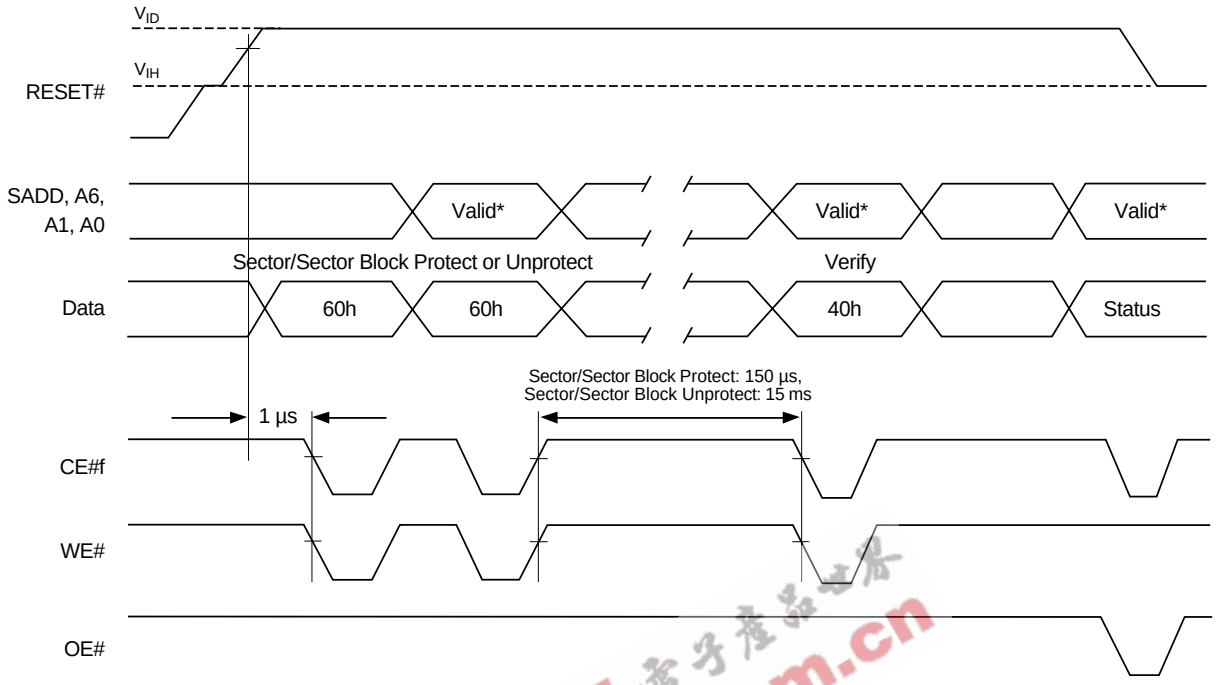


Figure 25. Temporary Sector/Sector Block Unprotect Timing Diagram

FLASH AC CHARACTERISTICS



* *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 26. Sector/Sector Block Protect and Unprotect Timing Diagram

FLASH AC CHARACTERISTICS

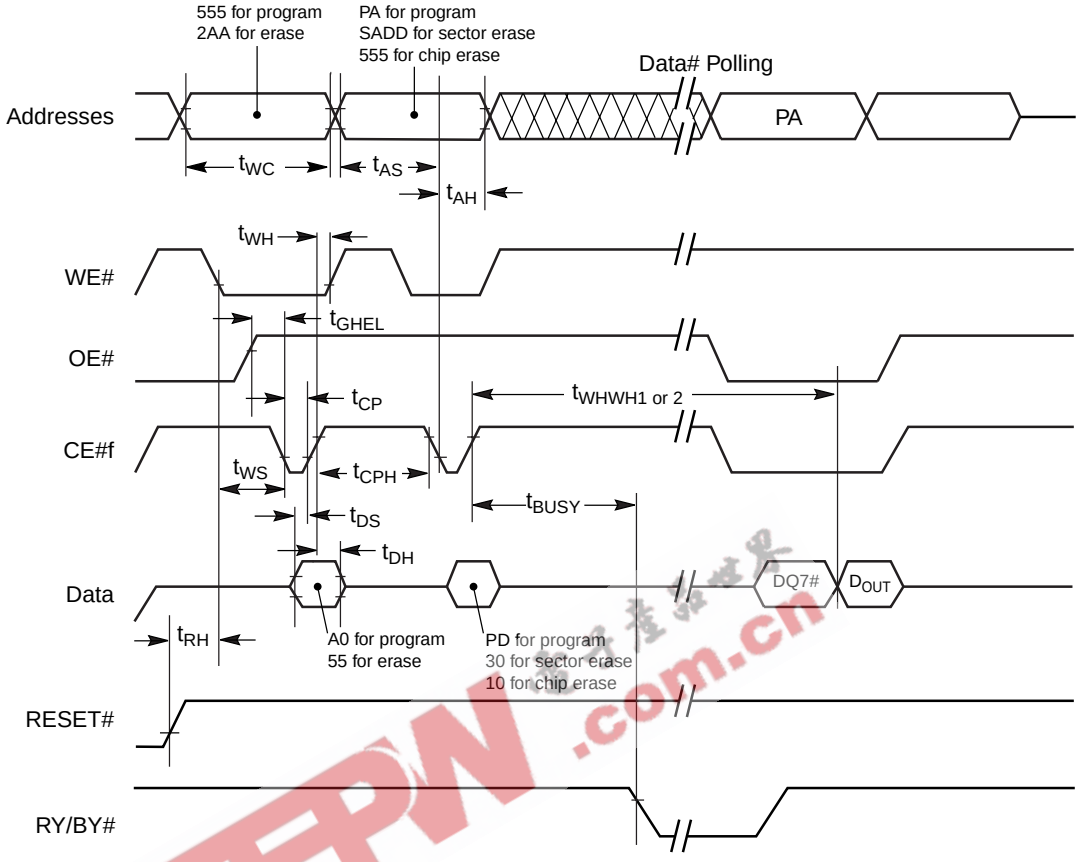
Alternate CE#f Controlled Erase and Program Operations

Parameter		Description		Speed Options		Unit
JEDEC	Std			10	11	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	100	110	ns
t_{AVWL}	t_{AS}	Address Setup Time (WE# to Address)	Min	0		ns
	t_{ASO}	Address Setup Time to CE#f Low During Toggle Bit Polling	Min	15		ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	60		ns
	t_{AHT}	Address Hold time from CE#f or OE# High During Toggle Bit Polling	Min	0		ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	60		ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0		ns
t_{ELEH}	t_{CP}	CE#f Pulse Width	Min	60		ns
t_{EHEL}	t_{CPH}	CE#f Pulse Width High	Min	60		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	16		µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte (Note 2)	Typ	5		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	1		sec

Notes:

1. *Not 100% tested.*
2. *See the "Flash Erase And Programming Performance" section for more information.*

FLASH AC CHARACTERISTICS



Notes:

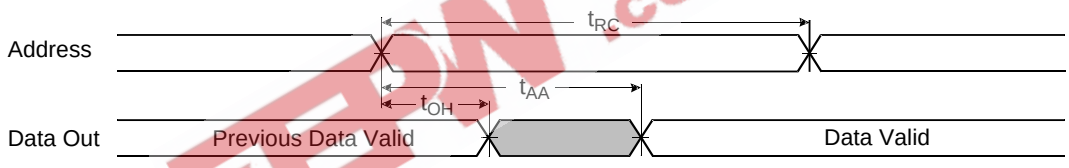
1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*

Figure 27. Flash Alternate CE#f Controlled Write (Erase/Program) Operation Timings

SRAM AC CHARACTERISTICS

Read Cycle

Parameter Symbol	Description		10, 11	Unit
t_{RC}	Read Cycle Time	Min	70	ns
t_{AA}	Address Access Time	Max	70	ns
t_{CO1}, t_{CO2}	Chip Enable to Output	Max	70	ns
t_{OE}	Output Enable Access Time	Max	35	ns
t_{BA}	LB#s, UB#s to Access Time	Max	70	ns
t_{LZ1}, t_{LZ2}	Chip Enable (CE1#s Low and CE2s High) to Low-Z Output	Min	10	ns
t_{BLZ}	UB#, LB# Enable to Low-Z Output	Min	10	ns
t_{OLZ}	Output Enable to Low-Z Output	Min	5	ns
t_{HZ1}, t_{HZ2}	Chip Disable to High-Z Output	Max	25	ns
t_{BHZ}	UB#s, LB#s Disable to High-Z Output	Max	25	ns
t_{OHZ}	Output Disable to High-Z Output	Max	25	ns
t_{OH}	Output Data Hold from Address Change	Min	10	ns



Note: *CE1#s = OE# = V_{IL}, CE2s = WE# = V_{IH}, UB#s and/or LB#s = V_{IL}*

Figure 28. SRAM Read Cycle—Address Controlled

SRAM AC CHARACTERISTICS

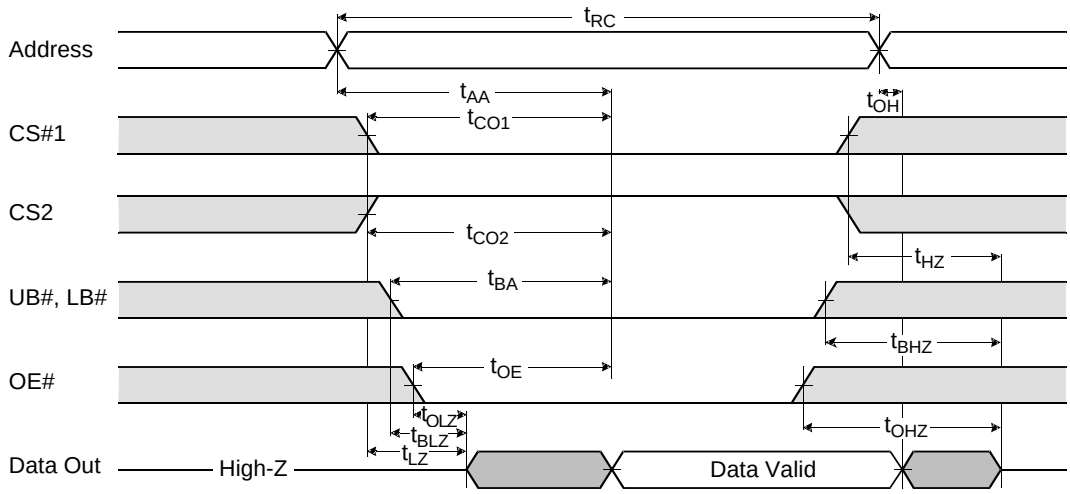


Figure 29. SRAM Read Cycle

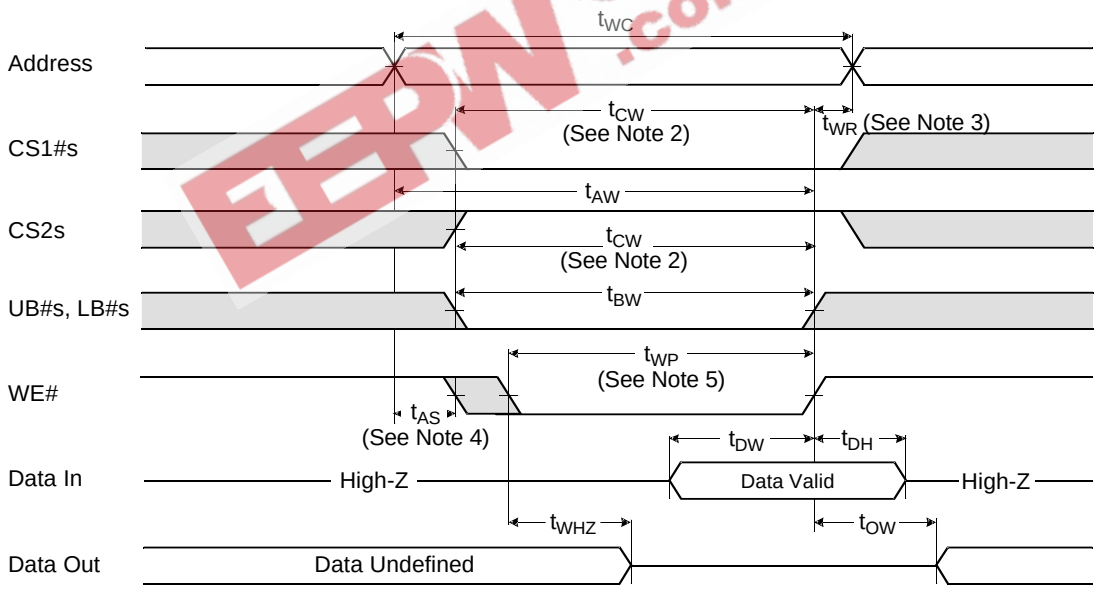
Notes:

1. *WE# = V_{IH}, if CIOs is low, ignore UB#s/LB#s timing.*
2. *t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.*
3. *At any given temperature and voltage condition, t_{HZ} (Max.) is less than t_{LZ} (Min.) both for a given device and from device to device interconnection.*

SRAM AC CHARACTERISTICS

Write Cycle

Parameter Symbol	Description		10, 11	Unit
t_{WC}	Write Cycle Time	Min	70	ns
t_{Cw}	Chip Enable to End of Write	Min	60	ns
t_{AS}	Address Setup Time	Min	0	ns
t_{AW}	Address Valid to End of Write	Min	60	ns
t_{BW}	UB#s, LB#s to End of Write	Min	60	ns
t_{WP}	Write Pulse Time	Min	50	ns
t_{WR}	Write Recovery Time	Min	0	ns
t_{WHZ}	Write to Output High-Z	Min	0	ns
		Max	20	
t_{DW}	Data to Write Time Overlap	Min	30	ns
t_{DH}	Data Hold from Write Time	Min	0	ns
t_{OW}	End Write to Output Low-Z	min	5	ns

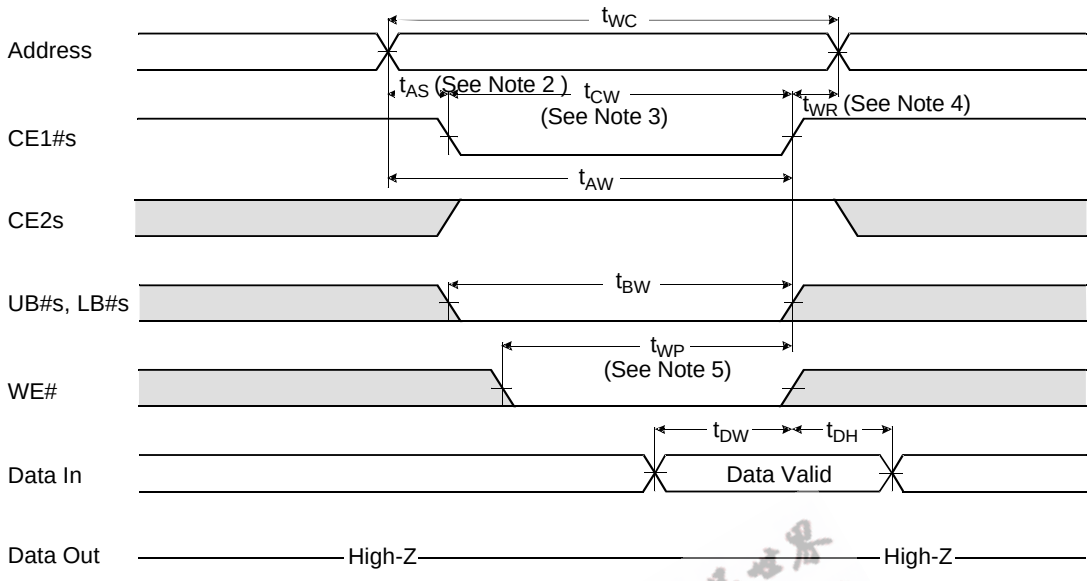


Notes:

1. *WE# controlled, if CIOs is low, ignore UB#s and LB#s timing.*
2. *t_{CW} is measured from CE1#s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE1#s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1 and low WE#. A write begins when CE1#s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE1#s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 30. SRAM Write Cycle—WE# Control

SRAM AC CHARACTERISTICS

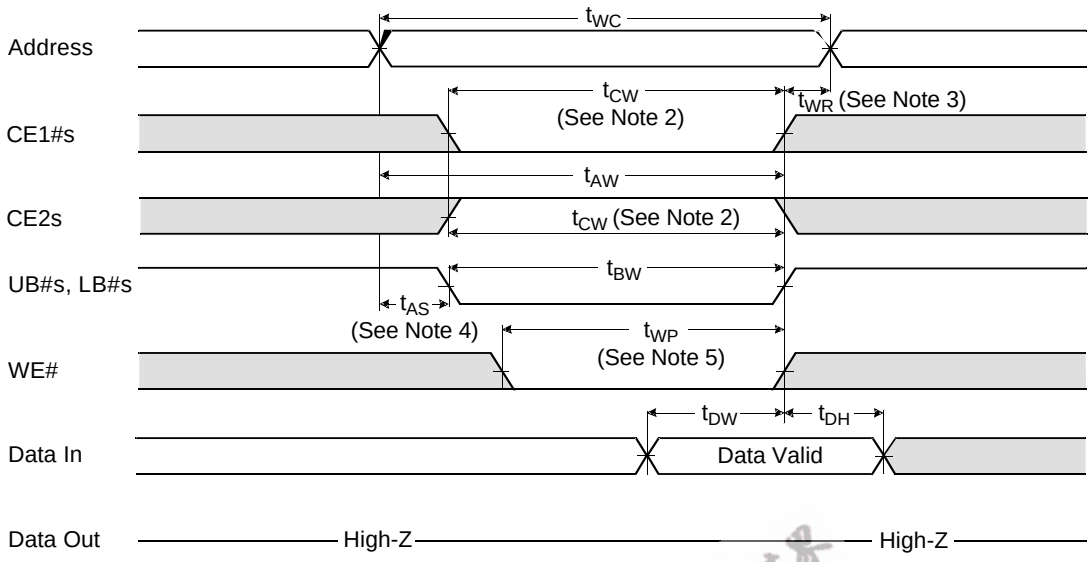


Notes:

1. *CE1#s controlled, if CIOs is low, ignore UB#s and LB#s timing.*
2. *t_{CW} is measured from CE1#s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE1#s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1 and low WE#. A write begins when CE1#s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE1#s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 31. SRAM Write Cycle—CE1#s Control

SRAM AC CHARACTERISTICS



Notes:

1. *UB#s and LB#s controlled, CIOs must be high.*
2. *t_{CW} is measured from CE1#s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE1#s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1 and low WE#. A write begins when CE1#s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE1#s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 32. SRAM Write Cycle—UB#s and LB#s Control

FLASH ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		1	10	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		93		sec	
Word Program Time		16	360	µs	Excludes system level overhead (Note 5)
Accelerated Byte/Word Program Time		5		µs	
Chip Program Time (Note 3)	Word Mode	20	100		

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 2.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.8 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 10 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 1,000,000 cycles.*

FLASH LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.*

PACKAGE PIN CAPACITANCE

Parameter Symbol	Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	11	14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	12	16	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	14	16	pF
C_{IN3}	WP#/ACC Pin Capacitance	V_{IN} = 0	17	20	pF

Note: *7.Test conditions T_A = 25°C, f = 1.0 MHz.*

FLASH DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

SRAM DATA RETENTION

Parameter Symbol	Parameter Description	Test Setup	Min	Typ	Max	Unit
V_{DR}	V_{CC} for Data Retention	CS1#s ≥ V_{CC} – 0.2 V (Note 1)	1.0		2.2	V
I_{DR}	Data Retention Current	V_{CC} = 3.0 V, CE1#s ≥ V_{CC} – 0.2 V (Note 1)		0.5 (Note 2)	3	µA
t_{SDR}	Data Retention Set-Up Time	See data retention waveforms	0			ns
t_{RDR}	Recovery Time		t_{RC}			ns

Notes:

1. *CE1#s ≥ V_{CC} – 0.2 V, CE2s ≥ V_{CC} – 0.2 V (CE1#s controlled) or CE2s ≤ 0.2 V (CE2s controlled), CIOs = V_{SS} or V_{CC}.*
2. *Typical values are not 100% tested.*

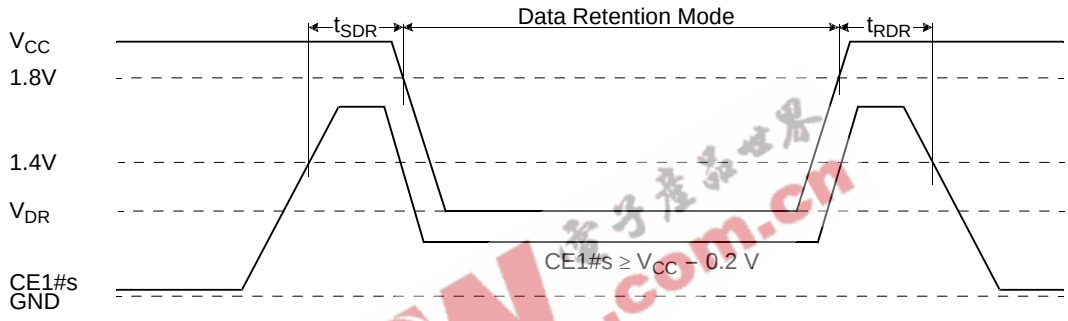


Figure 33. CE1#s Controlled Data Retention Mode

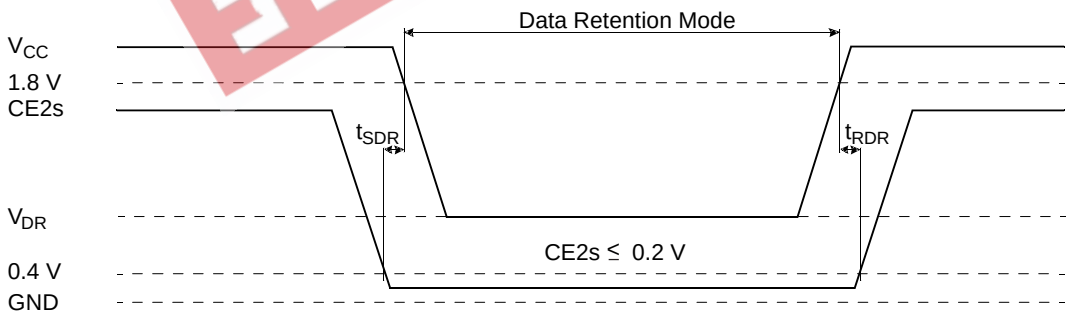
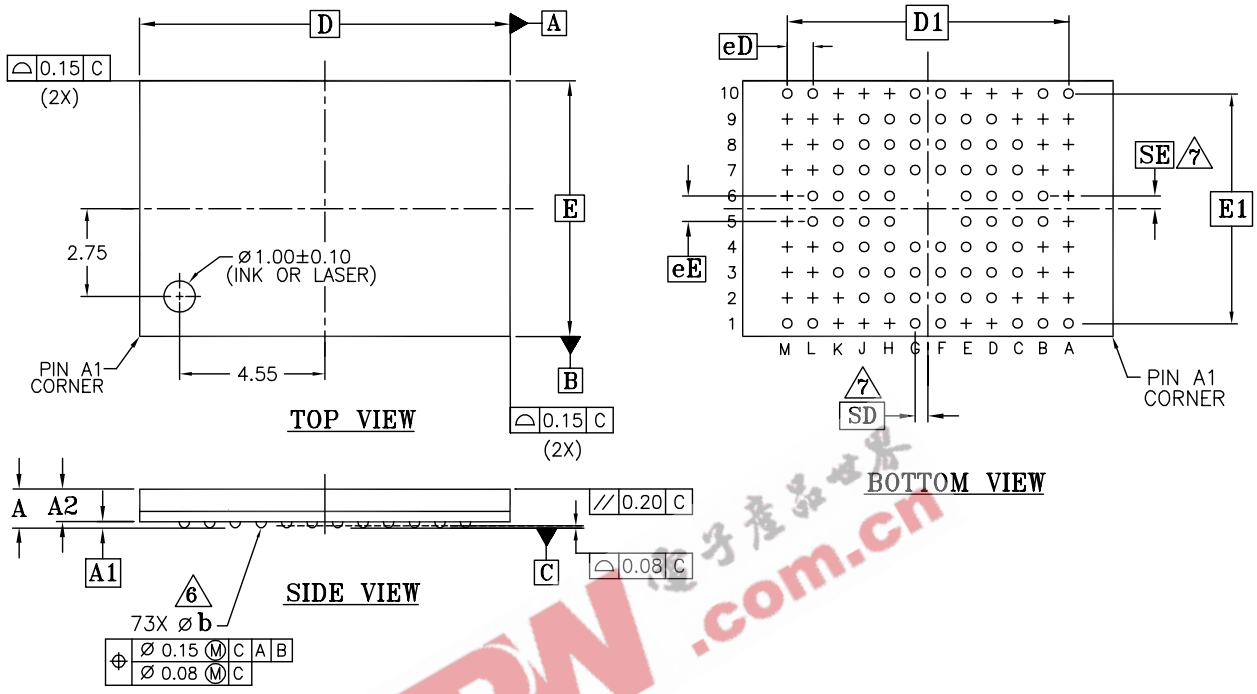


Figure 34. CE2s Controlled Data Retention Mode

PHYSICAL DIMENSIONS

FLB073—73-Ball Fine-Pitch Grid Array 8 x 11.6 mm



PACKAGE	FLB 073			NOTE
JEDEC	N/A			
	8.00mm X 11.60mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	–	–	1.40	PROFILE
A1	0.20	–	0.30	BALL HEIGHT
A2	0.95	–	1.09	BODY THICKNESS
D	11.60 BSC			BODY SIZE
E	8.00 BSC			BODY SIZE
D1	8.80 BSC			MATRIX FOOTPRINT
E1	7.20 BSC			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	73			BALL COUNT
ø b	0.25	0.30	0.35	BALL DIAMETER
eE	0.80 BSC			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD/SE	0.40 BSC			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9,B2,B3,B4,B7,B8,B9 C10,D1,D10,E1,E10,F5,F6,G5,G6,H1,H10 J1,J10,K1,K10,L2,L3,L4,L7,L8,L9, M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

REVISION SUMMARY

Revision A (February 18, 2002)

Initial release.

Revision A+1 (May 13, 2002)

Distinctive Characteristics

Modified text in “High Performance” bullet. Deleted reference to 48-ball FBGA package.

Figure 30, SRAM Write Cycle—WE# Control

Corrected t_{BW} in Data Out waveform to t_{WHZ}.