PRELIMINARY

AM

Am79C873

NetPHY™ -1
10/100 Mbps Ethernet Physical Layer Single-Chip Transceiver with 100BASE-FX

DISTINCTIVE CHARACTERISTICS

- **100BASE-FX direct interface to industry standard electrical/optical transceivers**
- **10/100BASE-TX physical-layer, single-chip transceiver**
- **Compliant with the IEEE 802.3u 100BASE-TX standard**
- **Compliant with the ANSI X3T12 TP-PMD 1995 standard**
- **Compliant with the IEEE 802.3u Auto-Negotiation protocol for automatic link type selection**
- **Supports the MII with serial management interface**
- **Supports Full Duplex operation for 10 Mbps and 100 Mbps**
- **High performance 100 Mbps clock g and data recovery circuitry**
- **Adaptive equalization circuitry for 10 receiver**
- **Controlled output edge rates in 100 I**
- **Supports a 10BASE-T interface witho need for an external filter**
- **Provides Loopback mode for system diagnostics**
- **Includes flexible LED configuration c**
- **Digital clock recovery circuit using a digital algorithm to reduce jitter**
- **Low-power, high-performance CMOS**
- **Available in a 100-pin PQFP packag**

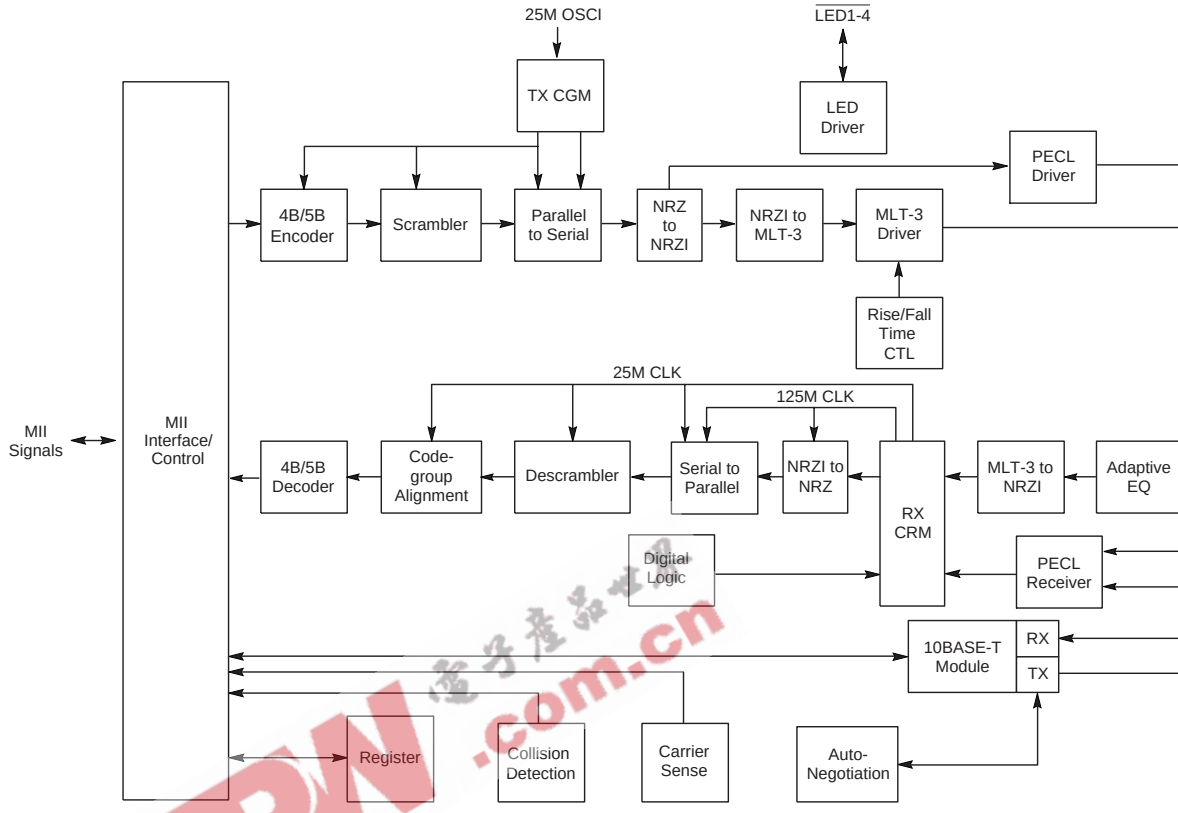
GENERAL DESCRIPTION

The NetPHY-1 device is a physical-layer, single-chip, low-power transceiver for 100BASE-TX, 100BASE-FX, and 10BASE-T operations. On the media side, it provides a direct interface to Fiber Media for 100BASE-FX Fast Ethernet, Unshielded Twisted Pair Category 5 Cable (UTP5) for 100BASE-TX Fast Ethernet, or UTP5/UTP3 Cable for 10BASE-T Ethernet. Through the IEEE 802.3u Media Independent Interface (MII), the NetPHY-1 device connects to the Medium Access Control (MAC) layer, ensuring a high interoperability among products from different vendors.

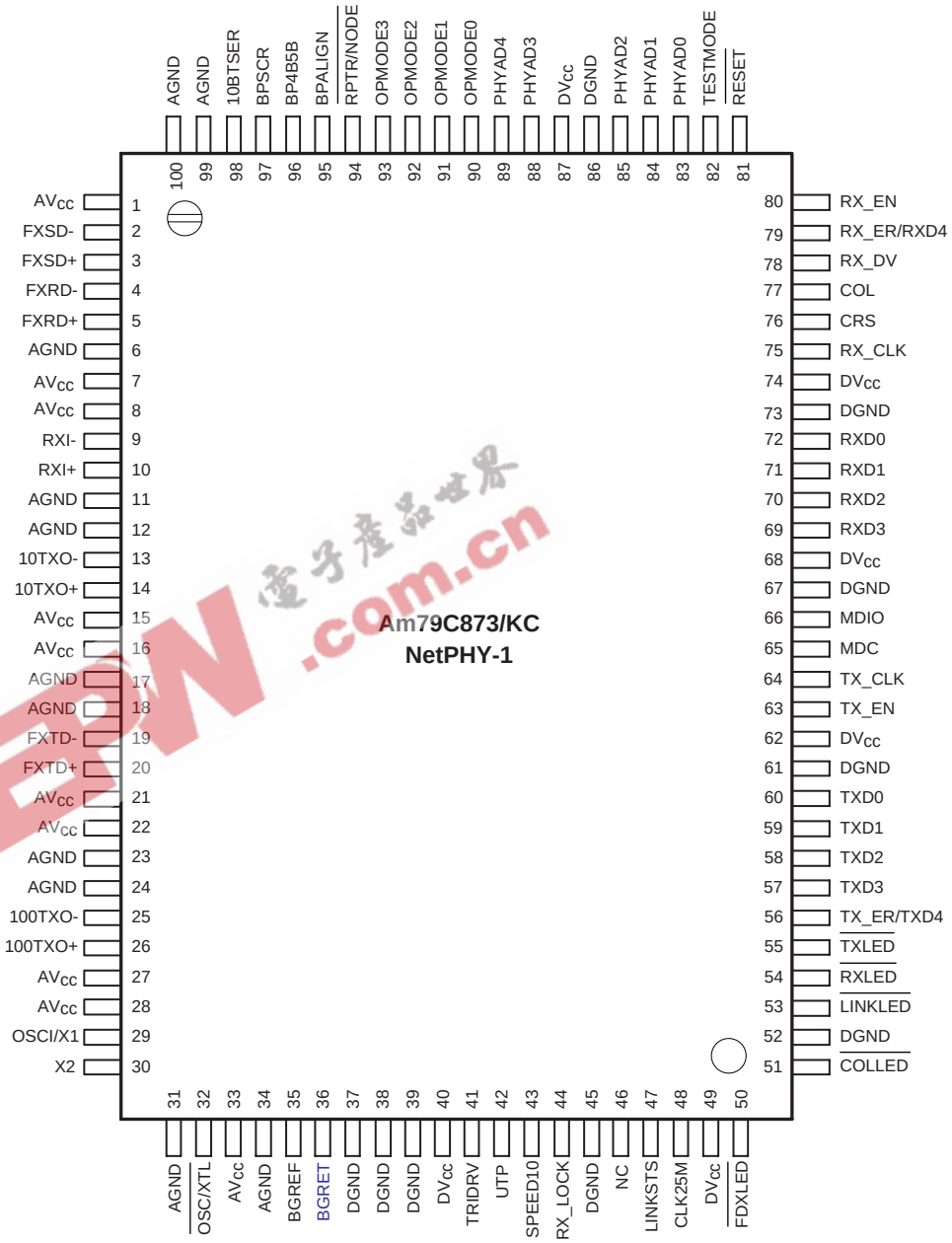
The NetPHY-1 device uses a low-power, high-performance CMOS process. It contains the entire physical layer functions of 100BASE-FX and 100B defined by the IEEE 802.3u standard, in Physical Coding Sublayer (PCS), Physic Attachment (PMA), 100BASE-TX Twisted P Medium Dependent (TP-PMD) subla 10BASE-T Encoder/Decoder (ENDEC). Th device provides strong support for the Auto function utilizing automatic media speed a selection. The NetPHY-1 device incorporat nal wave-shaping filter to control rise/fall tim ing the need for external filtering on Mbps signals.

Publication# **22164** Rev: **A**
Issue Date: **February 1999**

BLOCK DIAGRAM



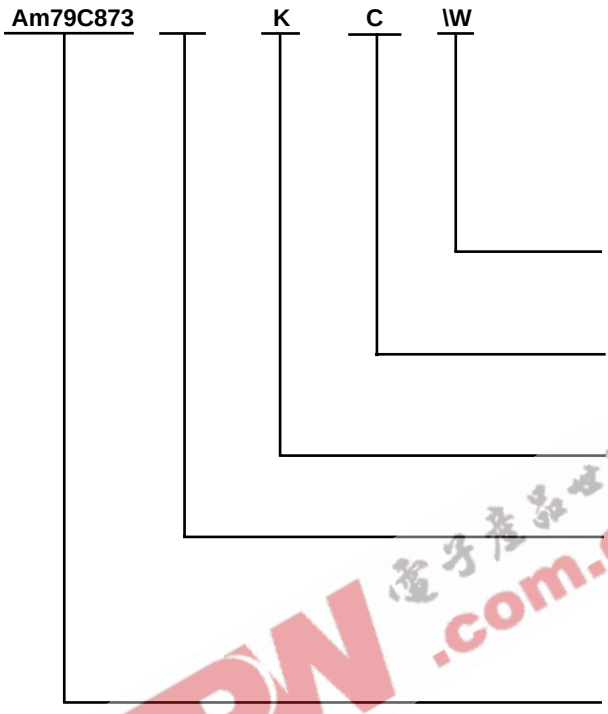
CONNECTION DIAGRAM



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combinat
by a combination of the elements below.



ALTERNATE PACKAGING OPTION
\W = Trimmed and formed in a tray

TEMPERATURE RANGE
C = Commercial (0˚C to +70˚C)

PACKAGE TYPE
K = Plastic Quad Flat Pack (PQR100)

SPEED OPTION
Not Applicable

DEVICE NUMBER/DESCRIPTION
Am79C873
NetPHY-1™ 10/100 Mbps Ethernet Physical
Single-Chip Transceiver with 100BASE-FX Suppo

Valid Combinations

Valid Combinations list configurations planne
ported in volume for this device. Consult the loc
office to confirm availability of specific valid com
to check on newly released combinations.

Valid Combinations	
Am79C873	KC\W

RELATED AMD PRODUCTS

Part No.	Description
Controllers	
Am79C90	CMOS Local Area Network Controller for Ethernet (C-LANCE™)
Integrated Controllers	
Am79C930	PCnet™-Mobile Single Chip Wireless LAN Media Access Controller
Am79C940	Media Access Controller for Ethernet (MACE™)
Am79C961A	PCnet-ISA II Full Duplex Single-Chip Ethernet Controller for ISA Bus
Am79C965A	PCnet-32 Single-Chip 32-Bit Ethernet Controller for 486 and VL Buses
Am79C970A	PCnet-PCI II Full Duplex Single-Chip Ethernet Controller for PCI Local Bus
Am79C971	PCnet-FAST Single-Chip Full Duplex 10/100 Mbps Ethernet Controller for PCI Local Bus
Am79C972	PCnet-FAST+ Enhanced 10/100 Mbps PCI Ethernet Controller with OnNow Support
Am79C973/ Am79C975	PCnet-Fast III Single-chip 10/100 Mbps PCI Ethernet Controller With Integrated PHY
Am79C978	PCnet-Home Single-chip 1/10 Mbps PCI Home networking Controller
Physical Layer Devices (Single-Port)	
Am7996	IEEE 802.3/Ethernet/Cheapernet Transceiver
Am79761	Physical Layer 10-Bit Transceiver for Gigabit Ethernet (GigaPHY™-SD)
Am79C98	Twisted Pair Ethernet Transceiver (TPEX)
Am79C100	Twisted Pair Ethernet Transceiver Plus (TPEX+)
Physical Layer Devices (Multi-Port)	
Am79C871	Quad Fast Ethernet Transceiver for 100BASE-X Repeaters (QFEXr™)
Am79C988A	Quad Integrated Ethernet Transceiver (QuIET™)
Am79C989	Quad Ethernet Switching Transceiver (QuEST™)
Integrated Repeater/Hub Devices	
Am79C981	Integrated Multiport Repeater Plus (IMR+)
Am79C982	Basic Integrated Multiport Repeater (bIMR)
Am79C983	Integrated Multiport Repeater 2 (IMR2™)
Am79C984A	Enhanced Integrated Multiport Repeater (eIMR™)
Am79C985	Enhanced Integrated Multiport Repeater Plus (eIMR+™)
Am79C987	Hardware Implemented Management Information Base (HIMIB™)

CONTENTS

PIN DESCRIPTIONS

MII Interface

TX_ER/TXD4

Transmit Error **Input**

In 100 Mbps mode, if this signal is asserted high and TX_EN is active, the HALT symbol is substituted for the actual data nibble. In 10 Mbps mode, this input is ignored.

In bypass modes (BP4B5B or BPALIGN), TX_ER becomes the TXD4 pin, the fifth TXD data bit.

TXD[3:0]

Transmit Data **Input**

These are the transmit data input pins for nibble data from the MII in 100 Mbps or 10 Mbps nibble mode (25 MHz for 100 Mbps mode, 2.5 MHz for 10 Mbps nibble mode).

In 10 Mbps serial mode, the TXD0 pin is used as the serial data input pin. TXD[3:1] are ignored.

TX_EN

Transmit Enable **Input**

Active high input indicates the presence of valid nibble data on TXD[3:0] for both 100 Mbps or 10 Mbps nibble mode.

In 10 Mbps serial mode, active high indicates the presence of valid 10 Mbps data on TXD0.

TX_CLK

Transmit Clock **Output/Z[1]**

This pin provides the transmit clock output from the NetPHY-1 deviceas follows:

- 25 MHz nibble transmit clock derived from transmit Phase Locked Loop (TX PLL) in 100BASE-TX mode
- 2.5 MHz transmit clock in 10BASE-T nibble mode
- 10 MHz transmit clock in 10BASE-T serial mode

MDC

Management Data Clock **Input**

This pin is the synchronous clock to the MDIO management data input/output serial interface which is asynchronous to transmit and receive clocks. The maximum clock rate is 2.5 MHz.

MDIO

Management Data I/O **Input/Output**

This pin is the bidirectional management instruction/data signal that may be driven by the station management entity or the PHY. This pin requires a 1.5 KΩ pull-up resistor.

1. Goes to high impedance.

RXD[3:0]

Receive Data

Nibble wide receive data (synchronous to R
MHz for 100BASE-TX mode, 2.5 MHz for
nibble mode). Data is driven on the falli
RX_CLK.

In 10 Mbps serial mode, the RXD0 pin is
data output pin. RXD[3:1] are ignored.

RX_CLK

Receive Clock

Provides the recovered receive clock f
modes of operation:

- 25 MHz nibble clock in 100 Mbps mo
- 2.5 MHz nibble clock in 10 Mbps nibb
- 10 MHz receive clock in 10 Mbps ser

CRS

Carrier Sense

This pin is asserted high to indicate the
carrier due to receive or transmit activities
T or 100BASE-TX Half Duplex modes.

In Repeater, when Full Duplex or Loopbac
logic 1, it indicates the presence of carrier
receive activity.

COL

Collision Detect

This pin is asserted high to indicate detec
sion conditions in 10 Mbps and 100 Mbps
modes. In 10BASE-T Half Duplex mode wit
set active (bit 13, register 18h), it is also as
duration of approximately 1ms at the end
sion to indicate heartbeat. In Full Duplex
signal is always logic 0. There is no heartb
in Full Duplex mode.

RX_DV

Receive Data Valid

This pin is asserted high to indicate that v
present on RXD[3:0].

RX_ER/RXD4

Receive Error

This pin is asserted high to indicate that an
bol has been detected inside a received pa
Mbps mode.

In a bypass mode (BP4B5B or BPALIG
RX_ER becomes RXD4, the fifth RXD da
5B symbols.

RX_EN

Receive Enable **Input**

This pin is active high enabled for receive signals RXD[3:0], RX_CLK, RX_DV and RX_ER. A low on this input tri-states these output pins. For normal operation in a NODE application, this pin should be pulled high.

Media Interface

RXI±

100/10 Mbps-TX/T Twisted Pair Differential Input Pair **Input**

These pins are the differential receive input for 10BASE-T and 100BASE-TX. They are capable of receiving 100BASE-TX MLT-3 or 10BASE-T Manchester encoded data.

FXRD±

100BASE-FX PECL Differential Input Pair **Input**

These pins are the differential receive input for 100BASE-FX. They are capable of receiving 100BASE-FX.

FXSD±

100BASE-FX PECL Signal Detect **Input**

These input signals from the FX-PMD transceiver indicate detection of a receive signal from the Fiber Media.

10TXO±

10BASE-T Differential Output Pair **Output**

This output pair provides controlled rise and fall times designed to filter the transmitters output.

100TXO±

100BASE-TX Twisted Pair Differential Output Pair **Output**

This output pair drives MLT-3 encoded data to the 100 M twisted pair cable and provides controlled rise and fall times designed to filter the transmitters output, reducing any associated EMI.

FXTD±

100BASE-FX PECL Differential Output PairOutput

These pins are the differential transmit output for 100BASE-FX. They are capable of transmitting 100BASE-FX

LED Interface

These outputs can directly drive LEDs or provide status information to a network management device.

$\overline{\text{FDXLED}}$ (POLLED)

Polarity/Full Duplex LED **Output**

This pin indicates Full Duplex mode status for 100 Mbps and 10 Mbps operation (Active low). If bit 4 of Register 16 (FDXLED_MODE) is set, the $\overline{\text{FDXLED}}$ pin function will change to indicate the Polarity Mbps operation. If polarity is inverted, the F go ON.

$\overline{\text{COLLED}}$

Collision LED

This pin indicates the presence of collision 10 Mbps and 100 Mbps operation. This meaning for 10 Mbps or 100 Mbps Full Du tion (Active low).

$\overline{\text{LINKLED}}$ (TRAFFIC LED)

Link LED

This pin indicates Good Link status for 1 100 Mbps operation (Active low). It funct TRAFFIC LED when bit 5 of register 16 is TRAFFIC LED mode, it is always ON whe OK. The TRAFFIC LED flashes when tra receiving.

$\overline{\text{RXLED}}$

Receive LED **Outp**

This pin indicates the presence of receive a Mbps and 100 Mbps operation (Active low PHY-1 device incorporates a “monostable” the RXLED output. This ensures that even ceive activity will generate an adequate LE

$\overline{\text{TXLED}}$

Transmit LED **Outp**

This pin indicates the presence of transmit a Mbps and 100 Mbps operation (Active low PHY-1 device incorporates a “monostable” the TXLED output. This ensures that ev transmit activity will generate an adequate L

Device Configuration/Control/Sta Interface

UTP

UTP Cable Indication

This pin is the UTP Cable Indication. Whe indicates that the UTP cable is being used

SPEED10

Speed 10 Mbps

When set high, this bit indicates a 10 Mbp when set low 100 Mbps operation. This p a low current LED to indicate that 100 Mbp is selected.

RX_LOCK

Lock for Clock/Data Recovery PLL

When this pin is high, it indicates that the covery PLL logic has locked to the input da

LNKSTS

Link Status Register Bit **Output**

This pin reflects the status of bit 2 register 1.

OPMODE0-OPMODE3

OPMODE0-OPMODE3 **Input**

These pins are used to control the forced or advertised operating mode of the NetPHY-1 device (see table below). The value is latched into the NetPHY-1 device registers at power-up/rese..

OP-MODE3	OP-MODE2	OP-MODE1	OP-MODE0	Function
0	0	0	0	Auto-Negotiation enable with all capabilities with Flow Control
0	0	0	1	Auto-Negotiation enable without all capabilities without Flow Control
0	0	1	0	Auto-Negotiation 100TX FDX with Flow Control only
0	0	1	1	Auto-Negotiation 100TX FDX/HDX without Flow Control
0	1	0	0	Auto-Negotiation 10TP FDX with Flow Control only
0	1	0	1	Auto-Negotiation 10TX FDX/HDX without Flow Control
0	1	1	0	Manual select 100TX FDX
0	1	1	1	Manual select 100TX HDX
1	0	0	0	Manual select 10TX FDX
1	0	0	1	Manual select 10TX HDX
1	0	1	0	Manual select 100FX FDX
1	0	1	1	Manual select 100FX HDX
1	1	1	1	Auto-Negotiation 10/100TX. HDX only

$\overline{\text{RTPR/NODE}}$

Repeater/Node Mode

When set high, this bit selects REPEATER
set low, it selects NODE. In REPEATE
NODE mode with Full Duplex configured,
Sense (CRS) output from the NetPHY-1 d
asserted only during receive activity. In NO
a mode not configured for Full Duplex ope
will be asserted during receive or transmi
power-up/reset, the value on this pin is
Register 16, bit 11.

BPALIGN

Bypass Alignment

This pin allows 100 Mbps transmit and r
streams to bypass all of the transmit and re
ations when set high. At power-up/reset, t
this pin is latched into bit Register 16, bit 1

BP4B5B

Bypass 4B5B Encoder/Decoder

This pin allows 100 Mbps transmit and r
streams to bypass the 4B to 5B encoder a
decoder circuits when set high. At power-
value on this pin is latched into Register 16, bit

BPSCR

Bypass Scrambler/Descrambler

This pin allows 100 Mbps transmit and r
streams to bypass the scrambler and desc
cuits when set high. At power-up/reset, t
this pin is latched into Register 16, bit 14.

10BTSER

Serial/Nibble Select

10 Mbps Serial Operation:

When set high, this input selects a serial o
mode. Manchester encoded transmit and r
is exchanged serially with a 10 MHz clock
least significant bits of the nibble-wide MII
pin TXD[0] and RXD[0] respectively. This
tended for use with the NetPHY-1 device c
a device (MAC or Repeater) that has a 10
interface. Serial operation is not supported
mode. For 100 Mbps, this input is ignored.

10 and 100 Mbps Nibble Operation:

When set low, this input selects the MII co
ble data transfer mode. Transmit and receiv
changed in nibbles on the TXD[3:0] and RX
respectively.

At power-up/reset, the value on this pin is
Register 18, bit 10.

Clock Interface

OSCI/X1

Crystal or Oscillator Input **Input**

This pin should be connected to a 25 MHz (±50 ppm) crystal if $\overline{\text{OSC/XTL}}$=0 or a 25 MHz (±50 ppm) external TTL oscillator input, if $\overline{\text{OSC/XTLB}}$=1.

X2

Crystal Oscillator Output **Output**

An external 25 MHz (±50 ppm) crystal should be connected to this pin if $\overline{\text{OSC/XTL}}$=0, or left unconnected if $\overline{\text{OSC/XTL}}$=1.

$\overline{\text{OSC/XTL}}$

Crystal or Oscillator Selector Pin **Output**

$\overline{\text{OSC/XTL}}$=0: An external 25 MHz (±50ppm) crystal should be connected to X1 and X2 pins.

- $\overline{\text{OSC/XTL}}$=1: An external 25 MHz (±50ppm) oscillator should be connected to X1 and X2 should be left unconnected.

CLK25M

25 MHz Clock Output **Output/Z**

This clock is derived directly from the crystal circuit.

PHY Address Interface

The PHYAD[4:0] pins provide up to 32 unique PHY addresses. An address selection of all zeros (00000) will result in a PHY isolation condition. See the isolate bit description in the BMCR, address 00.

PHYAD0

PHY Address 0 **Input**

This pin provides PHY address bit 0 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 8 during power up/reset.

PHYAD1

PHY Address 1 **Input**

This pin provides PHY address bit 1 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 7 during power up/reset.

PHYAD2

PHY Address 2 **Input**

This pin provides PHY address bit 2 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 6 during power up/reset.

PHYAD3

PHY Address 3 **Input**

This pin provides PHY address bit 3 for multiple PHY address applications. The status of this pin is latched into Register 17, bit 5 during power up/reset.

PHYAD4

PHY Address 4

This pin provides PHY address bit 4 for m
address applications. The status of this pi
into Register 17, bit 4 during power up/res

Miscellaneous

NC

No Connect

These pins are to be left unconnected (floa

BGREF

Bandgap Voltage Reference

Connect a 6.01K Ω, 1% resistor between
the BGRET pin to provide an accurate cu
ence for the NetPHY-1 device.

BGRET

Bandgap Voltage Reference Return

This is the return pin for 6.01K Ω resistor c

TRIDRV

Tri-State Digital Output

When set high, all digital output pins are s
impedance state, and I/O pins, go to input

$\overline{\text{RESET}}$

Reset

This pin is the active low input that initializes
1 device. It should remain low for 30 ms af
stabilized at 5 Vdc (nominal) before it transi

TESTMODE

Test Mode Control Pin

TESTMODE=0: Normal operating mode.

TESTMODE=1: Enable test mode.

Power and Ground Pins

The power (VCC) and ground (GND) pins
PHY-1 device are grouped in pairs of two
Digital Circuitry Power/Ground Pairs and
cuitry Power/Ground Pair.

DGND

Digital Logic Ground

These pins are the digital supply pairs.

DVCC

Digital Logic Power Supply

These pins are the digital supply pairs.

AGND

Analog Circuit Ground

These pins are the analog circuit supply pa

AVCC

Analog Circuit Power Supply

These pins are the analog circuit supply pa

FUNCTIONAL DESCRIPTION

The NetPHY-1 Fast Ethernet single-chip transceiver, provides the functionality as specified in the IEEE 802.3u standard, integrates complete 100BASE-FX, 100BASE-TX modules and a complete 10BASE-T module. The NetPHY-1 device provides a Media Independent Interface (MII) as defined in the IEEE 802.3u standard (Clause 22).

The NetPHY-1 device performs all Phys Sublayer (PCS), Physical Media Acce Twisted Pair Physical Medium Dependen sublayer, 10BASE-T Encoder/Decoder, a Pair Media Access Unit (TPMAU) functio shows the major functional blocks implem NetPHY-1 device.

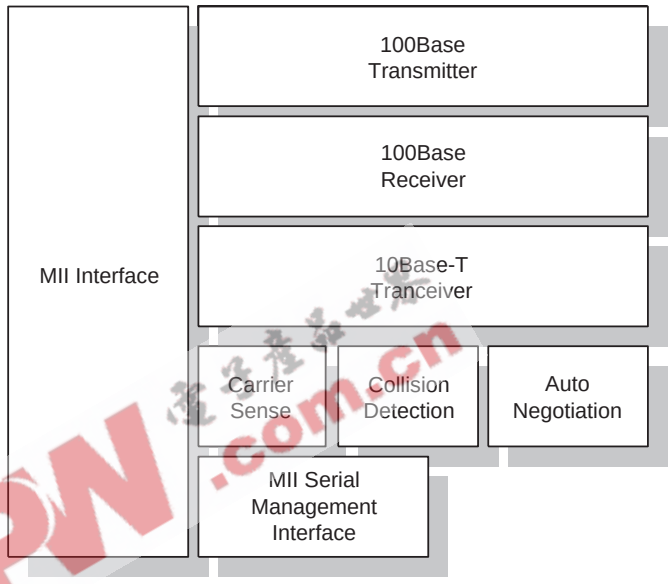


Figure 1. Functional Block Diagram

MII Interface

The purpose of the MII interface is to provide a simple, easy to implement connection between the MAC Reconciliation layer and the PHY. The MII is designed to make the differences between various media transparent to the MAC sublayer.

The MII consists of a nibble wide receive data bus, a nibble wide transmit data bus, and control signals to facilitate data transfers between the PHY and the Reconciliation layer.

- TXD (transmit data) is a nibble (4 bits) of data that are driven by the reconciliation sublayer synchronously with respect to TX_CLK. For each TX_CLK period which TX_EN is asserted, TXD (3:0) are accepted for transmission by the PHY.
- TX_CLK (transmit clock) output to the MAC reconciliation sublayer is a continuous clock that provides the timing reference for the transfer of the TX_EN, TXD, and TX_ER signals.
- TX_EN (transmit enable) input from the ciliation sublayer to indicate nibbles are b sented on the MII for transmission on medium. TX_ER (transmit coding error synchronously with respect to TX_CLK. asserted for one or more clock periods, is asserted, the PHY will emit one or m that are not part of the valid data delimit where in the frame being transmitted.
- RXD (receive data) is a nibble (4 bits) are sampled by the reconciliation su chronously with respect to RX_CLK RX_CLK period which RX_DV is ass (3:0) are transferred from the PHY reconciliation sublayer.
- RX_CLK (receive clock) output to the M iation sublayer is a continuous clock th the timing reference for the transfer of RXD, and RX_ER signals.

- RX_DV (receive data valid) input from the PHY to indicate the PHY is presenting recovered and decoded nibbles to the MAC reconciliation sublayer. To interpret a receive frame correctly by the reconciliation sublayer, RX_DV must encompass the frame starting no later than the Start-of-Frame delimiter and excluding any End-Stream delimiter.
- RX_ER (receive error) transitions synchronously with respect to RX_CLK. RX_ER will be asserted for 1 or more clock periods to i the reconciliation sublayer that an detected somewhere in the frame bei ted from the PHY to the reconciliation
- CRS (carrier sense) is asserted by the either the transmit or receive medium is deasserted by the PHY when the transmi medium are idle. Figure 2 depicts the beh during 10BASE-T and 100BASE-TX tran

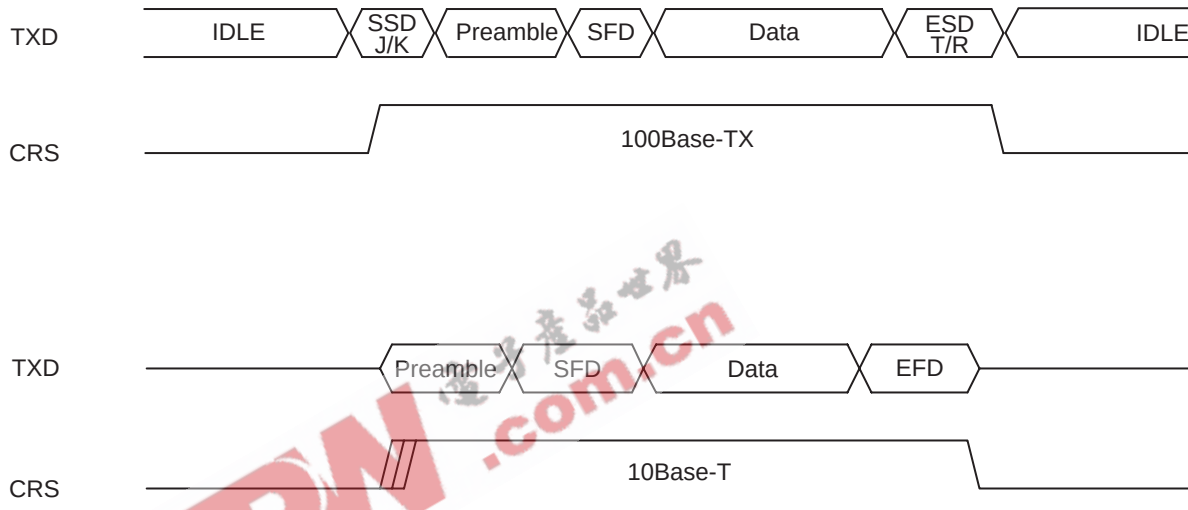


Figure 2. Carrier Sense during 10BASE-T and 100BASE-TX Transmission

100BASE Operation

The 100BASE transmitter receives 4-bit nibble data clocked in at 25 MHz at the MII and outputs a scrambled 5-bit encoded MLT-3 signal to the media at 100 Mbps. The on-chip clock circuit converts the 25 MHz clock into a 125 MHz clock for internal use.

The IEEE 802.3u specification defines the Media Independent Interface. The interface specification defines a dedicated receive data bus and a dedicated transmit data bus.

These two busses include various controls indications that facilitate data transfers b NetPHY-1 device and the Reconciliation la

100BASE Transmit

The 100BASE transmitter consists of th blocks shown in Figure 3. The 100BASE t tion converts 4-bit synchronous data prov MII to a scrambled MLT-3 125 million symb ond serial data stream.

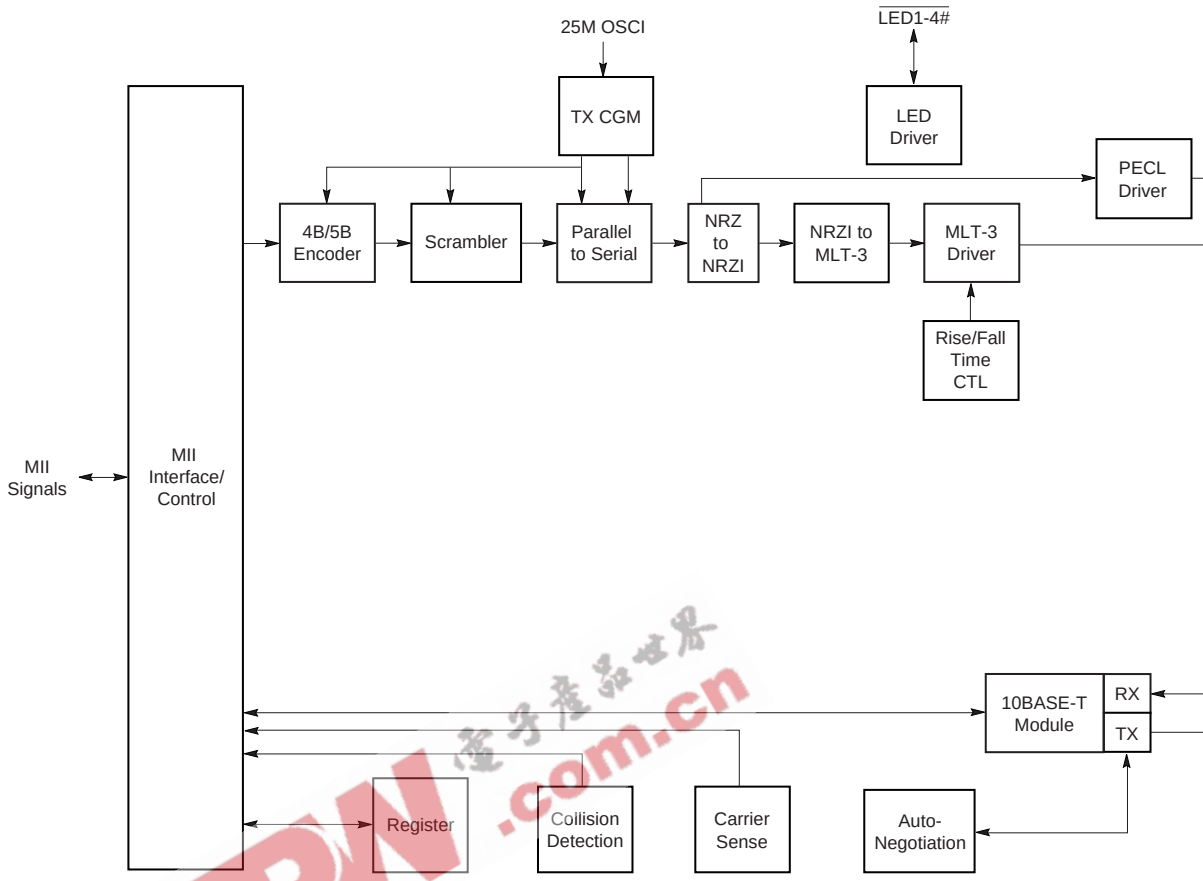


Figure 3. 100BASE Transmitter Functional Block Diagram

The block diagram in Figure 3 provides an overview of the functional blocks contained in the transmit section. The transmitter section contains the following functional blocks:

- 4B5B Encoder
- Scrambler
- Parallel-to-Serial Converter
- NRZ-to-NRZI Converter
- PECL Driver (For FX Operation)
- NRZI to MLT-3 (For TX Operation)
- MLT-3 Driver (For TX Operation)

4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission (see Table 1). This conversion is required for control and packet data to be combined in code groups. The 4B5B enc tutes the first 8 bits of the MAC preamble code-group pair (11000 10001) upon trans

The 4B5B encoder continues to replace 4B preamble and data nibbles with corres code-groups. At the end of the transmit p the deassertion of the Transmit Enable sig MAC Reconciliation layer, the 4B5B encode T/R code-group pair (01101 00111) indica frame. After the T/R code-group pair, the 4B continuously injects IDLEs into the tra stream until Transmit Enable is asserted a transmit packet is detected.

The NetPHY-1 device includes a Bypass 4B sion option within the 100BASE-TX transm port of applications like 100 Mbps repeate not require 4B5B conversion.

Table 1. 4B5B Code Group

Symbol	Meaning	4B code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	undefined	01101
R	ESD (2)	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V	Invalid	undefined	11001

Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100BASE-TX op scrambling the data, the total energy pres cable is randomly distributed over a wid range. Without the scrambler, energy le cable could peak beyond FCC limitations cies related to repeated 5B sequences like transmission of IDLE symbols. The scramb combined with the NRZ 5B data from the encoder via an XOR logic function. The scrambled data stream with sufficient rand decrease radiated emissions at critical f Since EMI is not a concern in a fiber app scrambler is bypassed in 100BASE-FX.

Parallel-to-Serial Converter

The Parallel-to-Serial Converter receives scrambled data from the scrambler and (i.e., converts it from a parallel to a serial d The serialized data stream is then prese NRZ-to-NRZI Encoder block

NRZ-to-NRZI Converter

After the transmit data stream has been scr serialized, the data must be NRZI encoded bility with the TP-PMD standard for 100BAS mission over Category-5 unshielded twisted

PECL Driver For 100BASE-FX

The PECL driver accepts NRZI coded data a it to PECL signal levels for transmission over

The output pair is a differential pseudo ECL terface designed to connect directly to a st optic PMD. The differential driver for the FX rent mode and is designed to drive resistive in a complementary mode. The FXTD± pi pable of sourcing current, this implies tha be set by the ratios of the Thevenin termin tors for each of the lines. RIOH is a pull-up r nected from the FXTD± output to VCC. RI down resistor connected from the FXTD ground. RIOH and RIOL are electrically in p an AC standpoint. A target impedance needed for the transmission line impedanc 62 Ω for RIOH and a value of 300 Ω for RI a Thevenin equivalent characteristic im 49.7 Ω and a VOH value of VCC-.88 volts with PECL circuits. VOL is required to be V greater. A sink current of 19 milli-amps achieve this through the output termination

MLT-3 Converter

The MLT-3 conversion is accomplished by co data stream output from the NRZI encoder nary data streams with alternately ph one events.

MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver which converts these streams to current sources and alternately drives either side of the transmit transformer primary winding resulting in a minimal current MLT-3 signal. Refer to Figure 4 for the block diagram of the MLT-3 converter.

100BASE Receiver

The 100BASE receiver contains several function blocks that convert the scrambled 125 Mbps serial data to synchronous 4-bit nibble data that is then provided to the MII.

The receive section contains the following functional blocks:

- Signal Detect
- Adaptive Equalization
- MLT-3-to-Binary Decoder
- Clock Recovery Module
- NRZI -o-NRZ Decoder
- Serial-to-Parallel Converter
- Descrambler
- Code Group Alignment
- 4B5B Decoder

100BASE-TX Signal Detect

The signal detect function meets the specific dated by the ANSI XT12 TP-PMD 100BAS dards for both voltage thresholds and timing

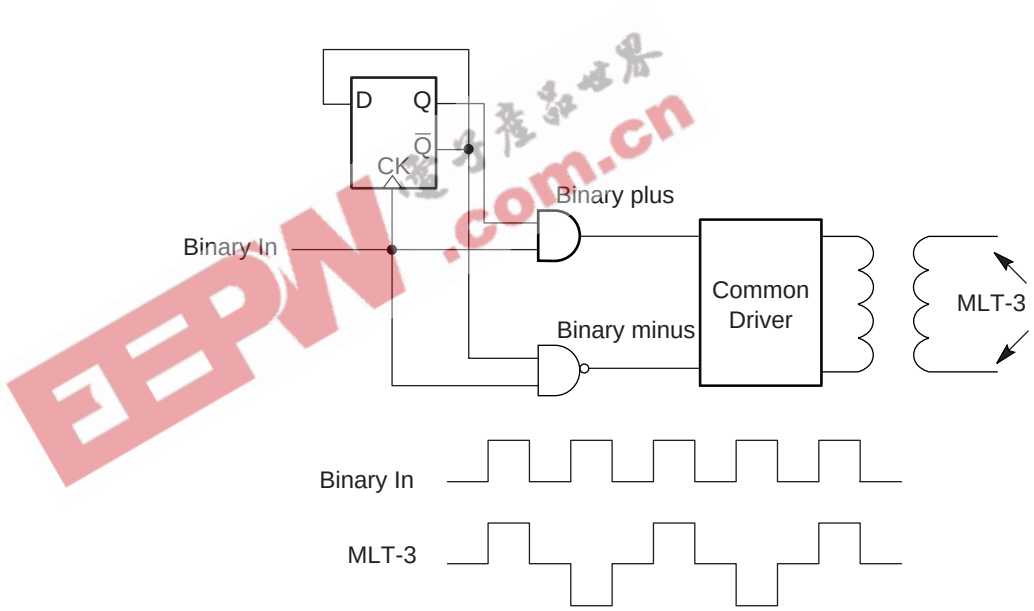


Figure 4. MLT-3 Converter Block Diagram

100BASE-FX Signal Detect

The NetPHY-1 device accepts signal detect information on the FXSD pin at PECL signal levels from the FX Optical Module.

Adaptive Equalization

When transmitting data at high speeds over copper twisted pair cable, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation caused by frequenc must be compensated for to ensure the int received data.

In order to ensure quality transmission whe MLT-3 encoding, the compensation mus adapt to various cable lengths and cable typ ing on the installed environment. The sele cable lengths for a given implementation, nificant compensation which will be over-k tion that includes shorter, less attenu lengths. Conversely, the selection of short ate cable lengths requiring less compe

cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

PECL Receiver

The PECL receiver accepts PECL signal-level data from the FX Optical Module and presents it to the Clock Recovery Module.

MLT-3-to-NRZI Decoder

The NetPHY-1 device decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data. The relationship between NRZI and MLT-3 data is shown in Figure 4.

Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3-to-NRZI decoder or the PECL Receiver. The Clock Recovery Module locks onto the data stream and extracts the 125 MHz reference clock. The extracted and synchronized clock and data are presented to the NRZI-to-NRZ Decoder.

NRZI-to-NRZ Decoder

The transmit data stream is required to be NRZI encoded in for compatibility with 100BASE transmission over. This conversion process must be reversed on the receive end. The NRZI-to-NRZ decoder, receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

Serial-to-Parallel Converter

The Serial-to-Parallel Converter receives a serial data stream from the NRZI-to-NRZ converter, and converts the data stream to parallel data to be presented to the descrambler.

Descrambler

Because of the scrambling process required to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, descrambles the data streams, and presents the data streams to the Code Group alignment block.

Note: *The scrambler is bypassed for 100BASE-FX operation.*

Code Group Alignment

The Code Group Alignment block receives unaligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected, and subsequent data is aligned on a fixed boundary.

4B5B Decoder

The 4B5B Decoder functions as a look-u
translates incoming 5B code groups into
data. When receiving a frame, the first tw
groups received are the start-of-frame de
symbols). The J/K symbol pair is stripped a
bles of preamble pattern are substituted.
code groups are the end-of-frame delimite
bols).The T/R symbol pair is also stripped f
ble presented to the Reconciliation layer.

10BASE-T Operation

The 10BASE-T transceiver is IEEE 802.3u
When the NetPHY-1 device is operating in
mode, the coding scheme is Manchester
cessed for transmit is presented to the MII
nibble format, converted to a serial bit s
Manchester encoded. When receiving, the
encoded bit stream is decoded and conver
ble format for presentation to the MII interfa

Collision Detection

For Half Duplex operation, a collision is det
the transmit and receive channels are act
neously. When a collision has been detect
reported by the COL signal on the MII inte
sion detection is disabled in Full Duplex op

Carrier Sense

Carrier Sense (CRS) is asserted in Half D
ation during transmission or reception of d
Full Duplex mode, CRS is asserted d
receive operations.

Auto-Negotiation

The objective of Auto-Negotiation is to prov
to exchange information between segmen
vices and to automatically configure both
take maximum advantage of their abilities
tant to note that Auto-Negotiation does not
segment characteristics. The Auto-Negotiat
provides a means for a device to advertis
modes of operation to a remote link partn
edge the receipt and understanding of com
of operation, and to reject un-shared mode
tion. This allows devices on both ends of a
establish a link at the best common mode o
If more than one common mode exists betw
devices, a mechanism is provided to allow
to resolve to a single mode of operation us
termined priority resolution function.

Auto-Negotiation also provides a parall
function for devices that do not support the
tiation feature. During Parallel detection the
change of configuration information, in
receive signal is examined. If it is discove
signal matches a technology that the rece

supports, a connection will be automatically established using that technology. This allows devices that do not support Auto-Negotiation but support a common mode of operation to establish a link.

MII Serial Management

The MII serial management interface consists of a data interface, basic register set, and a serial management interface to the register set. Through this interface it is possible to control and configure multiple PHY devices, get status and error information, and determine the type and capabilities of the attached PHY device(s).

The NetPHY-1 devices management functions correspond to MII specification for IEEE 802.3u-1995 (Clause 22) for registers 0 through 6 with vendor-specific registers 16,17, and 18.

In read/write operation, the management data frame is 64-bits long and starts with 32 contiguous logic one bits (preamble) synchronization clock cycles o
Start of Frame Delimiter (SFD) is indicate
pattern followed by the operation code (OP
cates Read operation and <01> indicates W
tion. For read operation, a 2-bit turnaroun
between Register Address field and Data
vided for MDIO to avoid contention. Follow
around time, 16-bit data is read from or w
management registers.

Serial Management Interface

The serial control interface uses a simple tw
rial interface to obtain and control the status
ical layer through the MII interface. The s
interface consists of Management Data C
and Management Data Input/Output (MDI/O

The MDIO pin is bidirectional and may be s
to 32 devices.

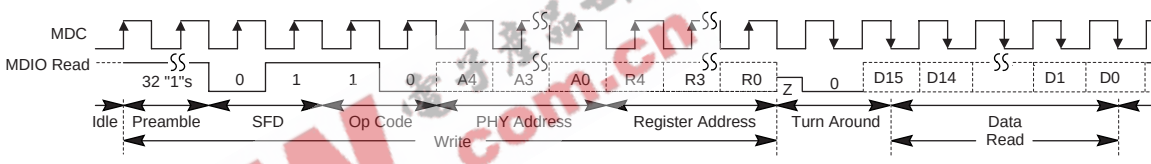


Figure 5. Management Interface - Read Frame Structure

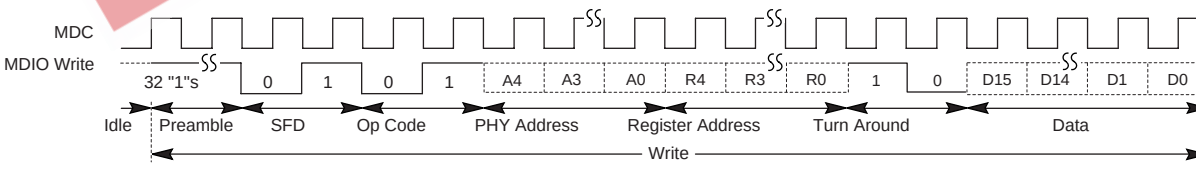


Figure 6. Management Interface - Write Frame Structure

Register Description

Register Address	Register Name	Description
0	BMCR	Basic Mode Control Register
1	BMSR	Basic Mode Status Register
2	PHYIDR1	PHY Identifier Register 1
3	PHYIDR2	PHY Identifier Register 2
4	ANAR	Auto-Negotiation Advertisement Register
5	ANLPAR	Auto-Negotiation Link Partner Ability Register
6	ANER	Auto-Negotiation Expansion Register
16	DSCR	AMD Specified Configuration Register
17	DSCSR	AMD Specified Configuration/Status Register
18	10BTCSR	10BASE-T Configuration/Status Register
Others	Reserved	Reserved For Future Use-Do Not Read/Write To These Registers

Key to Default

In the register description that follows, the default column takes the form:

<Reset Value>, <Access Type> / <Attribute(s)>

Where

<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
X	No default value
(Pin No.)	Value latched in from pin number at reset

<Access Type>:

RO = Read only

RW = Read/Write

<Attribute (s)>:

SC = Self clearing

P = Value permanently set

LL = Latching low

LH = Latching high

Basic Mode Control Register (BMCR) - Register 0

Bit	Bit Name	Default	Description
0.15	Reset	0, RW/SC	**Reset**: 1=Software reset 0=Normal operation When set this bit configures the PHY status and control regis default states. This bit will return a value of one until the rese complete.
0.14	Loopback	0, RW	**Loopback**: Loopback control register 1=Loopback enabled 0=Normal operation When in 100M operation is selected, setting this bit will caus descrambler to lose synchronization. A 720ms “dead time” w before any valid data appears at the MII receive outputs.
0.13	Speed Selection	1, RW	**Speed Select**: 1=100 Mbps 0=10 Mbps Link speed may be selected either by this bit or by Auto-Neg 12 of this register is set. When Auto-Negotiation is enabled, t return Auto-Negotiation link speed.
0.12	Auto-Negotiation Enable	1, RW	**Auto-Negotiation Enable**: 1= Auto-Negotiation enabled: 0= Auto-Negotiation disabled: When auto-Negotiation is enabled bits 8 and 13 will contain t Negotiation results. When Auto-Negotiation is disabled bits 8 determine the duplex mode and link speed.
0.11	Power Down	0, RW	**Power Down**: 1=Power Down 0=Normal Operation Setting this bit will power down the NetPHY-1 device with the the crystal oscillator circuit.
0.10	Isolate	(PHYAD= 00000), RW	**Isolate**: 1= Isolate 0= Normal Operation When this bit is set the data path will be isolated from the MI TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL and CR placed in a high impedance state. The management interface effected by this bit. When the PHY Address is set to 00000 th will be set upon power-up/reset.

Basic Mode Control Register (BMCR) - Register 0 (Continued)

Bit	Bit Name	Default	Description
0.9	Restart Auto-Negotiation	0, RW/SC	**Restart Auto-Negotiation**: 1= Restart Auto-Negotiation. 0= Normal Operation When this bit is set the Auto-Negotiation process is re-initiate Auto-Negotiation is disabled (bit 12 of this register cleared), th function and it should be cleared. This bit is self-clearing and value of 1 until Auto-Negotiation is initiated. The operation of Negotiation process will not be affected by the management clears this bit.
0.8	Duplex Mode	1, RW	**Duplex Mode**: 1= Full Duplex operation. 0= Normal operation If Auto-Negotiation is disabled, setting this bit will cause the device to operate in Full Duplex mode. When Auto-Negotiation this bit reflects the duplex selected by Auto-Negotiation.
0.7	Collision Test	0, RW	**Collision Test**: 1= Collision Test enabled. 0= Normal Operation When set, this bit will cause the COL signal to be asserted in the assertion of TX_EN.
0.6	Reserved	0, RO	**Reserved**: Write as 0, ignore on read.

Basic Mode Status Register (BMSR) - Register 1

Bit	Bit Name	Default	Description
1.15	100BASE-T4	0,RO/P	**100BASE-T4 Capable**: 1=NetPHY-1 device is able to perform in 100BASE-T4 mode 0=NetPHY-1 device is not able to perform in 100BASE-T4 m
1.14	100BASE-TX Full Duplex	1,RO/P	**100BASE-TX Full Duplex Capable**: 1=NetPHY-1 device is able to perform 100BASE-TX in Full D 0=NetPHY-1 device is not able to perform 100BASE-TX in F mode.
1.13	100BASE-TX Half Duplex	1,RO/P	**100BASE-TX Half Duplex Capable**: 1=NetPHY-1 device is able to perform 100BASE-TX in Half D 0=NetPHY-1 device is not able to perform 100BASE-TX in H mode.
1.12	10BASE-T Full Duplex	1,RO/P	**10BASE-T Full Duplex Capable**: 1=NetPHY-1 device is able to perform 10BASE-T in Full Dup 0=NetPHY-1 device is not able to perform 10BASE-T in Full D
1.11	10BASE-T Half Duplex	1,RO/P	**10BASE-T Half Duplex Capable**: 1=NetPHY-1 device is able to perform 10BASE-T in Half Dup 0=NetPHY-1 device is not able to perform 10BASE-T in Half D
1.10-1.7	Reserved	0,RO	**Reserved**: Write as 0, ignore on read.
1.6	MF Preamble Suppression	0,RO	**MII Frame Preamble Suppression**: 1=PHY will accept management frames with preamble suppr 0=PHY will not accept management frames with preamble su
1.5	Auto-Negotiation Complete	0,RO	**Auto-Negotiation Complete**: 1=Auto-Negotiation process completed. 0=Auto-Negotiation process not completed.
1.4	Remote Fault	0, RO/LH	**Remote Fault**: 1= Remote fault condition detected (cleared on read or by a Fault criteria and detection method is NetPHY-1 device imple specific. This bit will set after the RF bit in the ANLPAR (bit 1 address 05) is set. 0= No remote fault condition detected.
1.3	Auto-Negotiation Ability	1,RO/P	**Auto Configuration Ability**: 1=NetPHY-1 device able to perform Auto-Negotiation. 0=NetPHY-1 device not able to perform Auto-Negotiation.
1.2	Link Status	0,RO/LL	**Link Status**: 1=Valid link established (for either 10 Mbps or 100 Mbps ope 0=Link not established. The link status bit is implemented with a latching function, so occurrence of a link failure condition causes the Link Status cleared and remain cleared until it is read via the manageme

Basic Mode Status Register (BMSR) - Register 1

Bit	Bit Name	Default	Description
1.1	Jabber Detect	0, RO/LH	**Jabber Detect**: 1=Jabber condition detected. 0=No jabber condition detected. This bit is implemented with a latching function. Once Jabbe are detected this bit will remain set until a read operation is through a management interface or a NetPHY-1 device reset works only in 10 Mbps mode.
1.0	Extended Capability	1,RO/P	**Extended Capability**: 1=Extended register capable. 0=Basic register capable only.

PHY ID Identifier Register 1 (PHYIDR1) - Register 2

The PHY Identifier Registers 1 and 2 work together in a single identifier of the NetPHY-1 device. The Identifier consists of a concatenation of the **Organizationally Unique Identifier** (OUI), a vendor's mod and a model revision number. The IEEE as is 00606E.

Bit	Bit Name	Default	Description
2.15-2.0	OUI_MSB	<0181H>	**OUI Most Significant Bits**: This register stores bits 3 - 18 of the OUI (00606E) to bits 15 register, respectively. The most significant two bits of the OUI (the IEEE standard refers to these as bit 1 and 2).

PHY Identifier Register 2 (PHYIDR2) - Register 3

Bit	Bit Name	Default	Description
3.15-3.10	OUI_LSB	<101110>,RO/P	**OUI Least Significant Bits**: Bits 19 - 24 of the OUI (00606E) are mapped to bits 15 - 10 of t respectively.
3.9-3.4	VNDR_MDL	<000000>,RO/P	**Vendor Model Number**: Six bits of the vendor model number mapped to bits 9 - 4 (mos bit to bit 9).
3.3-3.0	MDL_REV	<0001>,RO/P	**Model Revision Number**: Four bits of the vendor model revision number mapped to bits significant bit to bit 3).

Auto-Negotiation Advertisement Register(ANAR) - Register 4

This register contains the advertised abilities of the NetPHY-1 device as they will be transmitted to link p ing Auto-Negotiation.

Bit	Bit Name	Default	Description
4.15	NP	0,RO/P	**Next Page Indication**: 0=No next page available 1=Next page available The NetPHY-1 device does not support the next page functio permanently set to 0
4.14	ACK	0,RO	**Acknowledge**: 1=Link partner ability data reception acknowledged. 0=Not acknowledged. The NetPHY-1 device's Auto-Negotiation state machine will a control this bit in the outgoing FLP bursts and set it at the appr during the Auto-Negotiation process. Software should not atte to this bit.
4.13	RF	0, RW	**Remote Fault**: 1=Local Device senses a fault condition. 0=No fault detected.
4.12-4.11	Reserved	0, RW	**Reserved**: Write as 0, ignore on read.
4.10	FCS	0, RW	**Flow Control Support**: 1=Controller chip supports flow control ability. 0=Controller chip does not support flow control ability.
4.9	T4	0, RO/P	**100BASE-T4 Support**: 1=100BASE-T4 supported by the local device. 0=100BASE-T4 not supported. The NetPHY-1 device does not support 100BASE-T4 so this permanently set to 0.
4.8	TX_FDX	1, RW	**100BASE-TX Full Duplex Support**: 1=100BASE-TX Full Duplex supported by the local device. 0=100BASE-TX Full Duplex not supported.
4.7	TX_HDX	1, RW	**100BASE-TX Support**: 1=100BASE-TX supported by the local device. 0=100BASE-TX not supported.
4.6	10_FDX	1, RW	**10BASE-T Full Duplex Support**: 1=10BASE-T Full Duplex supported by the local device. 0=10BASE-T Full Duplex not supported.
4.5	10_HDX	1, RW	**10BASE-T Support**: 1=10BASE-T supported by the local device. 0=10BASE-T not supported.
4.4-4.0	Selector	<00001>, RW	**Protocol Selection Bits**: These bits contain the binary encoded protocol selector supp node. <00001> indicates that this device supports IEEE 802.3 CSM

Auto-Negotiation Link Partner Ability Register (ANLPAR) - Register 5

This register contains the advertised abilities of the link partner as they are received during Auto-Nego

Bit	Bit Name	Default	Description
5.15	NP	0, RO	**Next Page Indication**: 0= Link partner, no next page available. 1= Link partner, next page available.
5.14	ACK	0, RO	**Acknowledge**: 1=Link partner ability data reception acknowledged. 0=Not acknowledged. The NetPHY-1 device's Auto-Negotiation state machine will a control this bit from the incoming FLP bursts. Software should to write to this bit.
5.13	RF	0, RO	**Remote Fault**: 1=Remote fault indicated by link partner. 0=No remote fault indicated by link partner.
5.12-5.10	Reserved	0, RO	**Reserved**: Write as 0, ignore on read.
5.9	T4	0, RO	**100BASE-T4 Support**: 1=100BASE-T4 supported by the link partner. 0=100BASE-T4 not supported by the link partner.
5.8	TX_FDX	0, RO	**100BASE-TX Full Duplex Support**: 1=100BASE-TX Full Duplex supported by the link partner. 0=b 100BASE-TX Full Duplex not supported by the link partn
5.7	TX_HDX	0, RO	**100BASE-TX Support**: 1=100BASE-TX Half Duplex supported by the link partner. 0=100BASE-TX Half Duplex not supported by the link partne
5.6	10_FDX	0, RO	**10BASE-T Full Duplex Support**: 1=10BASE-T Full Duplex supported by the link partner. 0=10BASE-T Full Duplex not supported by the link partner.
5.5	10_HDX	0, RO	**10BASE-T Support**: 1=10BASE-T Half Duplex supported by the link partner. 0=10BASE-T Half Duplex not supported by the link partner.
5.4-5.0	Selector	<00000>, RO	**Protocol Selection Bits**: Link partners binary encoded protocol selector.

Auto-Negotiation Expansion Register (ANER) - Register 6

Bit	Bit Name	Default	Description
6.15-6.5	Reserved	0, RO	**Reserved**: Write as 0, ignore on read.
6.4	PDF	0, RO/LH	**Local Device Parallel Detection Fault**: PDF=1: A fault detected via parallel detection function. PDF=0: No fault detected via parallel detection function.
6.3	LP_NP_ABLE	0, RO	**Link Partner Next Page Able**: LP_NP_ABLE=1: Link partner, next page available. LP_NP_ABLE=0: Link partner, no next page.
6.2	NP_ABLE	0,RO/P	**Local Device Next Page Able**: NP_ABLE=1: NetPHY-1 device, next page available. NP_ABLE=0: NetPHY-1 device, no next page. NetPHY-1 device does not support this function, so this bit is
6.1	PAGE_RX	0, RO/LH	**New Page Received**: A new link code word page received. This bit will be automatic when the register (Register 6) is read by management.
6.0	LP_AN_ABLE	0, RO	**Link Partner Auto-Negotiation Able**: LP_AN_ABLE=1 indicates that the link partner supports Auto Negotiation.

AMD Specified Configuration Register (DSCR) - Register 16

Bit	Bit Name	Default	Description
16.15	BP_4B5B	, RW	**Bypass 4B5B Encoding and 5B4B Decoding**: 1=4B5B encoder and 5B4B decoder function bypassed. 0=Normal 4B5B and 5B4B operation The value of the pin is this bit at power-up/reset.
16.14	BP_SCR	Pin 97, RW	**Bypass Scrambler/Descrambler Function**: 1=Scrambler and descrambler function bypassed. 0=Normal scrambler and descrambler operation. The value of the input pin is latched into this bit at power-up/
16.13	BP_ALIGN	Pin 98, RW	**Bypass Symbol Alignment Function**: 1= Receive functions (descrambler, symbol alignment and sy decoding functions) bypassed. Transmit functions (symbol en scrambler) bypassed. 0= Normal operation. The value of the BPALIGN input pin is latched into this bit at reset.
16.12	Reserved	0, RW	**Reserved**: This bit must be set as 0.
16.11	REPEATER	Pin 94, RW	**Repeater/Node Mode**: 1=Repeater mode. 0=Node mode. In Repeater mode, the Carrier Sense (CRS) output from the device will be asserted only by receive activity. In NODE mode not configured for Full Duplex operation, CRS will be asserte receive or transmit activity. The value of the RPTR/NODE input pin is latched into this bit reset.
16.10	TX	1, RW	**100BASE-TX or FX Mode Control**: 1=100BASE-TX operation. 0=100BASE-FX operation.
16.9	UTP	1, RW	**UTP Cable Control**: 1=The media is a UTP cable, 0=STP.
16.8	CLK25MDIS	0, RW	**CLK25M Disable**: 1=CLK25M output clock signal tri-stated. 0=CLK25M enabled. This bit should be set to 1 to disable the 25 MHz output and re bounce and power consumption. For applications requiring th output, set this bit to 0.
16.7	F_LINK_100	1, RW	**Force Good Link in 100 Mbps**: 1=Normal 100 Mbps operation. 0=Force 100 Mbps good link status. This bit is useful for diagnostic purposes.
16.6	Reserved	0, RW	**Reserved**: This bit must be written as 0.

AMD Specified Configuration Register (DSCR) - Register 16

Bit	Bit Name	Default	Description
16.5	LINKLED_CTL	0, RW	**LINKLED Mode Select**: 0= Link LED output configured to indicate link status only. 1= Link LED output configured to indicate traffic status: Whe status is OK, the LED will be on. When the chip is in transmi receiving, it flashes.
16.4	FDXLED_MODE	0, RW	**FDXLED Mode Select**: 1= FDXLED output configured to indicate polarity in 10BASE 0= FDXLED output configured to indicate Full DuplexFull Du status for 10 Mbps and 100 Mbps operation.
16.3	SMRST	0, RW	**Reset State Machine**: When this bit is set to 1, all state internal machines will be re will clear after reset is completed.
16.2	MFPSC	0, RW	**MF Preamble Suppression Control**: 1= MF preamble suppression on. 0= MF preamble suppression off. MII frame preamble suppression control bi.t
16.1	SLEEP	0, RW	**Sleep Mode**: Writing a 1 to this bit will cause NetPHY-1 device to enter Slee power down all circuits except the oscillator and clock generat exit Sleep mode, write 0 to this bit position. The prior configur retained when the sleep state is terminated, but the state ma reset.
16.0	RLOUT	0, RW	**Remote Loopout Control**: When this bit is set to 1, the received data will loop out to the channel. This is useful for bit error rate testing.

AMD Specified Configuration and Status Register (DSCSR) - Register 17

Bit	Bit Name	Default	Description
17.15	100FDX	1, RO	**100 M Full Duplex Operation**: After Auto-Negotiation is completed, the results will be writte A 1 in this bit position indicates 10 0M Full Duplex operation. T can read bits [15:12] to determine which mode is selected af Negotiation. This bit is invalid when Auto-Negotiation is disab
17.14	100HDX	1, RO	**100 M Half Duplex Operation**: After Auto-Negotiation is completed, the results will be writte A 1 in this bit position indicates 100 M Half Duplex operation. T can read bits [15:12] to determine which mode is selected af Negotiation. This bit is invalid when Auto-Negotiation is disab
17.13	10FDX	1, RO	**10 M Full Duplex Operation**: After Auto-Negotiation is completed, the results will be writte A 1 in this bit position indicates 10 M Full Duplex operation. T can read bits [15:12] to determine which mode is selected af Negotiation. This bit is invalid when Auto-Negotiation is disab
17.12	10HDX	1, RO	**10 M Half Duplex Operation**: After Auto-Negotiation is completed, the results will be writte A 1 in this bit position indicates 10M Half Duplex operation. T can read bits [15:12] to determine which mode is selected af Negotiation. This bit is invalid when Auto-Negotiation is disab
17.11-17.10	Reserved	0, RW	**Reserved**: Write as 0, ignore on read.
17.8-17.4	PHYAD[4:0]	(PHYAD), RW	**PHY Address Bit 4:0**: The values of the PHYAD[4:0] pins are latched to this registe up/reset. The first PHY address bit transmitted or received is 4). A station management entity connected to multiple PHY e know the appropriate address of each PHY. A PHY address will cause the isolate bit of the BMCR (bit 10, Register Addre set.

Bit	Bit Name	Default	Description
17.3-17.0	ANMB[3:0]	0, RO	**Auto-Negotiation Monitor Bits**: These bits are for debug only. The Auto-Negotiation status w to these bits.

b3	b2	b1	b0	
0	0	0	0	In IDLE state
0	0	0	1	Ability match
0	0	1	0	Acknowledge match
0	0	1	1	Acknowledge match fail
0	1	0	0	Consistency match
0	1	0	1	Consistency match fail
0	1	1	0	Parallel detect signal_link_ready
0	1	1	1	Parallel detect signal_link_ready fail
1	0	0	0	Auto-Negotiation completed successfu

10BASE-T Configuration/Status (10BTCSRSCR) - Register 18

Bit	Bit Name	Default	Description
18.15	Reserved	0, RO	**Reserved**: Write as 0, ignore on read.
18.14	LP_EN	1, RW	**Link Pulse Enable**: 1=Transmission of link pulses enabled. 0=Link pulses disabled, good link condition forced. This bit is valid only in 10 Mbps operation.
18.13	HBE	Inverse Pin 94, RW	**Heartbeat Enable**: 1=Heartbeat function enabled. 0=Heartbeat function disabled. When the NetPHY-1 device is configured for Full Duplex opera will be ignored (the collision/heartbeat function is invalid in F mode). The initial state of this bit is the inverse value of RPTR/ pin at power on reset.
18.12	Reserved	0, RO	**Reserved**: Write as 0, ignore on read.
18.11	JABEN	1, RW	**Jabber Enable**: 1= Jabber function enabled. 0= Jabber function disabled. Enables or disables the Jabber function when the NetPHY-1 10BASE-T Full Duplex or 10BASE-T Transceiver Loop-back
18.10	10BT_SER	Pin 98, RW	**10BASE-T Serial Mode**: 1=10BASE-T serial mode selected. 0=10BASE-T nibble mode selected. The value on the 10BTSER input pin is latched into this bit a rese.t Serial mode not supported for 100 Mbps operation.
18.9-18.1	Reserved	0, RO	**Reserved**: Write as 0, ignore on read.
18.0	POLR	0, RO	**Polarity Reversed**: When this bit is set to 1, it indicates that the 10M cable polarity This bit is set and cleared by 10BASE-T module automatical

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –0°C to +70°C

Supply Voltage
with Respect to Ground . . . . . -4.75 V to +5.25 V

DC Input Voltage (V_{IN}) . . . . . –0.5 V to V_{CC} +0.5 V

DC Output or I/O Pin Voltage (V_{OUT}) . . . . .–0.5 V to V_{CC} +0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . .0°

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V

Operating ranges define those limits betwee functionality of the device is guaranteed.

Power Consumption

100BASE-TX Full Duplex . . . . . .

(Measured using Unscrambled IDLE transmi back to RXIN, includes external termination circ

10BASE-T Full Duplex . . . . . .

(Measured using Maximum packet size, mi transmission looped back to RXIN, includes exte tion circuitry)

Auto-Negotiation . . . . . .

(Measured during Parallel Detect until link estal

Idle . . . . . .

(Measured with no link established)

Power Down Mode . . . . . .

(Measured while MII Register 0 Bit 11 set true)

DC ELECTRICAL CHARACTERISTICS
(V_{CC} = 5 V_{DC}, ±5%, T_A = 0 to 70, unless specified otherwise)

Symbol	Parameter	Conditions	Min	Typical	M
I_{100TX}	Supply Current 100BASE 100BASE-TX active	V_{cc} = 5.0 V		180	1
I_{10TTP}	Supply Current 10BASE-TX active (Random data, Random IPG and Random size)	V_{cc} = 5.0 V		120	
I_{10TWC}	Supply Current 10BASE-TX active (Max. Packet size, Min. IPG and Worst case data pattern)	V_{cc} = 5.0 V			2
I_{PDM}	Supply Current Power Down Mode	V_{cc} = 5.0 V			4
I_{AN}	Supply Current during Auto-Negotiation	V_{cc} = 5.0 V			1
I_{RST}	Supply Current during Reset.	V_{cc} = 5.0 V			1
TTL Inputs (TXD0-TXD3, TX_CLK, MDIO, TX_EN, TX_DV, TX_ER, TESTMODE, PHYAD0-4, OPMODE0-4, RPTR, BPALIGN BPSCR, 10BTSER, $\overline{\text{RESET}}$)					
V_{IL}	Input Low Voltage	IIL = -400 uA			0
V_{IH}	Input High Voltage	IIH = 100 uA	2.0		
I_{IL}	Input Low Current	VIN = 0.4 V	-200		
I_{IH}	Input High Current	VIN = 2.7 V			1

DC ELECTRICAL CHARACTERISTICS
(V_{CC} = 5 V_{DC}, ±5%, T_A = 0 to 70, unless specified otherwise) (Continued)

Symbol	Parameter	Conditions	Min	Typical	M
MII TTL Outputs (RXD0-3, RX_EN, RX_DV, RX_ER, CRS, COL, MDIO)					
V_{OL}	Output Low Voltage	IOL = 4 mA			0
V_{OH}	Output High Voltage	IOH = -4 mA	2.4		
Non-MII TTL Outputs ($\overline{\text{TXLED}}$, $\overline{\text{RXLED}}$, $\overline{\text{LINKLED}}$, $\overline{\text{COLLED}}$, $\overline{\text{FDXLED}}$, RX_LOCK)					
V_{OL}	Output Low Voltage	IOL = 1 mA			0
V_{OH}	Output High Voltage	IOH = -0.1 mA	2.4		
V_{ICM}	RXI+/RXI- Input Common-Mode Voltage	100 Ω Termination Across	1.5	2.0	2
Twisted Pair Transmitter					
^{I}TD100	100TX++± 100BASE-TX Mode Differential Output Current		19		2
ITD10	10TX± 10BASE-T Differential Output Current		44	50	5
PECL Receiver					
VIH - VCC	PECL Receiver Voltage - High		-1.16		-0
VIL - VCC	PECL Receiver Voltage - Low		-1.81		-1
PECL Signal Detect					
VIH - VCC	PECL Signal Detect Voltage - High		-1.16		-0
VIL - VCC	PECL Signal Detect Voltage - Low		-1.81		-1
PECL Transmitter					
VOH - VCC	PECL Output Voltage - High		-1.05		-0
VOL - VCC	PECL Output Voltage - Low		-1.85		-1

AC ELECTRICAL CHARACTERISTICS
(Over full range of operating conditions unless specified otherwise)

Symbol	Parameter	Conditions	Min	Typical	M
Transmitter					
$t_{TR/F}$	100TXO+/- Differential Rise/Fall Time		3.0		5
t_{TM}	100TXO+/- Differential Rise/Fall Time Mismatch		-0.5		0
t_{TDC}	100TXO+/- Differential Output Duty Cycle Distortion		-0.5		0
$t_{T/T}$	100TXO+/- Differential Output Peak-to-Peak Jitter			300	
XOST	100TXO+/- Differential Voltage Overshoot				

AC ELECTRICAL CHARACTERISTICS
(Over full range of operating conditions unless specified otherwise) (Continued

Symbol	Parameter	Conditions	Min	Typical	M
PECL Transmitter (FX Transmit Interface)					
$pt_{TR/F}$	100FXTD+/- Differential Rise/Fall Time		1.0		2
pt_{TM}	100FXTD+/- Differential Rise/Fall Time Mismatch		-0.5		0
pt_{TDC}	100FXTD+/- Differential Output Duty Cycle Distortion		-0.5		0
pt_{PPJ}	100FXTD+/- Differential Output Peak-to-Peak Jitter				3
pt_{DDJ}	100FXTD+/- Differential Output Data Dependent Jitter				5
Clock Specifications					
XNTOL	TX Input Clock Frequency Tolerance	25 MHz Frequency			
XBTOL	TX Output Clock Frequency Tolerance	25 MHz Frequency	-100		+1
t_{PWH}	OSC Pulse Width High		14		
t_{PWL}	OSC Pulse Width Low		14		
t_{RPWH}	RX_CLK Pulse Width High		14		
t_{RPWL}	RX_CLK Pulse Width Low		14		

MII 100BASE-TX Transmit Timing

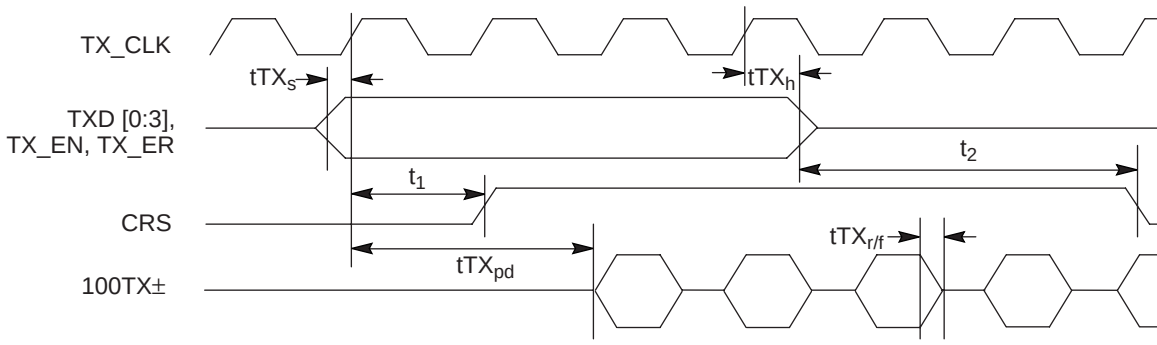


Figure 7. MII 100BASE-TX Transmit Timing Diagram

MII 100BASE-TX Transmit Timing Parameters (Half Duplex)

Symbol	Parameter	Conditions	Min	Typical (Note 1)	Ma
tTX_s	TXD[0:3], TX_EN, TX_ER Setup To TX_CLK High		11	-	-
tTX_h	TXD[0:3], TX_EN, TX_ER Hold From TX_CLK High		0	-	-
t1	TX_EN Sampled To CRS Asserted		-	4	-
t2	TX_EN Sampled To CRS De-asserted		-	4	-
tTX_{pd}	TX_EN Sampled To TPO Out (Tx Latency)		-	8	-
$tTX_{r/f}$	100TX Driver Rise/Fall Time	90% To 10%, Into 100 Ω Differential	3	4	5

Note:
1. Typical values are at 25 and are for design aid only; not guaranteed and not subject to production testing.

MII 100BASE-TX Receive Timing

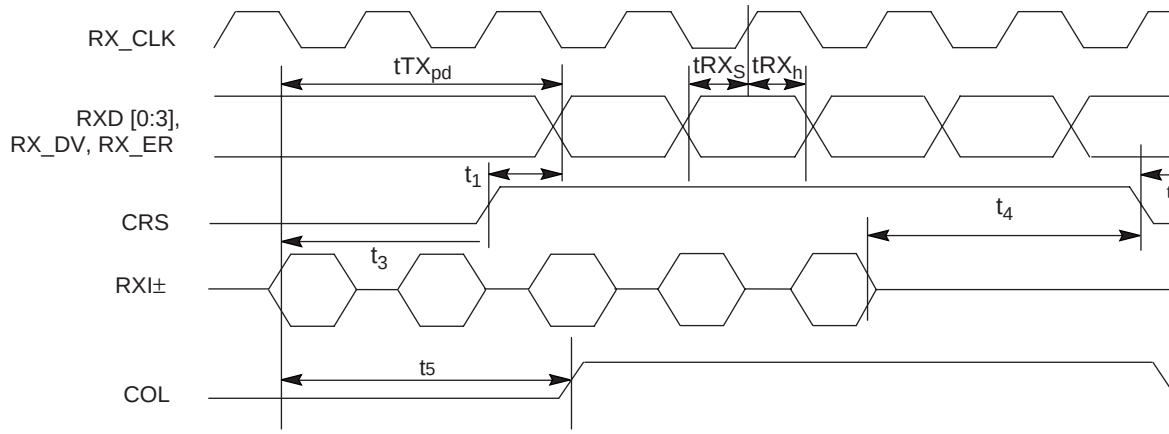


Figure 8. MII 100BASE-TX Receive Timing Diagram

MII-100BASE-TX Receive Timing Parameter (Half Duplex)

Symbol	Parameter	Conditions	Min	Typical (Note 1)	Ma
tRX_S	RXD[0:3), RX_DV, RX_ER Setup To RX_CLK High		10	-	-
tRX_h	RXD[0:3], RX_DV, RX_ER Hold From RX_CLK High		10	-	-
tRX_{pd}	RXI In To RXD[0:3] Out (RX Latency)		-	15	-
t1	CRS Asserted To RXD[0:3], RX_DV, RX_ER		-	4	-
t2	CRS De-asserted To RXD[0:3], RX_DV, RX_ER		-	0	-
t3	RXI In To CRS Asserted		10	-	1
t4	RXI Quiet To CRS De-asserted		14	-	1
t5	RXI In To COL De-asserted		14	-	1

Note:
1. Typical values are at 25 and are for design aid only; not guaranteed and not subject to production testing.

Auto-Negotiation and Fast Link Pulse Timing

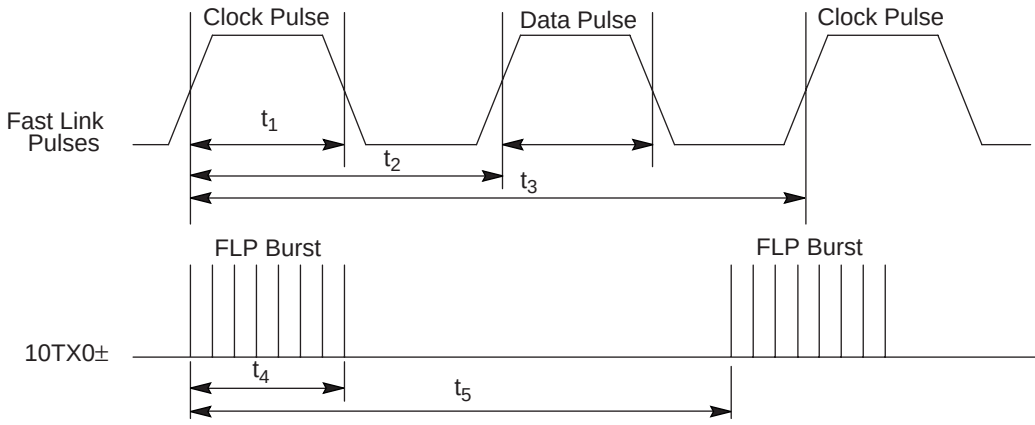


Figure 9. Auto-Negotiation and Fast Link Pulse Timing Diagram

Auto-Negotiation and Fast Link Pulse Timing Parameters

Symbol	Parameter	Conditions	Min	Typical	Ma
t1	Clock/Data Pulse Width		-	100	-
t2	Clock Pulse To Data Pulse Period	DATA = 1	-	62.5	-
t3	Clock Pulse To Clock Pulse Period		-	125	-
t4	FLP Burst Width		-	2	-
t5	FLP Burst To FLP Burst Period		-	13.93	-
-	Clock/Data Pulses Per Burst		33	33	3

MII 10BASE-T Nibble Transmit Timing

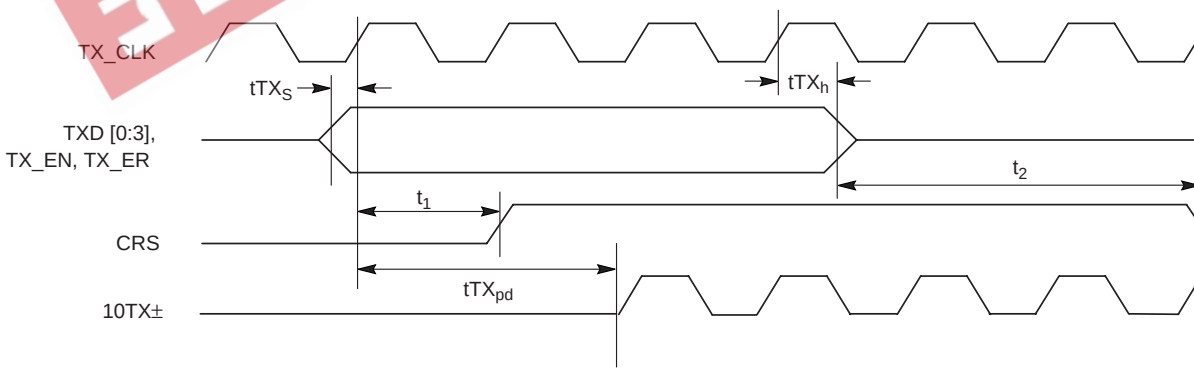


Figure 10. MII 10BASE-T Nibble Transmit Timing Diagram

MII-10BASE-T Nibble Transmit Timing Parameters

Symbol	Parameter	Conditions	Min	Typical	Ma
tTX_S	TXD[0:3), TX_EN, TX_ER Setup To TX_CLK High		11	-	-
tTX_h	TXD[0:3], TX_EN, TX_ER Hold From TX_CLK High		0	-	-
t1	TX_EN Sampled To CRS Asserted		-	2	4
t2	TX_EN Sampled To CRS De-asserted		-	15	2
tTX_{pd}	TX_EN Sampled To 10TXO Out (Tx Latency)		-	2	4

MII 10BASE-T Receive Nibble Timing Diagram

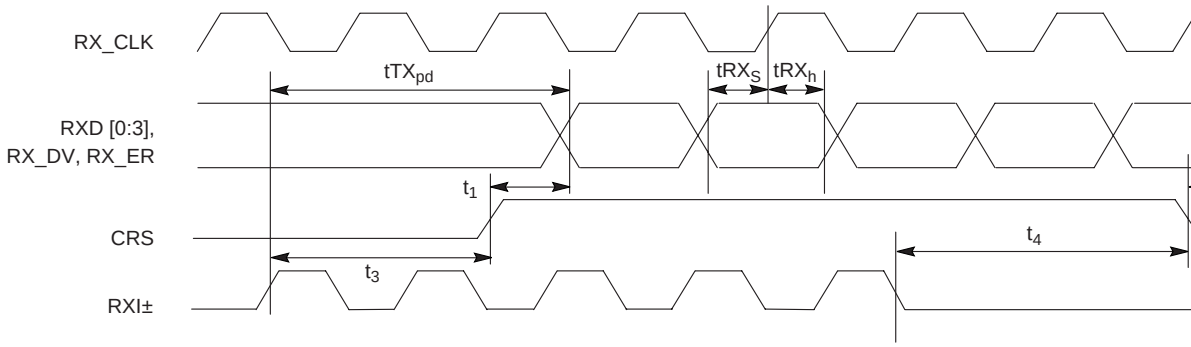


Figure 11. MII 10BASE-T Receive Nibble Timing Diagram

MII-10BASE-T Receive Nibble Timing Parameters

Symbol	Parameter	Conditions	Min	Typical	Ma
tRX_S	RXD[0:3), RX_DV, RX_ER Setup To RX_CLK High		10	-	-
tRX_h	RXD[0:3], RX_DV, RX_ER Hold From RX_CLK High		10	-	-
tRX_{pd}	RXI In To RXD[0:3] Out (RX Latency)		-	7	-
t1	CRS Asserted To RXD[0:3], RX_DV, RX_ER		1	14	2
t2	CRS De-asserted To RXD[0:3], RX_DV, RX_ER		-	-	3
t3	RXI In To CRS Asserted		1	2	4
t4	RXI Quiet To CRS De-asserted		1	10	1

10BASE-T SQE (Heartbeat) Timing

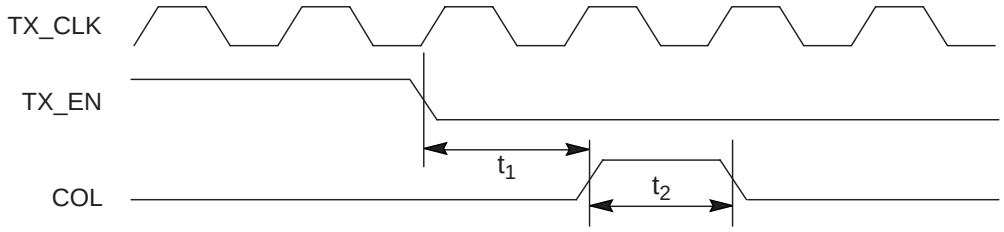


Figure 12. 10BASE-T SQE (Heartbeat) Timing Diagram

10BASE-T SQE (Heartbeat) Timing Parameters

Symbol	Parameter	Conditions	Min	Typical	Ma
t1	COL (SQE) Delay After TX_EN Off		0.65	1.3	1.
t2	COL (SQE) Pulse Duration		0.5	1.1	1.

10BASE-T Jab and Unjab Timing

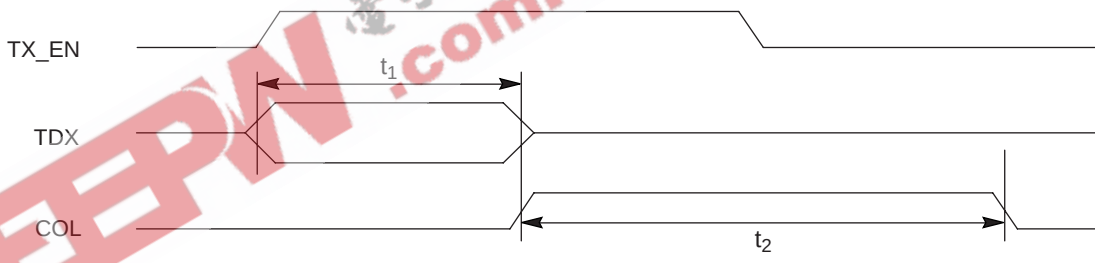


Figure 13. 10BASE-T Jab and Unjab Timing Diagram

10BASE-T Jab and Unjab Timing Parameters

Symbol	Parameter	Conditions	Min	Typical	Ma
t1	Maximum Transmit Time		20	48	15
t2	Unjab Time		250	505	15

MDIO Timing when OUTPUT by STA

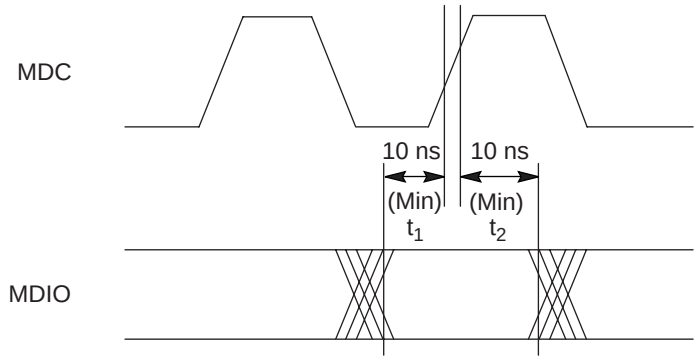


Figure 14. MDIO Timing when OUTPUT by STA Timing Diagram

MDIO Timing when OUTPUT by NetPHY-1 Device

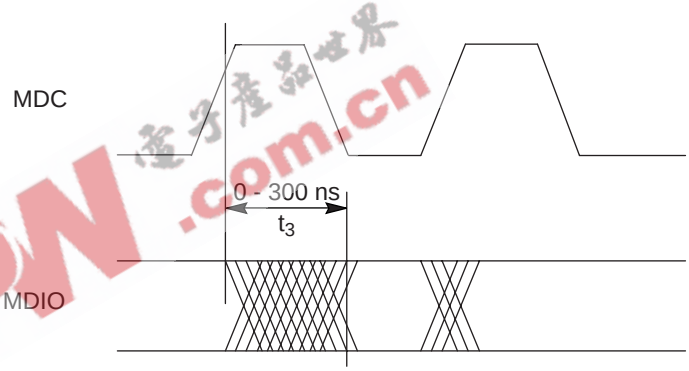


Figure 15. MDIO Timing when OUTPUT by NetPHY-1 Timing Diagram

MII Timing Parameters

Symbol	Parameter	Conditions	Min	Typical	Ma
t1	MDIO Setup Before MDC	When OUTPUT By STA	10	-	-
t2	MDIO Hold After MDC	When OUTPUT By STA	10	-	-
t3	MDC To MDIO Output Delay	When OUTPTU By NetPHY-1 device	0	-	10

MAGNETICS SELECTION GUIDE

The NetPHY-1 device requires a 1:1 ratio for both the receive and the transmit transformers. Refer to Table 2 for transformer requirements. Transformers meeting these requirements are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetics before using them in an application. The transformers listed in Table 2 are electrical equivalent, but may not be pin-to-pin equivalent.

Table 2. Transformer Requirements

Manufacturer	Part Number
Bel Fuse	S558-5999-01
Delta	LF8200, LF8221
HALO Electronics, Inc.	Single Port TG22-3506ND, TD22-3506G1, TG22-S010ND, TG22-S012ND, TG110-S050N2 Quad Port TG110-6506NX, TG110-S450NX, TG110-S452NX
Nano Pulse Inc.	NPI 6181-37, NPI 6120-30, NPI 6120-37 NPI 6170-30
Pulse Engineering	PE-68517, PE-68515, H1019, H1012 ----Single Port H1027, H1028 ---- Dual Port PE-69037, H1001, H1036, H1044 ---- Quad Port
Valor	ST6114, ST6118
YCL	20PMT04, 20PMT05

CRYSTAL SELECTION GUIDE

A crystal can be used to generate the 25
ence clock instead of a crystal oscillator. A
crystal, part number is 00301-00169, MP
25.000000 MHz, ±50 ppm or equivalent m
The crystal must be a fundamental type,
onant. Connect to X1 and X2, shunt each
to ground with an 18pf capacitor (see Figu

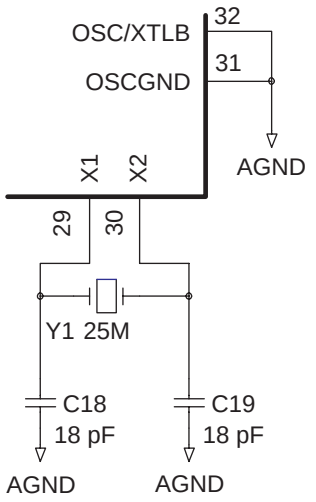
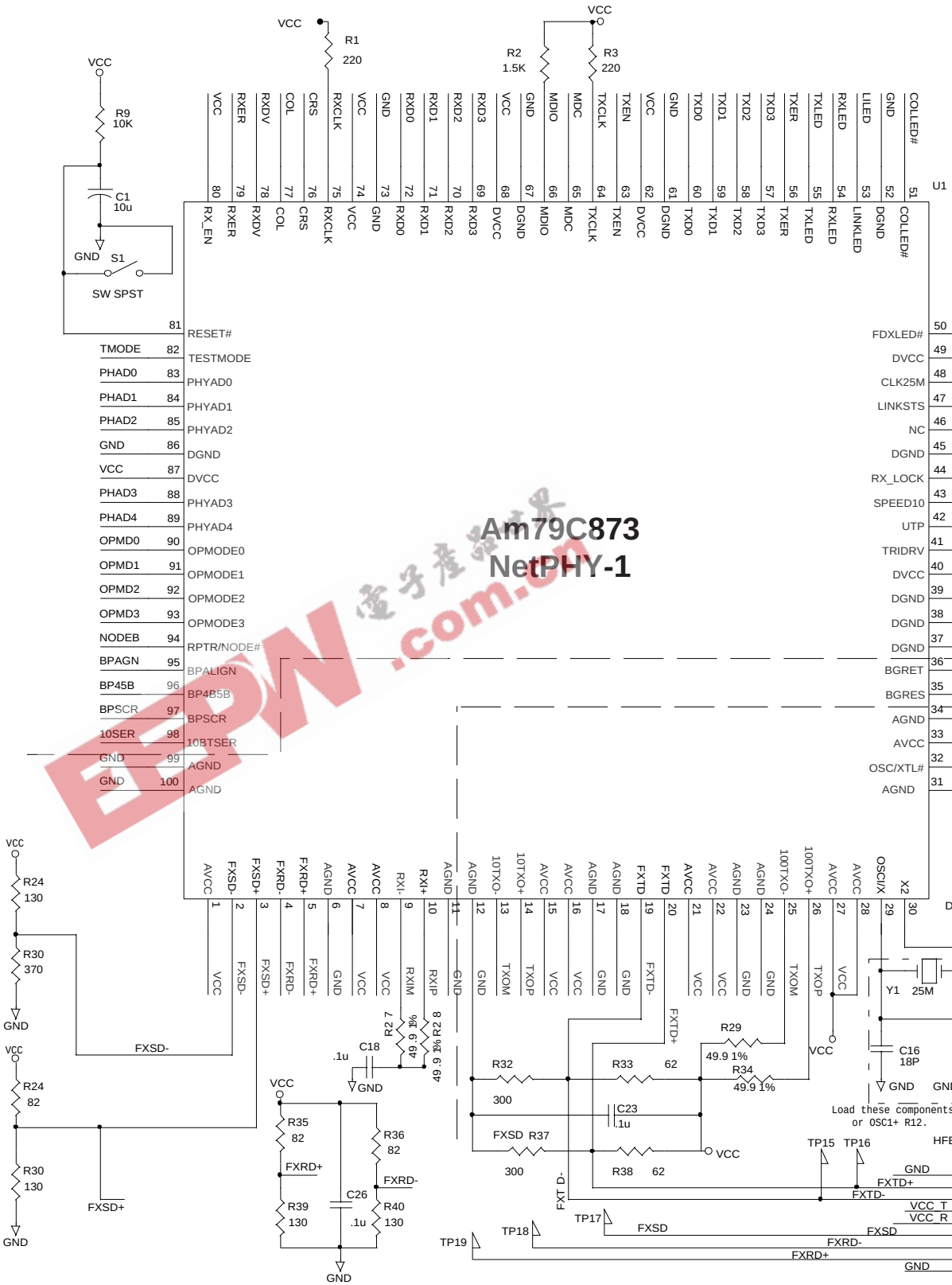


Figure 16. Crystal Circuit Diagr

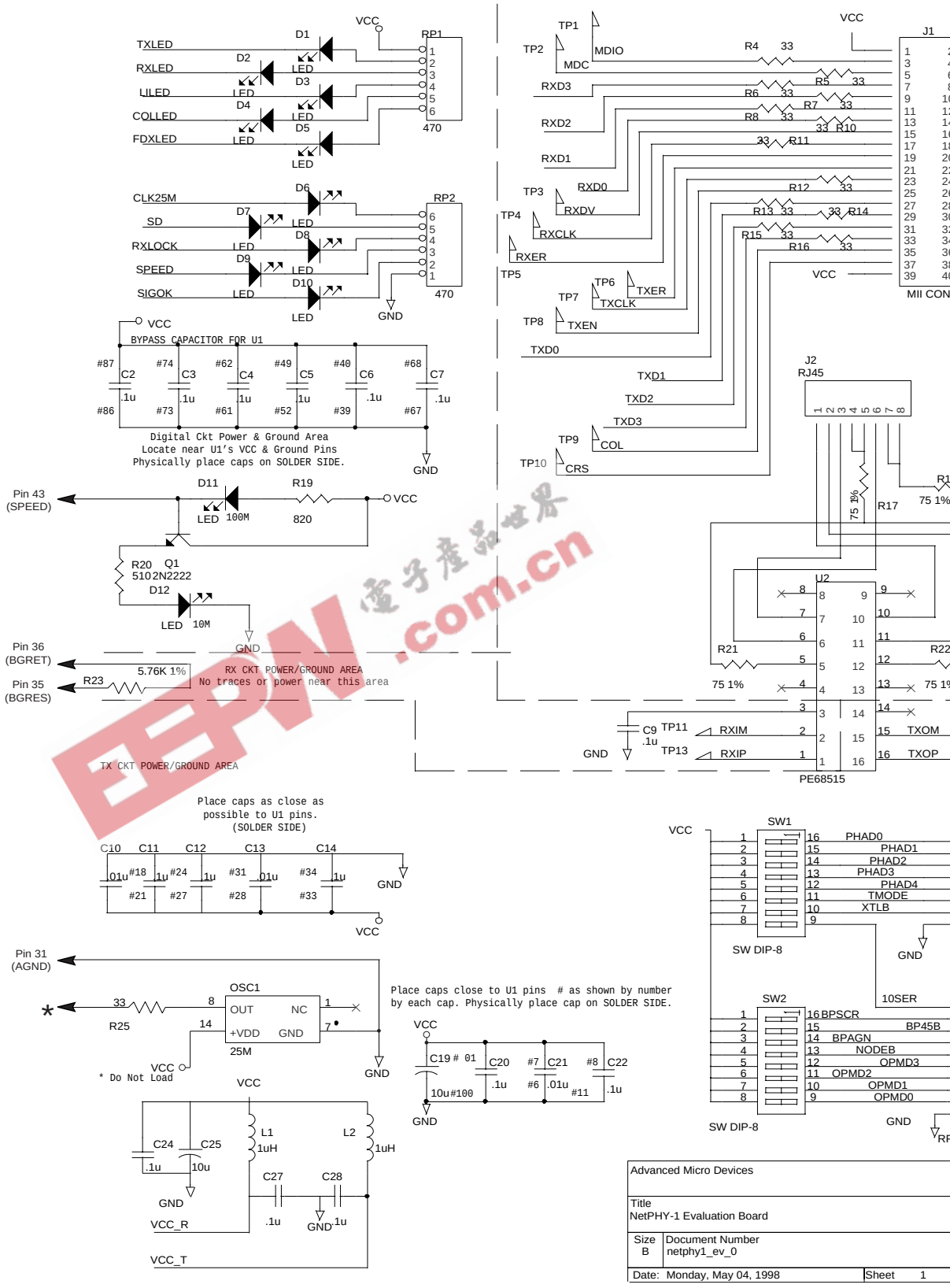
Table 3. Part List for Example Design

Item No	Qty	Reference Number	Part Description
1	11	C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,C11,C13	Capacitor, Decoupling, 0.1 µf, 50 V
2	1	C12	Capacitor, .01 µf, 2KV
3	4	D1,D2,D3,D4	LED, General Purpose
4	1	J1	Connector, RJ45
5	2	L1,L2	Ferrite, Panasonic EXCCL4532U
6	1	OSC1	Oscillator, Crystal, 25 MHz, ±50 ppm
7	2	Q2,Q1	Transistor, NNP, General Purpose, 2N222
8	2	R1,R2	Resistor, 470Ω, 5%
9	1	R3	Resistor, 820Ω, 5%
10	1	R4	Resistor, 33Ω, 5%
11	1	R5	Resistor, 510Ω, 5%
12	1	R6	Resistor, 6.01KΩ, 1%
13	4	R7,R8,R14,R15	Resistor, 49.9Ω, 1%
14	1	R9	Resistor, 1.5KΩ, 5%
15	4	R10,R11,R12,R13	Resistor, 75Ω, 1%
16	2	R17,R16	Resistor, 10KΩ, 5%
17	1	U1	NetPHY-1 device, PHY/Transceiver, 100 p
18	1	U2	Magnetics, Pulse Engineering, PE68515
19	3	R17,R18,R21	Resistor 82Ω, 5%
20	2	R19,R21	Resistor 62Ω, 5%
21	3	R22,R23,R26	Resistor 130Ω, 5%
22	2	R24,R25	Resistor 300Ω, 5%

NetPHY-1 MII Example Schematic



NetPHY-1 MII Example Schematic (Continued)



Advanced Micro Devices

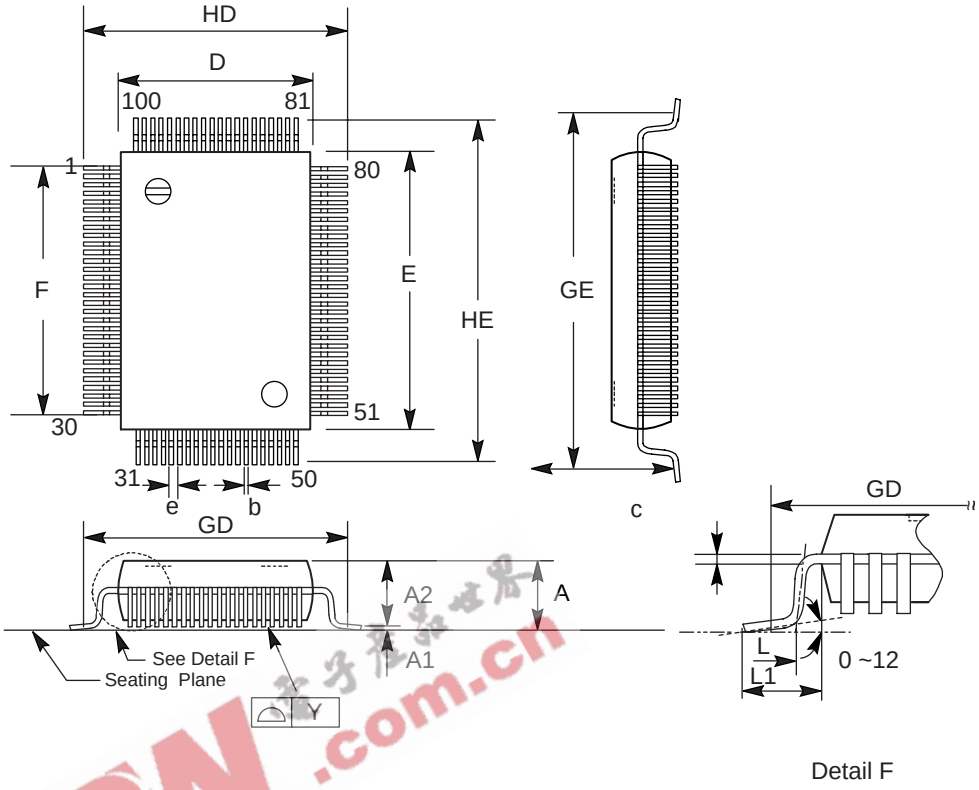
Title
NetPHY-1 Evaluation Board

Size	Document Number
B	netphy1_ev_0

Date: Monday, May 04, 1998 Sheet 1

PHYSICAL DIMENSIONS*

PQR100



Detail F

**For Reference Only*

Symbol	Dimensions In Inches	Dimensions In mm
A	0.130 Max.	3.30 Max.
A1	0.004 Min.	0.10 Min.
A2	0.1120.005	2.85 ±0.13
b	0.012 +0.004 -0.002	0.31 +0.10 -0.05
c	0.006 +0.004 -0.002	0.15 +0.10 -0.05
D	0.551 ±0.005	14.00 ±0.13
E	0.787 ±0.005	20.00 ±0.13
e	0.026 ±0.006	0.65 ±0.15
F	0.742 NOM.	18.85 NOM.
GD	0.693 NOM.	17.60 NOM.
GE	0.929 NOM.	23.60 NOM.
HD	0.740 ±0.012	18.80 ±0.31
HE	0.976 ±0.012	24.79 ±0.31
L	0.047 ±0.008	1.19 ±0.20
L_1	0.095 ±0.008	2.41 ±0.20
y	0.004 Max.	0.15 Max.
q	0∞ ~ 12∞	0∞ ~ 12∞

Notes:

1. *Dimension D & E do not include resin f*
2. *Dimension GD & GE are for PC Bo mount pad pitch design reference only.*
3. *All dimensions are based on metric sys*