Ordering number : EN 5580A

CMOS LSI

LC75833E, 75833W, 75833JE

1/3 Duty General-Purpose LCD Display Drivers

Overview

The LC75833E, LC75833W, and LC75833JE are 1/3-duty general-purpose LCD display drivers that can be used for frequency display in electronic tuners under the control of a microcontroller. The LC75833E and LC75833W can drive an LCD with up to 105 segments directly, the LC75833JE can drive an LCD with up to 93 segments directly. The LC75833E and LC75833W and LC75833JE can also control up to 8 general-purpose output ports. Since the LC75833E, LC75833W, and LC75833JE use separate power supply systems for the LCD drive block and the logic block, the LCD driver block power-supply voltage can be set to any voltage in the range 2.7 to 6.0 volts, regardless of the logic block power-supply voltage.

Features

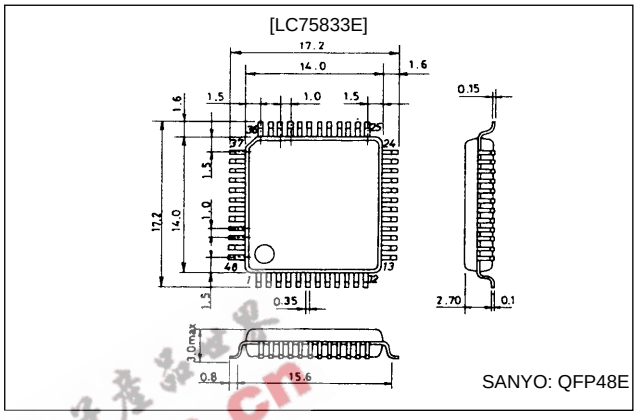
- Supports both 1/3 duty 1/2 bias and 1/3 duty 1/3 bias LCD drive under serial data control.
  LC75833E, LC75833W: up to 105 segments
  LC75833JE: up to 93 segments
  (without the S12, S23, S24, S35 segment output pins from the LC75833E, LC75833W)
- Serial data input supports CCB format communication with the system controller.
- Serial data control of the power-saving mode based backup function and all the segments forced off function
- Serial data control of switching between the segment output port and the general-purpose output port functions
- High generality, since display data is displayed directly without decoder intervention.
- Independent V_{LCD} for the LCD driver block (V_{LCD} can be set to any voltage in the range 2.7 to 6.0 volts, regardless of the logic block power-supply voltage.)
- The $\overline{INH}$ pin can force the display to the off state.
- RC oscillator circuit

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Package Dimensions

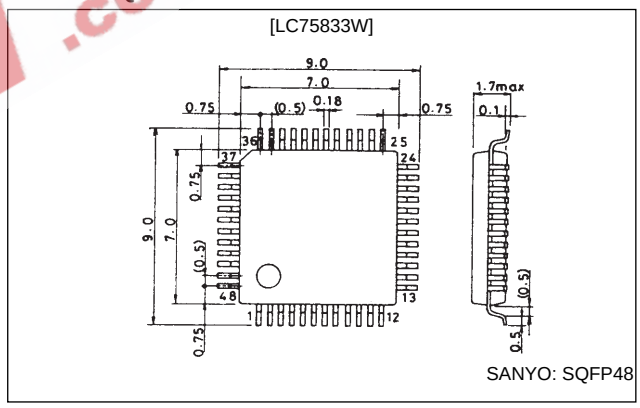
unit: mm

3156-QFP48E



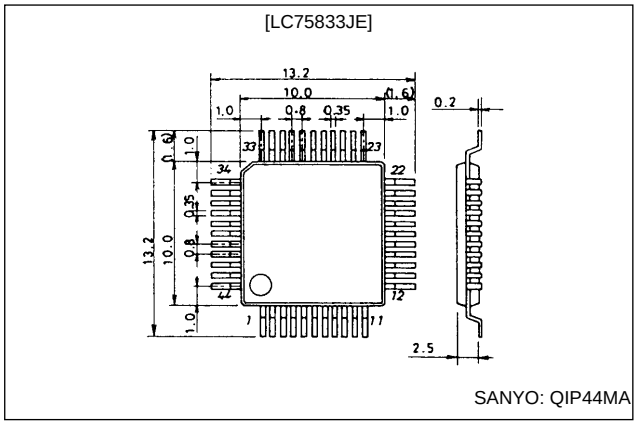
unit: mm

3163A-SQFP48



unit: mm

3148-QFP44MA



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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
	V_{LCD} max	V_{LCD}	–0.3 to +7.0	V
Input voltage	V_{IN} 1	CE, CL, DI, $\overline{INH}$	–0.3 to +7.0	V
	V_{IN} 2	OSC	–0.3 to V_{DD} + 0.3	V
	V_{IN} 3	V_{LCD} 1, V_{LCD} 2	–0.3 to V_{LCD} + 0.3	V
Output voltage	V_{OUT} 1	OSC	–0.3 to V_{DD} + 0.3	V
	V_{OUT} 2	S1 to S35, COM1 to COM3, P1 to P8	–0.3 to V_{LCD} + 0.3	V
Output current	I_{OUT} 1	S1 to S35	300	µA
	I_{OUT} 2	COM1 to COM3	3	mA
	I_{OUT} 3	P1 to P8	5	mA
Allowable power dissipation	Pd max	Ta = 85°C	150	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Note: The LC75833JE does not have the S12, S23, S24, S35 output pins.

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		6.0	V
	V_{LCD}	V_{LCD}	2.7		6.0	V
Input voltage	$V_{LCD}1$	$V_{LCD}1$		2/3 V_{LCD}	V_{LCD}	V
	$V_{LCD}2$	$V_{LCD}2$		1/3 V_{LCD}	V_{LCD}	V
Input high-level voltage	V_{IH}	CE, CL, DI, $\overline{INH}$	0.8 V_{DD}		6.0	V
Input low-level voltage	V_{IL}	CE, CL, DI, $\overline{INH}$	0		0.2 V_{DD}	V
Recommended external resistance	R_{OSC}	OSC		39		kΩ
Recommended external capacitance	C_{OSC}	OSC		1000		pF
Guaranteed oscillation range	f_{OSC}	OSC	19	38	76	kHz
Data setup time	t_{ds}	CL, DI: Figure 2	160			ns
Data hold time	t_{dh}	CL, DI: Figure 2	160			ns
CE wait time	t_{cp}	CE, CL: Figure 2	160			ns
CE setup time	t_{cs}	CE, CL: Figure 2	160			ns
CE hold time	t_{ch}	CE, CL: Figure 2	160			ns
High-level clock pulse width	$t_{øH}$	CL: Figure 2	160			ns
Low-level clock pulse width	$t_{øL}$	CL: Figure 2	160			ns
Rise time	t_r	CE, CL, DI: Figure 2		160		ns
Fall time	t_f	CE, CL, DI: Figure 2		160		ns
$\overline{INH}$ switching time	t_c	$\overline{INH}$, CE: Figure 3	10			µs

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis width	V_H	CE, CL, DI, $\overline{INH}$		0.1 V_{DD}		V
Input high level current	I_{IH}	CE, CL, DI, $\overline{INH}$; V_I = 6.0 V			5.0	µA
Input low level current	I_{IL}	CE, CL, DI, $\overline{INH}$; V_I = 0 V	–5.0			µA
Output high-level voltage	V_{OH} 1	S1 to S35; I_O = –20 µA	V_{LCD} – 0.9			V
	V_{OH} 2	COM1 to COM3; I_O = –100 µA	V_{LCD} – 0.9			V
	V_{OH} 3	P1 to P8; I_O = –1 mA	V_{LCD} – 0.9			V
Output low-level voltage	V_{OL} 1	S1 to S35; I_O = 20 µA			0.9	V
	V_{OL} 2	COM1 to COM3; I_O = 100 µA			0.9	V
	V_{OL} 3	P1 to P8; I_O = 1 mA			0.9	V
Output middle-level voltage*1	V_{MID} 1	COM1 to COM3; 1/2 bias, I_O = ±100 µA	1/2 V_{LCD} – 0.9		1/2 V_{LCD} + 0.9	V
	V_{MID} 2	S1 to S35; 1/3 bias, I_O = ±20 µA	2/3 V_{LCD} – 0.9		2/3 V_{LCD} + 0.9	V
	V_{MID} 3	S1 to S35; 1/3 bias, I_O = ±20 µA	1/3 V_{LCD} – 0.9		1/3 V_{LCD} + 0.9	V
	V_{MID} 4	COM1 to COM3; 1/3 bias, I_O = ±100 µA	2/3 V_{LCD} – 0.9		2/3 V_{LCD} + 0.9	V
	V_{MID} 5	COM1 to COM3; 1/3 bias, I_O = ±100 µA	1/3 V_{LCD} – 0.9		1/3 V_{LCD} + 0.9	V
Oscillator frequency	f_{OSC}	OSC; R_{OSC} = 39 kΩ C_{OSC} = 1000 pF	30.4	38	45.6	kHz
Current drain	I_{DD} 1	V_{DD}; power saving mode			5	µA
	I_{DD} 2	V_{DD}; V_{DD} = 6.0 V, output open, fosc = 38 k Hz		250	500	µA
	I_{LCD} 1	V_{LCD}; power saving mode			5	µA
	I_{LCD} 2	V_{LCD}; V_{LCD} = 6.0 V, output open 1/2 bias, fosc = 38 k Hz		100	200	µA
	I_{LCD} 3	V_{LCD}; V_{LCD} = 6.0 V, output open 1/3 bias, fosc = 38 k Hz		60	120	µA

Note: *1 Excluding the bias voltage generation divider resistors built in the $V_{LCD}1$ and $V_{LCD}2$. (See Figure 1.)

The LC75833JE does not have the S12, S23, S24, S35 output pins.

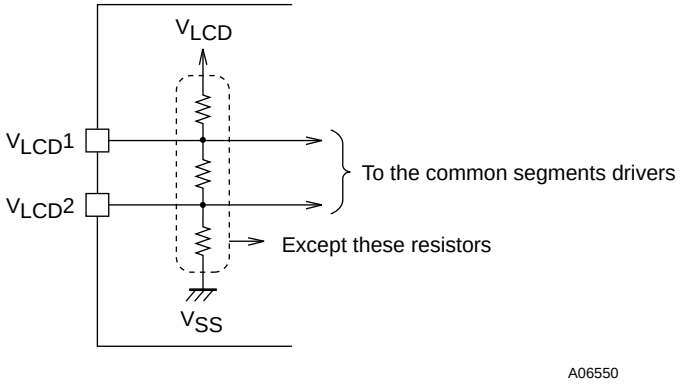
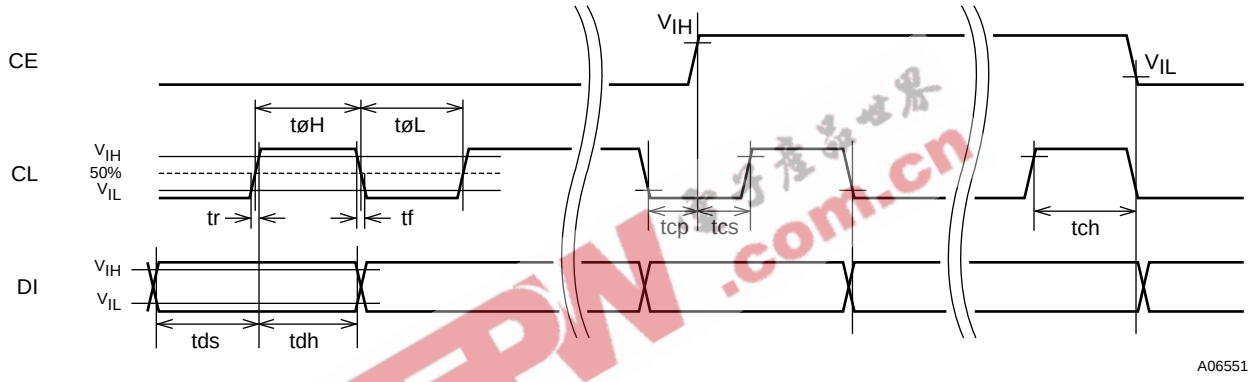


Figure 1

1. When CL is stopped at the low level



2. When CL is stopped at the high level

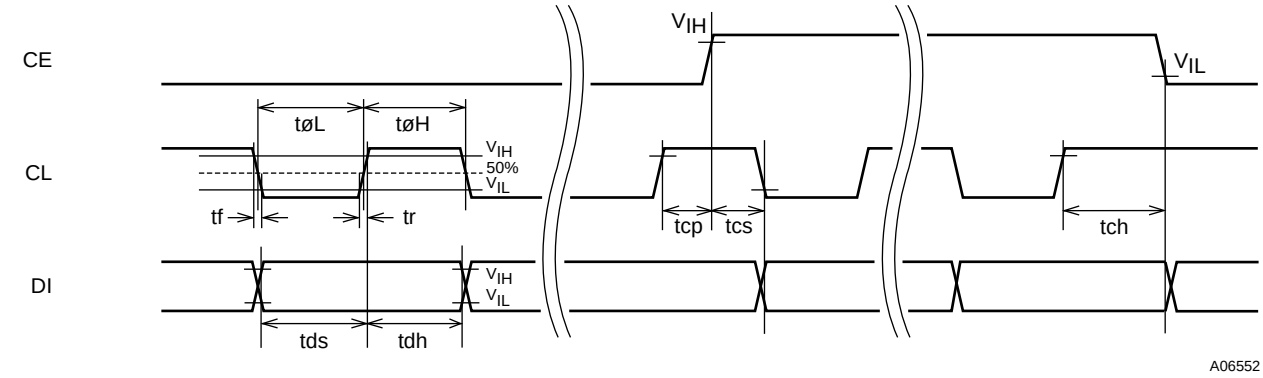
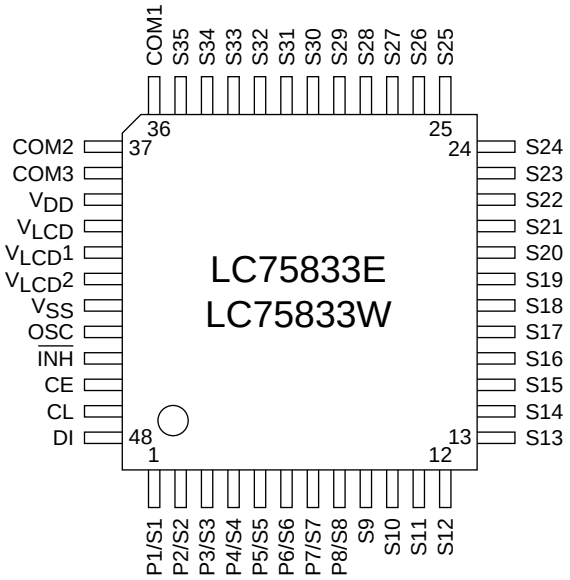


Figure 2

Pin Assignments



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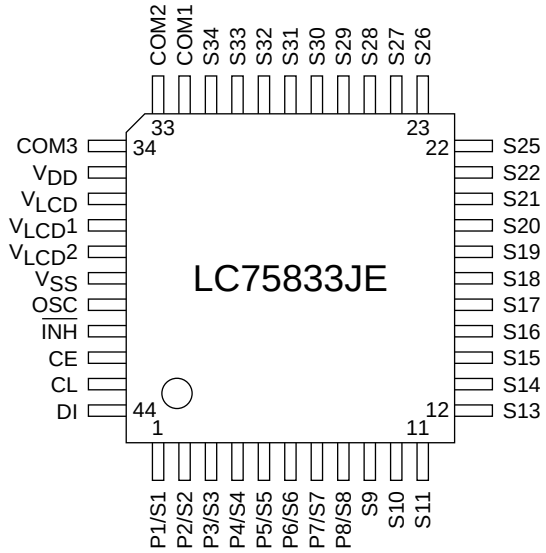

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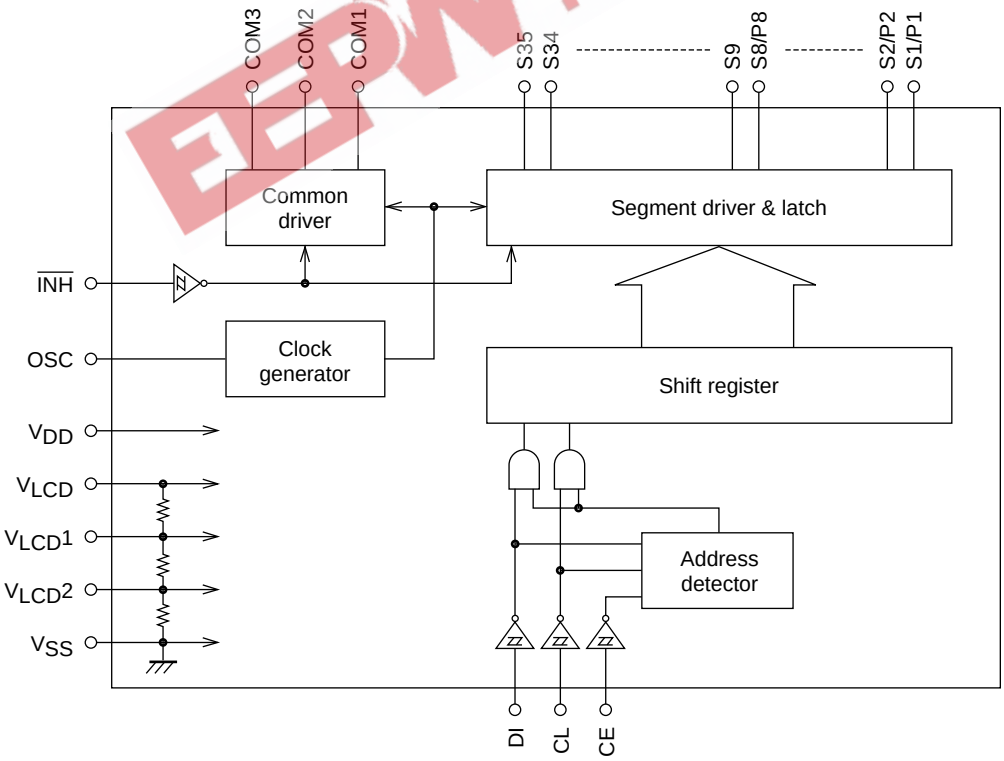
Block Diagram



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Note: The LC75833JE does not have the S12, S23, S24, S35 output pins.

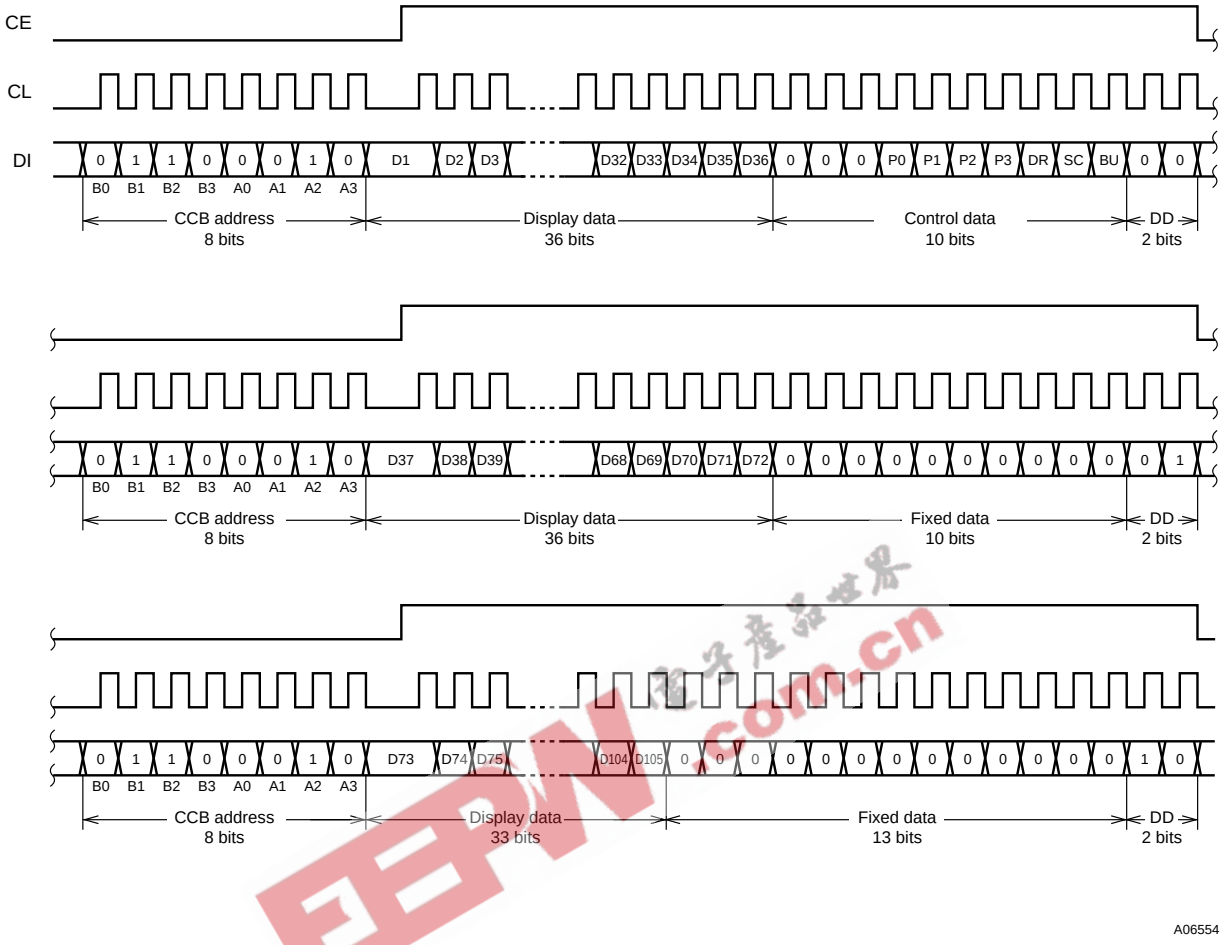
Pin Functions

Pin	Pin No.		Functions		Active	I/O	Handling when unused
	LC75833E, 75833W	LC75833JE					
S1/P1 to S8/P8 S9 to S35	1 to 8 9 to 35	1 to 8 9 to 31	Segment outputs for displaying the display data transferred by serial data input. The pins S1/P1 to S8/P8 can be used as general-purpose output ports when so set up by the control data.		—	O	Open
COM1 COM2 COM3	36 37 38	32 33 34	Common driver outputs. The frame frequency f_O is given by: $f_O = (f_{OSC}/384)$ Hz.		—	O	Open
OSC	44	40	Oscillator connection An oscillator circuit is formed by connecting an external resistor and capacitor to this pin.		—	I/O	V_{DD}
CE CL DI	46 47 48	42 43 44	Serial data transfer inputs. These pins are connected to the control microprocessor.	CE: Chip enable CL: Synchronization clock DI: Transfer data	H ↑ —	I	GND
$\overline{INH}$	45	41	Display off control input •$\overline{INH}$ = low (V_{SS}): Off S1/P1 to S8/P8 = Low (These pins are forcibly set to the segment output port function and fixed at the V_{SS} level.) S9 to S35 = Low (V_{SS}), COM1 to COM3 = Low (V_{SS}) •$\overline{INH}$ = high (V_{DD}): On Note that serial data transfers can be performed when the display is forced off by this pin.		L	I	GND
$V_{LCD}1$	41	37	Used to apply the LCD drive 2/3-bias voltage externally. This pin must be connected to $V_{LCD}2$ when 1/2-bias drive is used.		—	I	Open
$V_{LCD}2$	42	38	Used to apply the LCD drive 1/3-bias voltage externally. This pin must be connected to $V_{LCD}1$ when 1/2-bias drive is used.		—	I	Open
V_{DD}	39	35	Logic block power supply. Provide a voltage in the range 2.7 to 6.0 V.		—	—	—
V_{LCD}	40	36	LCD driver block power supply. Provide a voltage in the range 2.7 to 6.0 V.		—	—	—
V_{SS}	43	39	Ground pin. Connect to ground.		—	—	—

Note: The LC75833JE does not have the S12, S23, S24, S35 output pins.

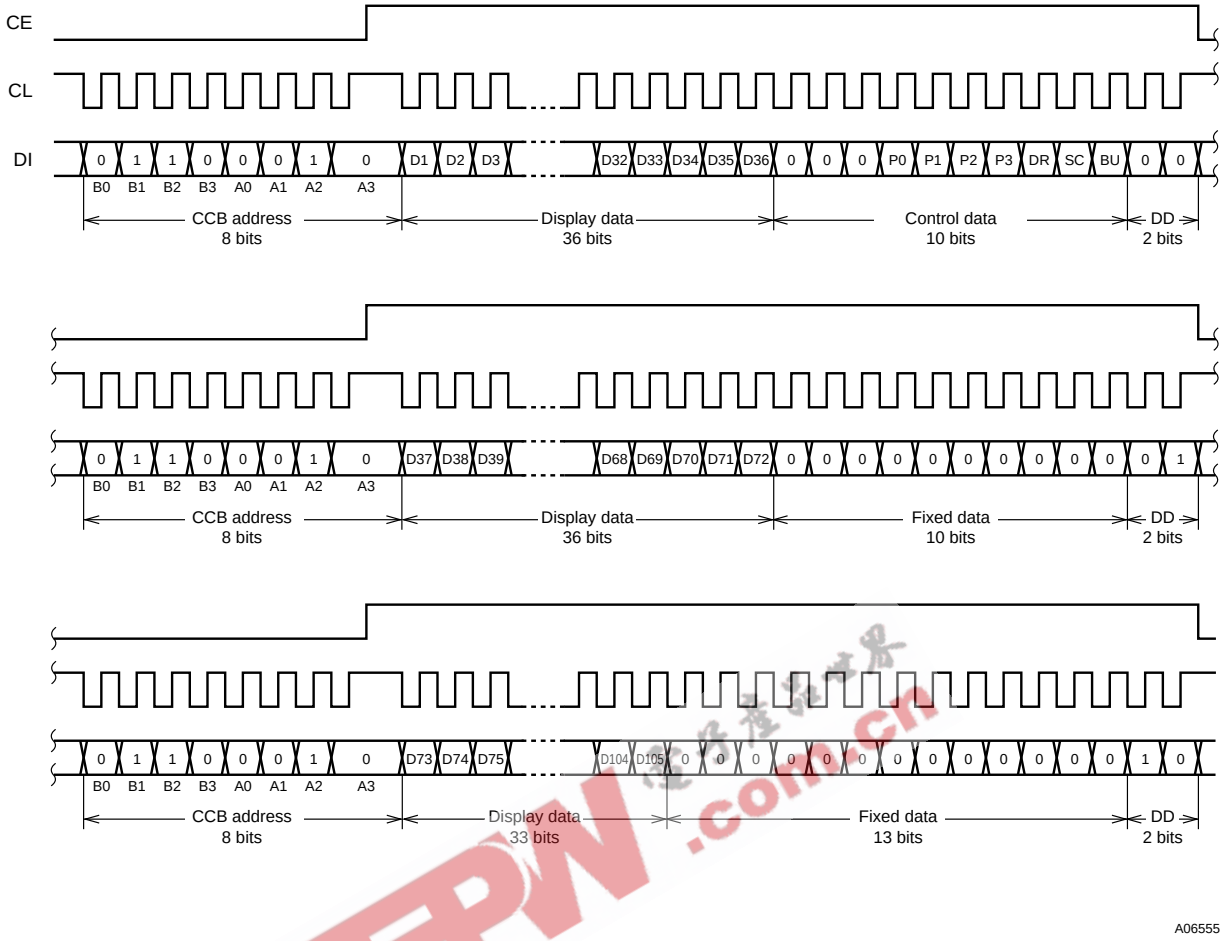
Serial Data Transfer Format

1. When CL is stopped at the low level



Note: DD ... Direction data

2. When CL is stopped at the high level

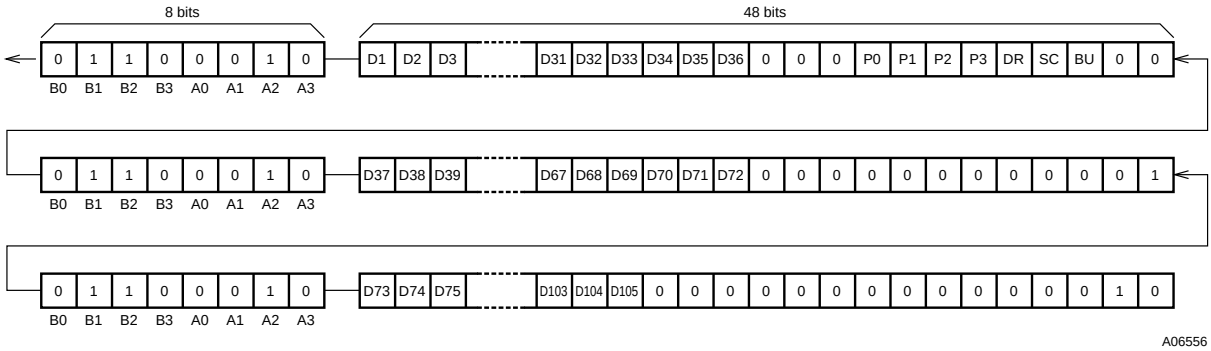


Note: DD ... Direction data

- CCB address.....46H
- D1 to D105.....Display data (At the LC75833JE, the display data D34 to D36, D67 to D72, D103 to D105 must be set to 0.
- P0 to P3 .....Segment output port/general-purpose output port switching control data
- DR .....1/2-bias drive or 1/3-bias drive switching control data
- SC.....Segments on/off control data
- BU .....Normal mode/power-saving mode control data

Serial Data Transfer Examples

- At the LC75833E and LC75833W when 73 or more segments are used, at the LC75833JE when 64 or more segments are used.
  144 bits of serial data must be sent.



Note: At the LC75833JE, the display data D34 to D36, D67 to D72, D103 to D105 must be set to 0.

- At the LC75833E and LC75833W when used with less than 73 segments, at the LC75833JE when used with less than 64 segments.
  Transfer either 48 bits or 96 bits of serial data depending on the number of segments used. However, the serial data shown in the figure below (the display data D1 to D36 and the control data) must be sent.

Note: At the LC75833JE, the display data D34 to D36 must be set to 0.

Control Data Functions

1. P0 to P3: Segment output port/general-purpose output port switching control data.
   These control data bits switch the S1/P1 to S8/P8 output pins between their segment output port and general-purpose output port functions.

Control data				Output pin states							
P0	P1	P2	P3	S1/P1	S2/P2	S3/P3	S4/P4	S5/P5	S6/P6	S7/P7	S8/P8
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0	1	P1	S2	S3	S4	S5	S6	S7	S8
0	0	1	0	P1	P2	S3	S4	S5	S6	S7	S8
0	0	1	1	P1	P2	P3	S4	S5	S6	S7	S8
0	1	0	0	P1	P2	P3	P4	S5	S6	S7	S8
0	1	0	1	P1	P2	P3	P4	P5	S6	S7	S8
0	1	1	0	P1	P2	P3	P4	P5	P6	S7	S8
0	1	1	1	P1	P2	P3	P4	P5	P6	P7	S8
1	0	0	0	P1	P2	P3	P4	P5	P6	P7	P8

Note: Sn (n = 1 to 8): Segment output ports
Pn (n = 1 to 8): General-purpose output ports

Also note that when the general-purpose output port function is selected, the output pins and the display data will have the correspondences listed in the tables below.

Output pin	Corresponding display data
S1/P1	D1
S2/P2	D4
S3/P3	D7
S4/P4	D10

Output pin	Corresponding display data
S5/P5	D13
S6/P6	D16
S7/P7	D19
S8/P8	D22

For example, if the output pin S4/P4 has the general-purpose output port function selected, it will output a high level (V_{LCD}) when the display data D10 is 1, and will output a low level (V_{SS}) when D10 is 0.

2. DR: 1/2-bias drive or 1/3-bias drive switching control data
   This control data bit selects either 1/2-bias drive or 1/3-bias drive.

DR	Drive type
0	1/3-bias drive
1	1/2-bias drive

3. SC: Segments on/off control data
   This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

4. BU: Normal mode/power-saving mode control data
   This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power saving mode (The OSC pin oscillator is stopped, and the common and segment output pins go to the VSS level. However, the S1/P1 to S8/P8 output pins that are set to be general-purpose output ports by the control data P0 to P3 can be used as general-purpose output ports.)

Display Data to Segment Output Pin Correspondence

Segment output pin	COM1	COM2	COM3
S1/P1	D1	D2	D3
S2/P2	D4	D5	D6
S3/P3	D7	D8	D9
S4/P4	D10	D11	D12
S5/P5	D13	D14	D15
S6/P6	D16	D17	D18
S7/P7	D19	D20	D21
S8/P8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54

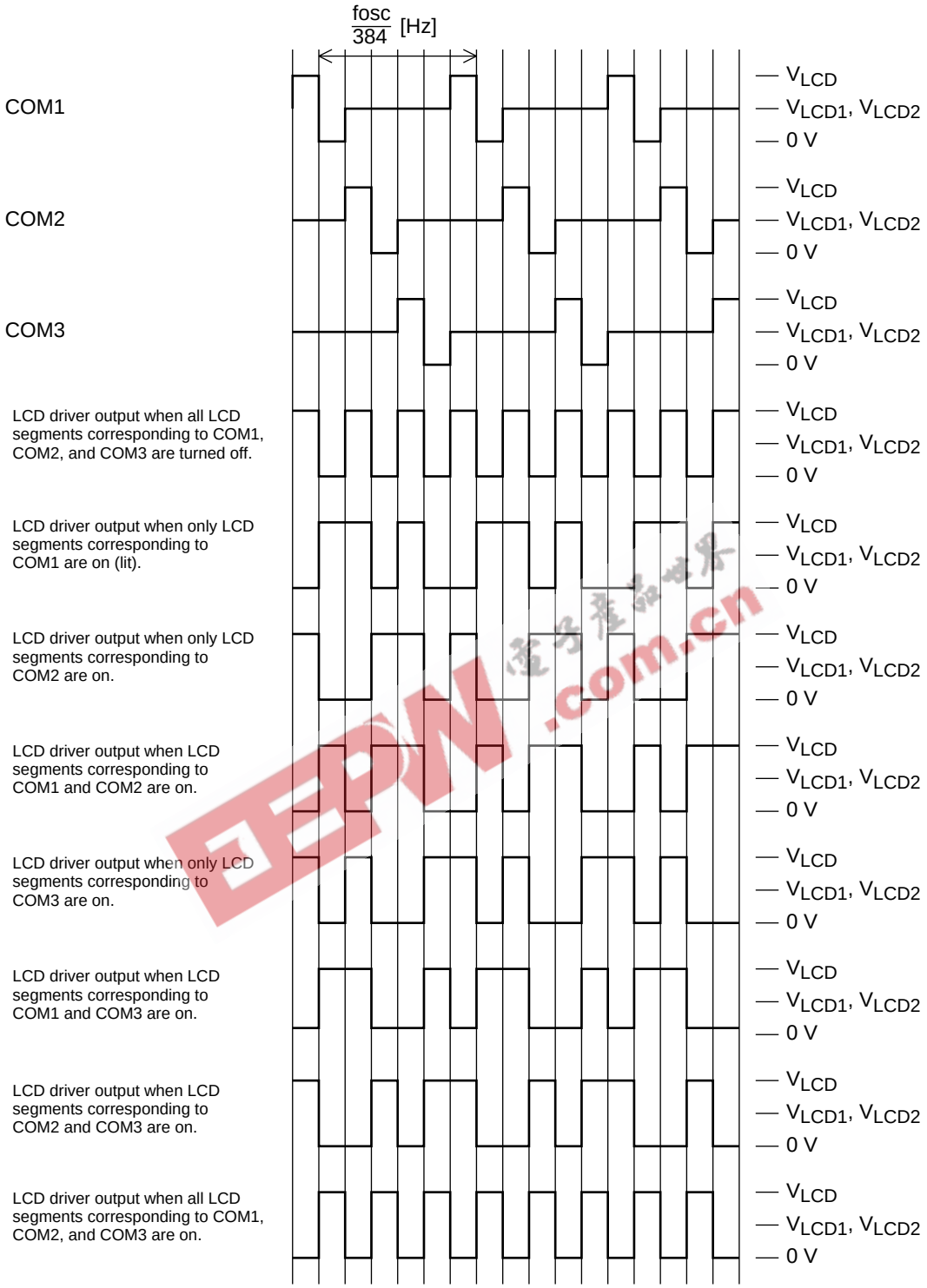
Segment output pin	COM1	COM2	COM3
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D86	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105

Note: This applies to the case where the S1/P1 to S8/P8 output pins are set to be segment output ports.
The LC75833JE do not have the S12, S23, S24, S35 output pins.

For example, the table below lists the segment output states for the S11 output pin.

Display data			Segment output pin (S11) state
D31	D32	D33	
0	0	0	The LCD segments corresponding to COM1 to COM3 are off.
0	0	1	The LCD segments corresponding to COM3 is on.
0	1	0	The LCD segments corresponding to COM2 is on.
0	1	1	The LCD segments corresponding to COM2 and COM3 are on.
1	0	0	The LCD segments corresponding to COM1 is on.
1	0	1	The LCD segments corresponding to COM1 and COM3 are on.
1	1	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	1	The LCD segments corresponding to COM1 to COM3 are on.

1/3-Duty 1/2-Bias Drive Technique



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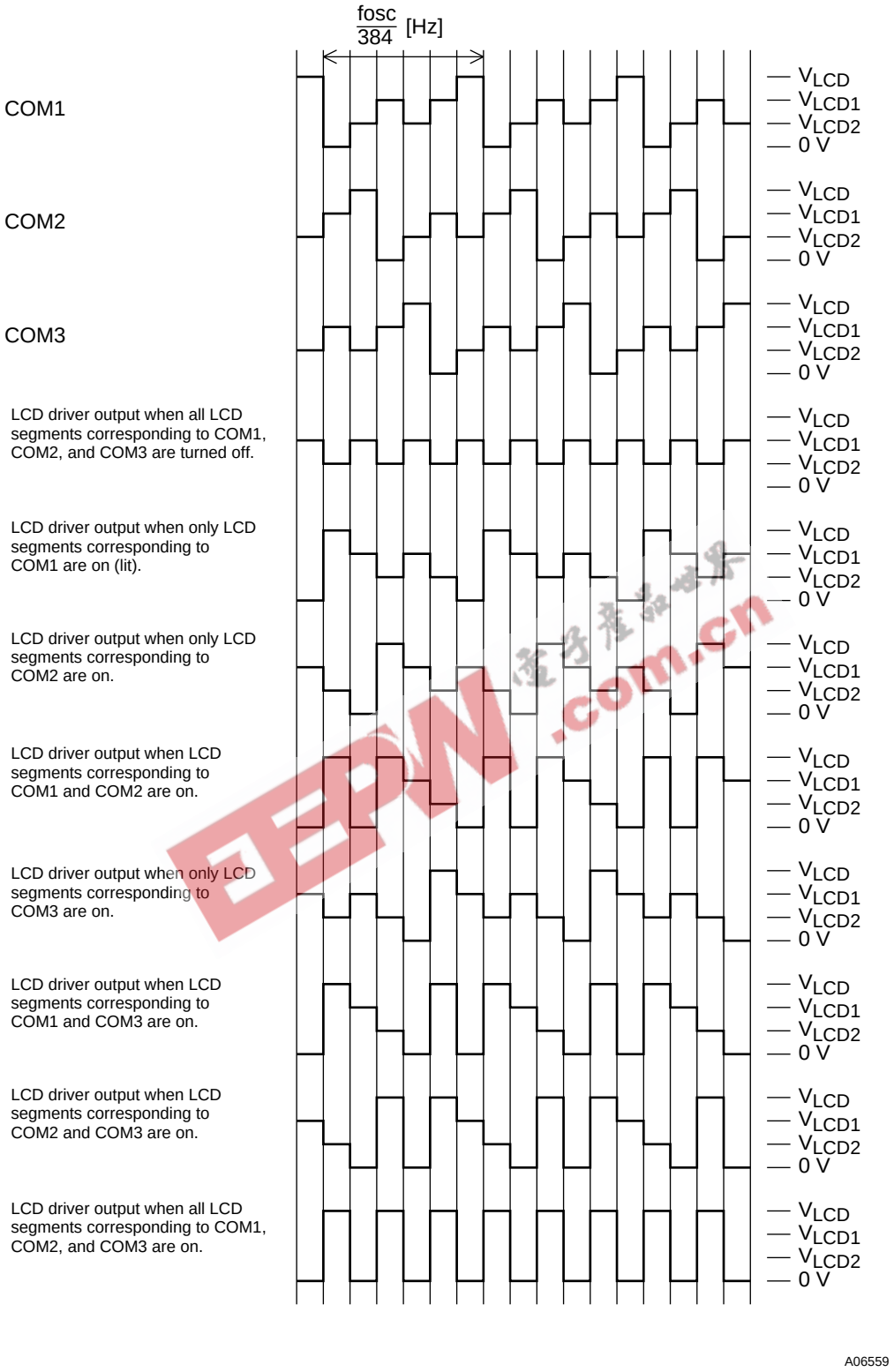
1/3-Duty 1/2-Bias Waveforms

1/3-Duty 1/3-Bias Technique



1/3-Duty 1/3-Bias Waveforms

The $\overline{INH}$ pin and Display Control

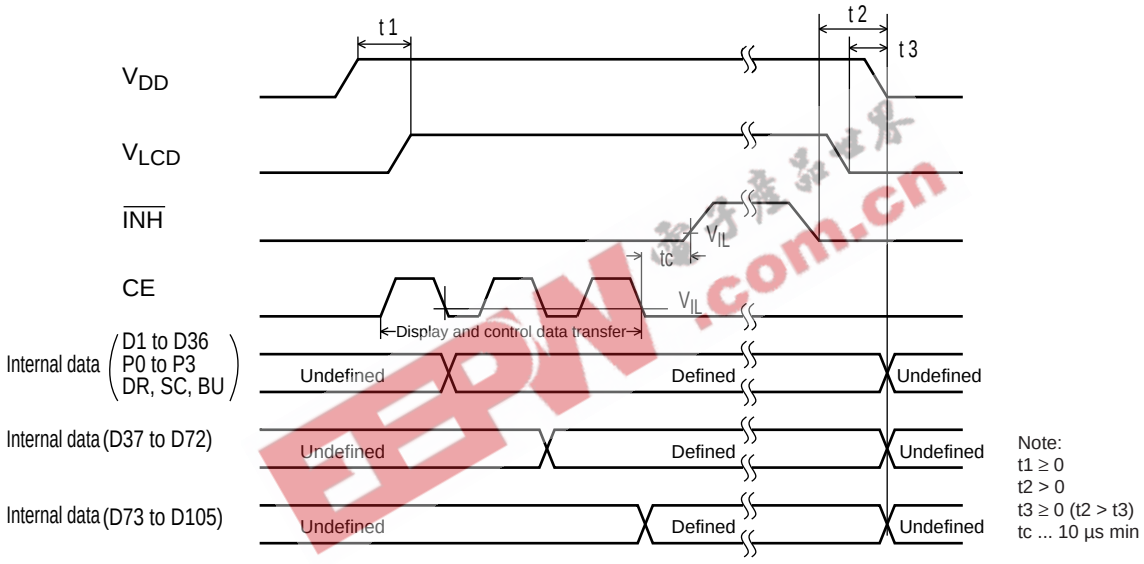
Since the LSI internal data (the display data and the control data) is undefined when power is first applied, applications should set the $\overline{INH}$ pin low at the same time as power is applied to turn off the display (LC75833E, LC75833W: This sets the S1/P1 to S8/P8, S9 to S35, and COM1 to COM3 to the V_{SS} level. LC75833JE: This sets the S1/P1 to S8/P8, S9 to S11, S13 to S22, S25 to S34, and COM1 to COM3 to the V_{SS} level.) and during this period send serial data from the controller. The controller should then set the $\overline{INH}$ pin high after the data transfer has completed. This procedure prevents meaningless displays at power on. (See Figure 3.)

Notes on the Power On/Off Sequences

Applications should observe the following sequence when turning the LC75833E, LC75833W, and LC75833JE power on and off.

- At power on: Logic block power supply (V_{DD}) on → LCD driver block power supply (V_{LCD}) on
- At power off: LCD driver block power supply (V_{LCD}) off → Logic block power supply (V_{DD}) off

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.



Note: At the LC75833JE, the display data D34 to D36, D67 to D72, D103 to D105 must be set to 0.

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Figure 3

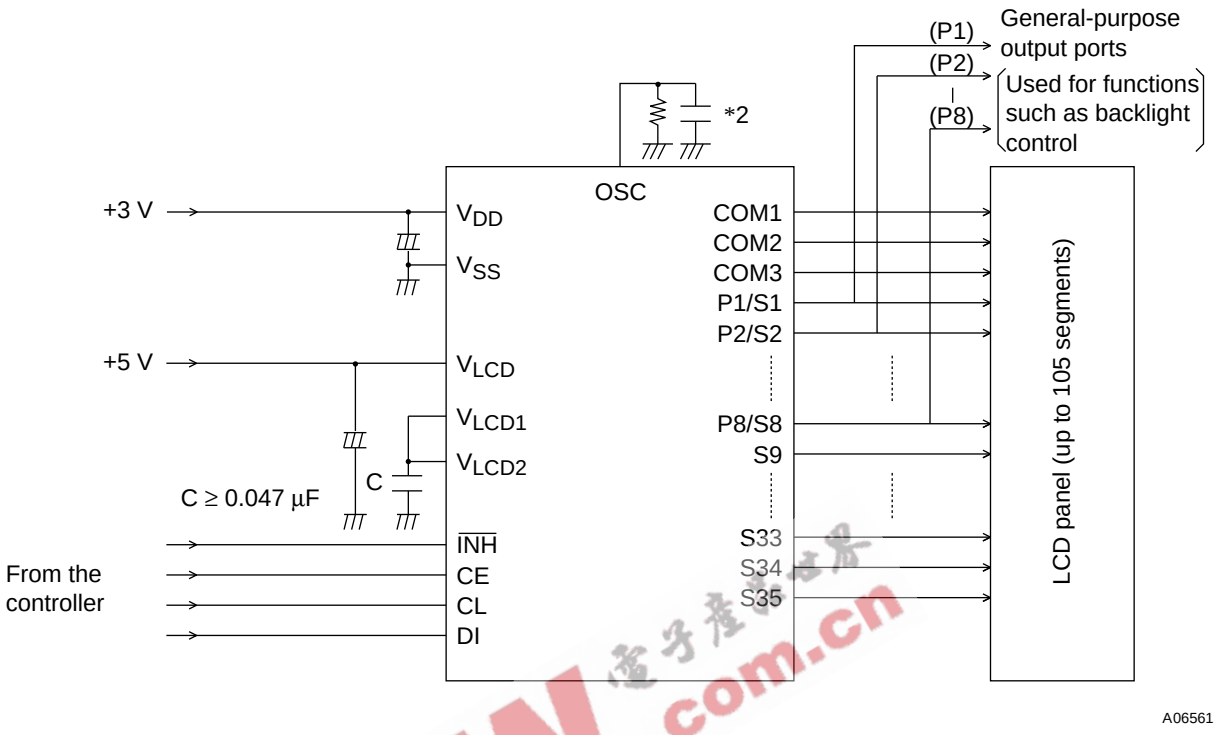
Notes on Controller Transfer of Display Data

Since the LC75833E, LC75833W, and LC75833JE accept display data divided into three separate transfer operations, we recommend that applications transfer all of the display data within a period of less than 30 ms to prevent observable degradation of display quality.

Sample Application Circuit 1

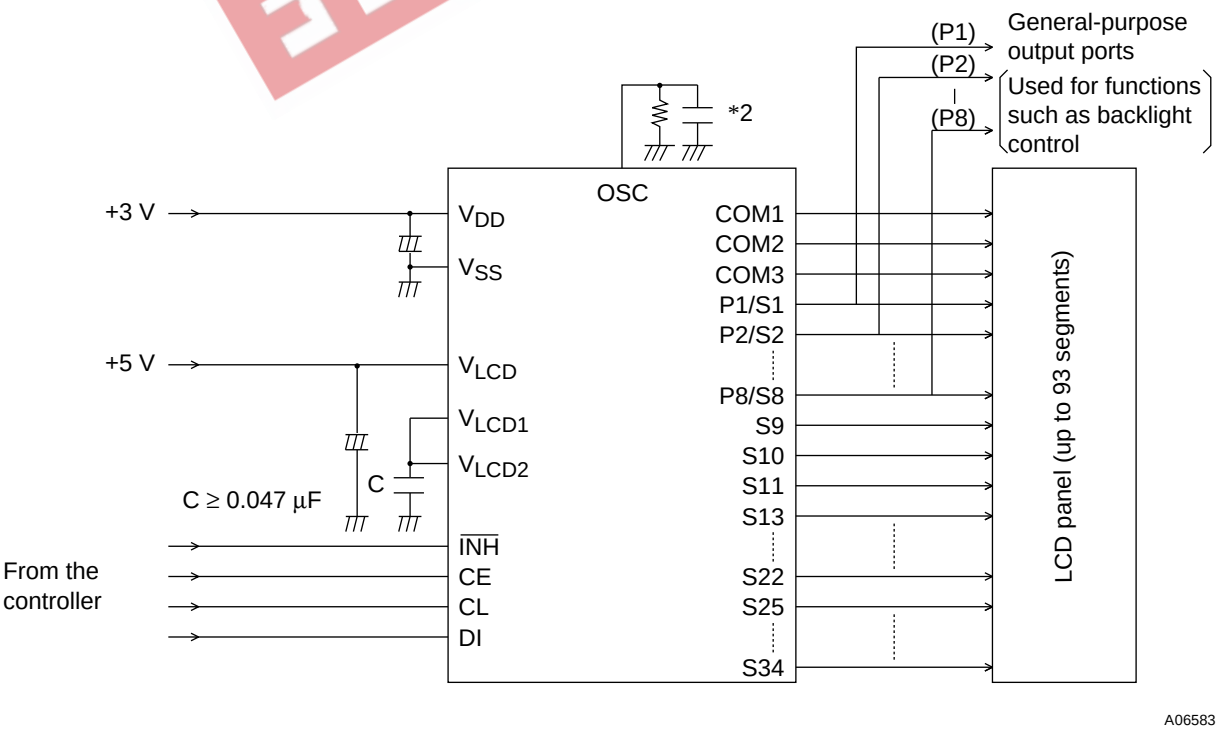
1/2 Bias (for use with normal size panels)

- LC75833E, LC75833W



Note: *2 When a capacitor except the recommended external capacitance (C_{OSC} = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

- LC75833JE

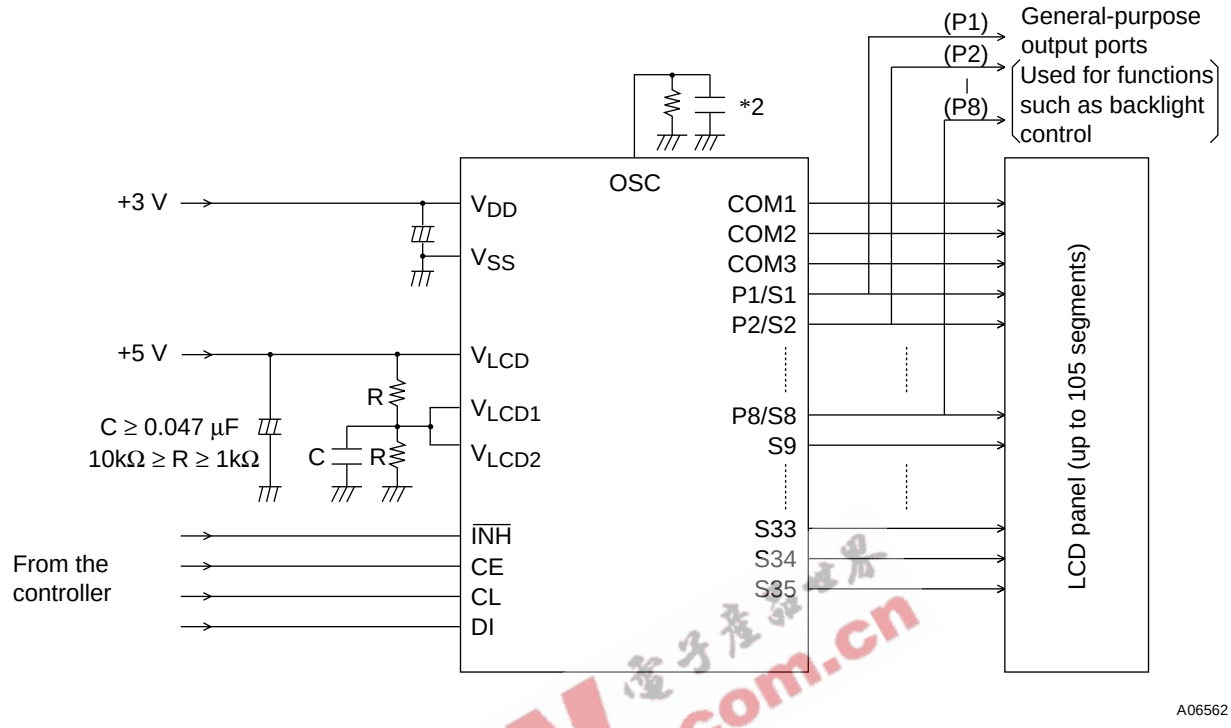


Note: *2 When a capacitor except the recommended external capacitance (C_{OSC} = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

Sample Application Circuit 2

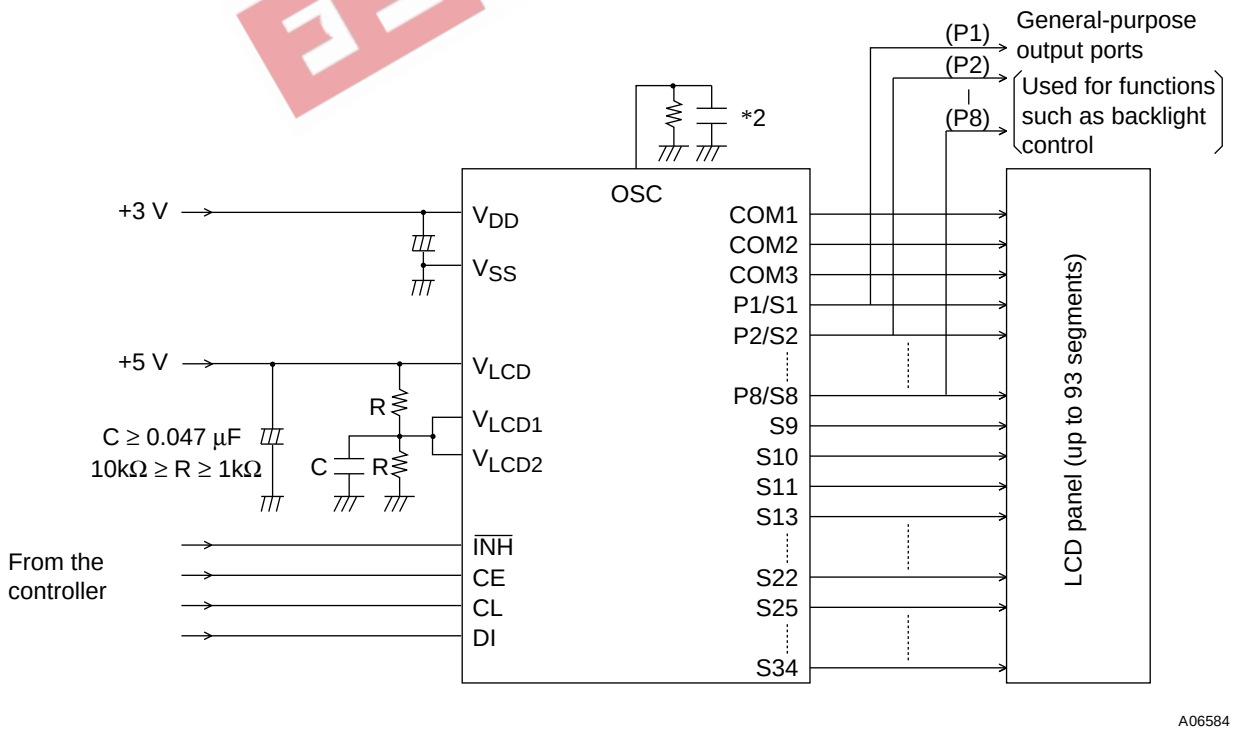
1/2 Bias (for use with large panels)

- LC75833E, LC75833W



Note: *2 When a capacitor except the recommended external capacitance (C_{OSC} = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

- LC75833JE

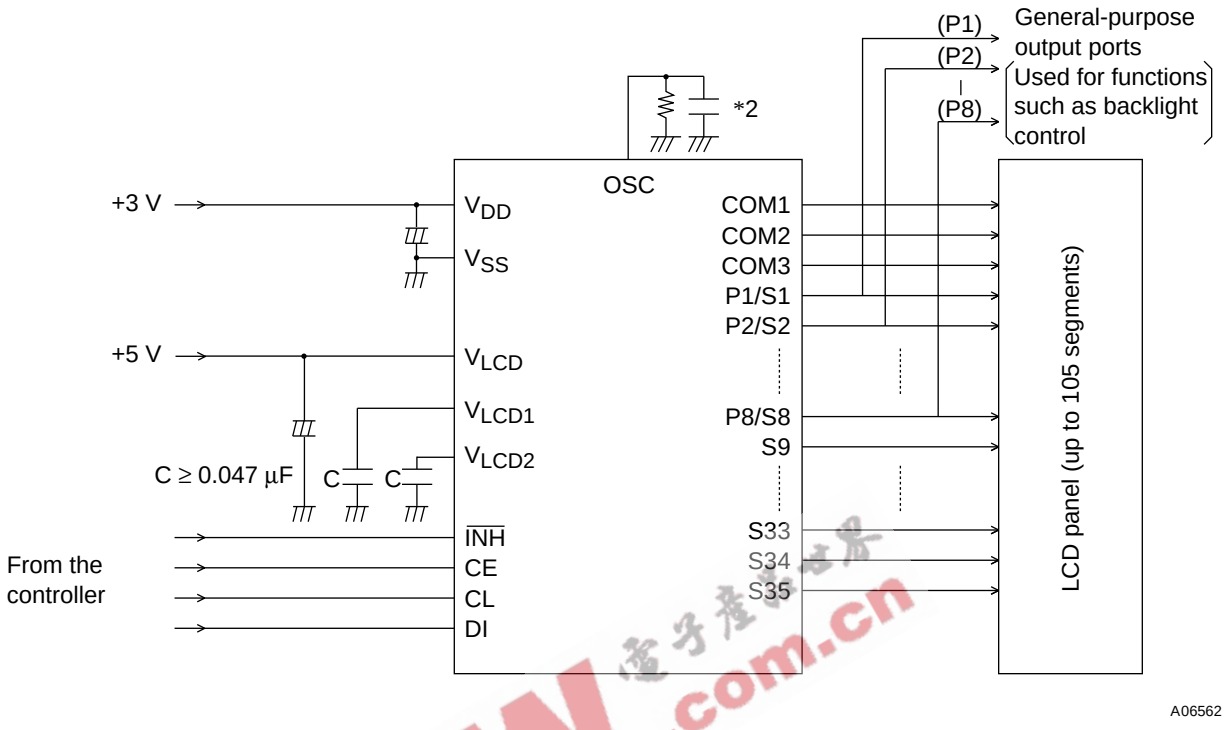


Note: *2 When a capacitor except the recommended external capacitance (C_{OSC} = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

Sample Application Circuit 3

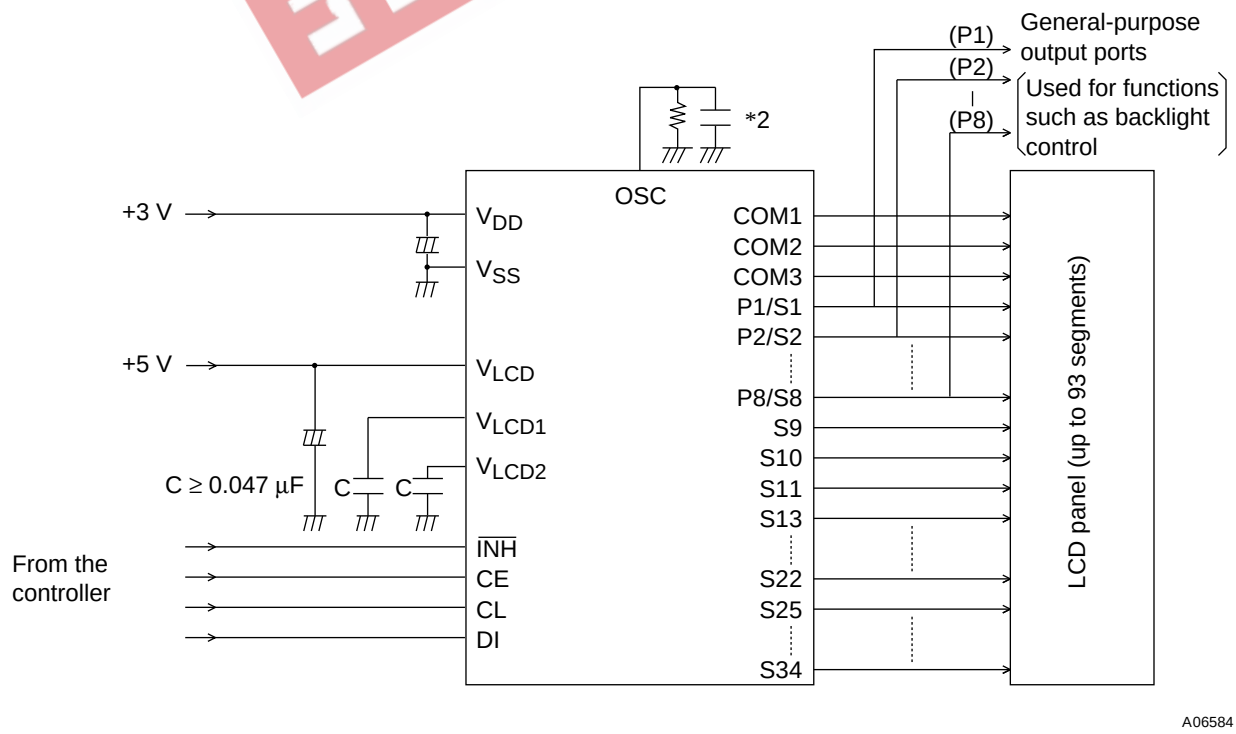
1/3 Bias (for use with normal size panels)

- LC75833E, LC75833W



Note: *2 When a capacitor except the recommended external capacitance (C_{OSC} = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

- LC75833JE

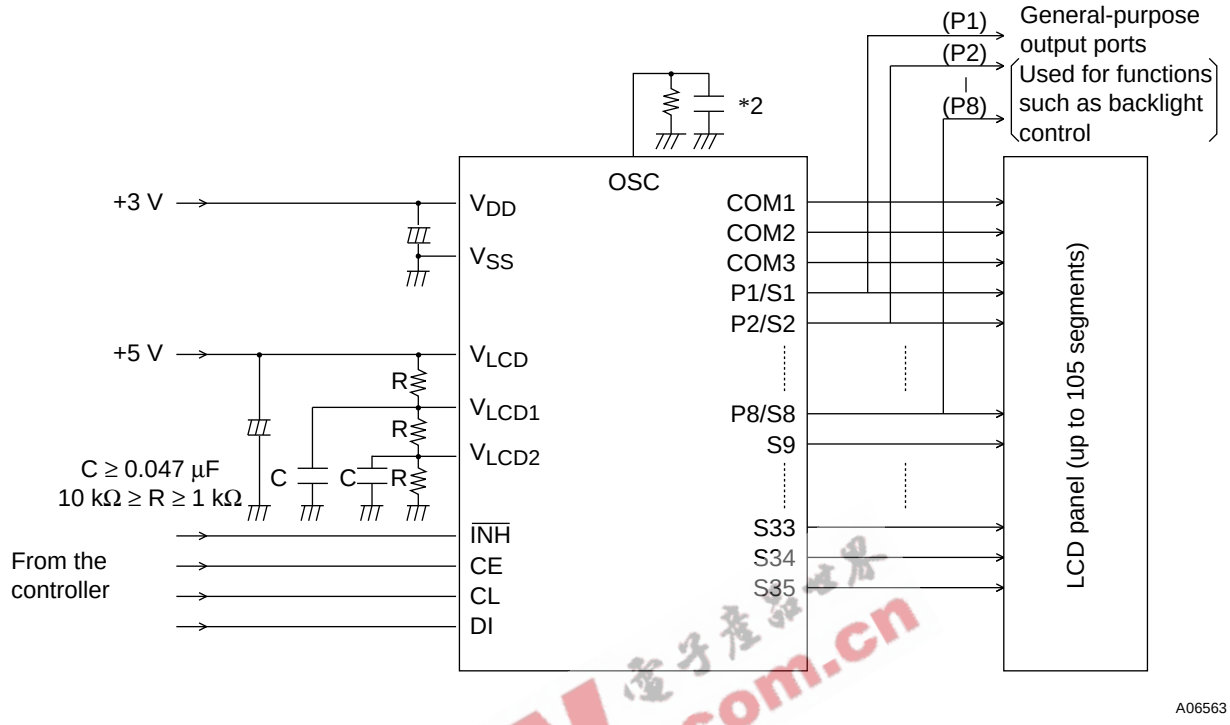


Note: *2 When a capacitor except the recommended external capacitance (C_{OSC} = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

Sample Application Circuit 4

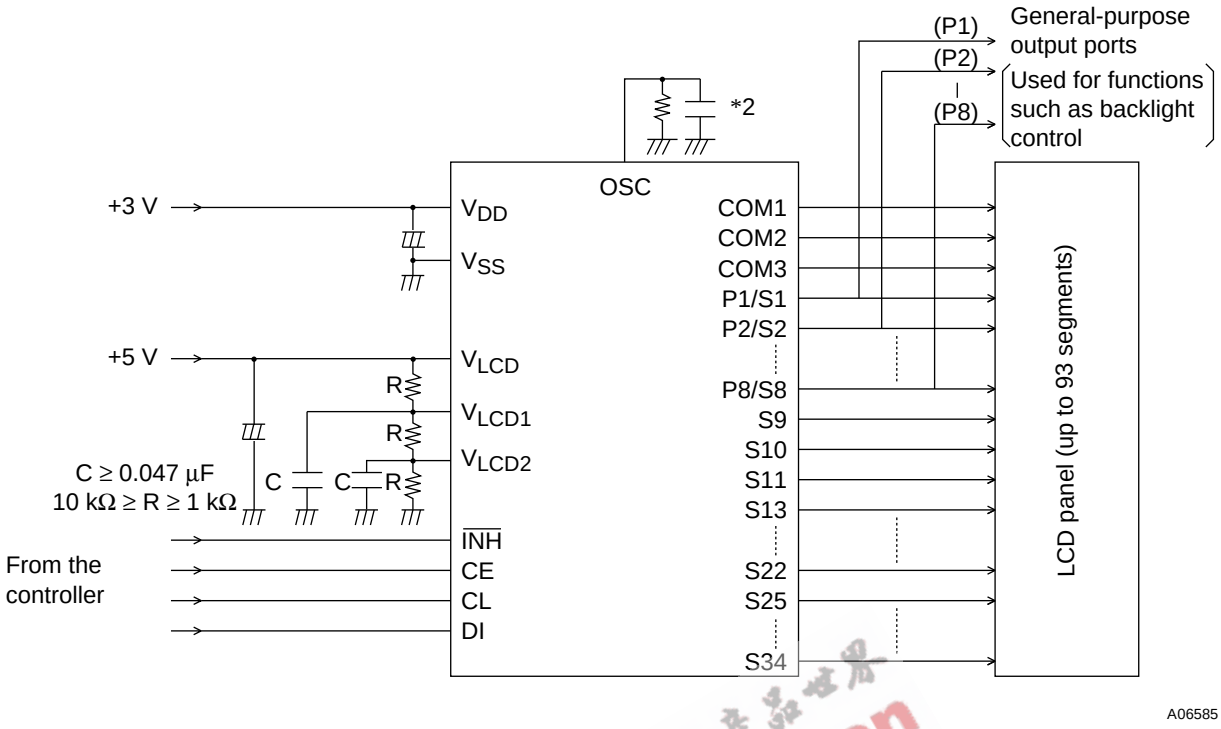
1/3 Bias (for use with large panels)

- LC75833E, LC75833W



Note: *2 When a capacitor except the recommended external capacitance (C_{OSC} = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

• LC75833JE



Note: *2 When a capacitor except the recommended external capacitance (C_{OSC} = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.