Z8E520/C520

1.5 MBPS USB LOW-POWER DEVICE CONTROLLER FOR MULTIPROTOCOL POINTING DEVICES

FEATURES

Part Number	ROM (KB)	RAM (Bytes)	Speed (MHz)
Z8E520 (OTP)	6	176	12
Z8C520 (ROM)	6	176	12

- Six Vectored Interrupts with Fixed Priority
- Processor Speed Dividable by Firmware Control
- Operating Current: 5 mA typical in USB Mode; 2.5 mA typical in Serial Mode (@ 3 MHz); 5 mA typical in PS/2 Mode
- 16 Total Input/Output Pins (Open-Drain/Push-Pull) Configurable
- 6 inputs with 3 level Programmable Reference Comparators
- 16-Bit Programmable Watch-Dog Timer (WDT) with Internal RC Oscillator
- Software Programmable Timers Configurable as:
  - Two 8-Bit Standard Timers and One 16-Bit Standard Timer or
  - One 16-Bit Standard Timer and One 16-Bit Pulse Width Modulator (PWM) Timer
- Identical Masked ROM Version (Z8C520)
- On-Chip Oscillator that accepts a Ceramic Resonator or External Clock
- Hardware Support for PS/2, Serial, USB, and General-Purpose I/O (GPIO)
- Power Reduction Modes:
  - STOP Mode (functionality shut down except SMR)
  - HALT Mode (XTAL still running-peripherals active)
- USB SIE Compliant with USB Spec 1.0
- 4.0 VDC to 6.0 VDC Operating Range @ 0°C to +70°C

GENERAL DESCRIPTION

Zilog's Z8E520 (OTP) and Z8C520 (Masked ROM) microcontrollers are low-power Z8^{Plus} MCUs, designed for the cost-effective implementation of USB and multiprotocol pointing devices.

For applications demanding powerful I/O capabilities, the Z8E520's input and output lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Both 8-bit and 16-bit timers, with a large number of user selectable modes, off-load the system of administering real-time tasks such as counting/timing and I/O data communications.

The microcontroller clock frequency is derived from the system clock by a programmable divider under firmware control.

The device is capable of functioning in four distinct, selectable communications modes: PS/2, RS232, GPIO (General-purpose I/O), and USB. The communications mode determines the functionality of the two special serial communications pins (PB6 and PB7). The device is placed in the required mode when firmware sets the specified mode bit in the communications control register. The firmware interface is similar in all modes. The same buffer area in RAM will accept the data to be transmitted. Up to 8 bytes may be loaded, and the data will actually be transmitted as soon as the appropriate command is issued (setting In Packet Ready in USB mode, for example).

GENERAL DESCRIPTION (Continued)

Power connections follow conventional descriptions at right:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

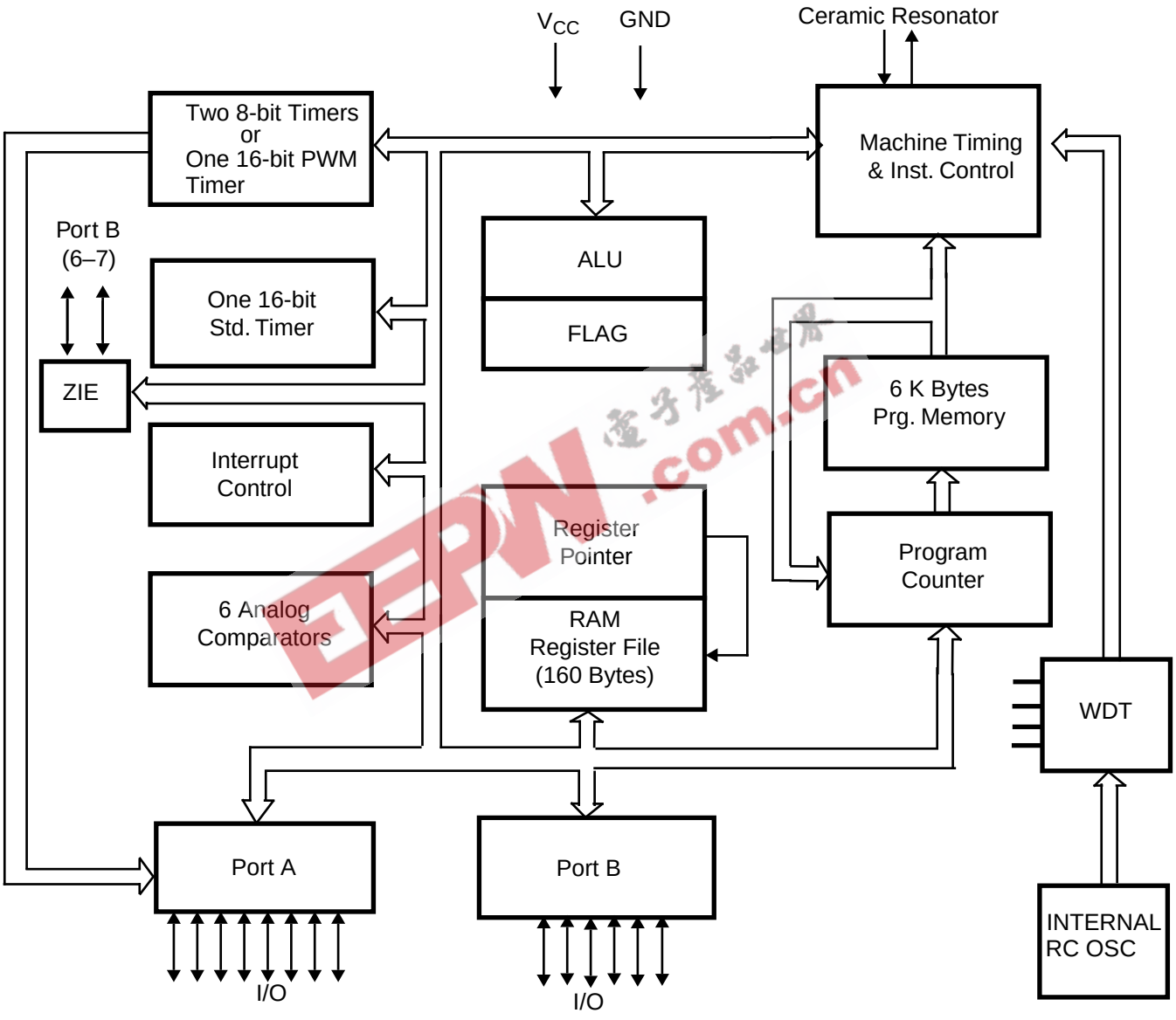


Figure 1. Z8E520 Functional Block Diagram

COMMUNICATION MODES

The Z8E520/C520 allows its user to function in a variety of communication modes. Having this freedom within a single chip opens up many possibilities when utilizing multiple protocol applications. The modes incorporated into the Z8E520/C520 include PS/2, RS232, GPIO, and USB. A description of each mode is detailed below.

PS/2 Mode. The serial baud rate is fixed at 12.5 K baud. Received data is automatically checked for parity and framing errors while HOST abort is supported. The serial communications pins function as PS/2 compatible DATA (PB6) and CLOCK (PB7).

RS232 Mode. The data rate is fixed at 1200 baud. The serial communications pins function as RxD (PB6) and TxD (PB7).

GPIO Mode. In General-Purpose I/O Mode, the serial communications pins function as standard I/O pins, with Input, Output P/P (Push/Pull) and OD (Open Drain) Output.

USB Mode. The Z8E520 includes two bidirectional endpoints that support communications compliant to the USB Specification version 1.0. The serial communications pins function as D– (PB6) and D+ (PB7). The detailed behavior of the SIE is controllable by the firmware, and three separate power states are provided for USB Suspend Mode support (see section below).

USB SUSPEND/RESUME FUNCTIONALITY

Suspend is dedicated through firmware by timing the Activity bit which is set by the SIE.

In Stop Mode, with the WDT disabled, power requirements are minimized. No power is consumed by the voltage regulator, the Z8^{Plus} core, nor differential detector. Only the Stop Mode Recovery (SMR) is enabled, so an input signal or Resume from the host can be detected and used to wake up the microcontroller.

In Stop Mode, with the WDT enabled, slightly more power is consumed, but the device can wake up periodically to perform maintenance and detect a change of state in the application.

USB FUNCTIONAL BLOCK DESCRIPTION

The USB portion of the chip is divided into two areas, the transceiver and the Serial Interface Engine (SIE). The transceiver handles incoming differential signals and “single ended zero (SE0)”. It also converts output data in digital form to differential drive at the proper levels (Figure 2).

The SIE performs all other processing on incoming and out going data, including signal recovery timing, bit stuffing, validity checking, data sequencing, and handshaking to the host. Data flow into and out of the MCU portions are dedicated registers mapped into Expanded Register File Memory.

The USB SIE handles three endpoints (control at Endpoint 0, data into the host from Endpoint 1 and data out from the host as Endpoint 2). All communications are at the 1.5 MB/sec data rate. Endpoint 1 and 2 can be combined as Control EP1.

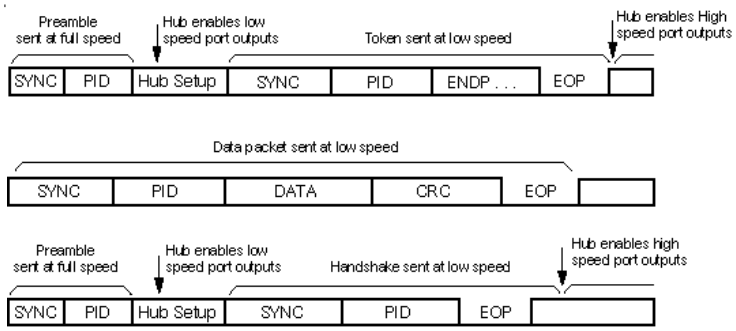


Figure 2. Data To/From Z8E520/C520

PIN IDENTIFICATION

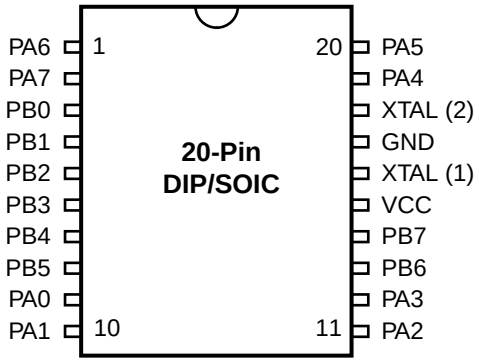


Figure 3. 20-Pin DIP/SOIC Pin Assignments

Table 1. 20-Pin DIP/SOIC Pin Identification

STANDARD Mode

Pin #	Symbol	Function	Direction
1, 2	PA X(6,7)	Digital I/O + I SINK	Bidirectional
3–8	PB X(0–5)	Digital I/O +Comparators	Bidirectional
9–12	PA X(0–3)	Digital I/O	Bidirectional
13–14	PB X (6–7)	Digital I/O + Communications	Bidirectional
15	V_{cc}	Power	
16	XTAL (1)	Clock	
17	GND	Power	
18	XTAL (2)	Clock	
19, 20	PA X(4,5)	Digital I/O + I SINK	Bidirectional

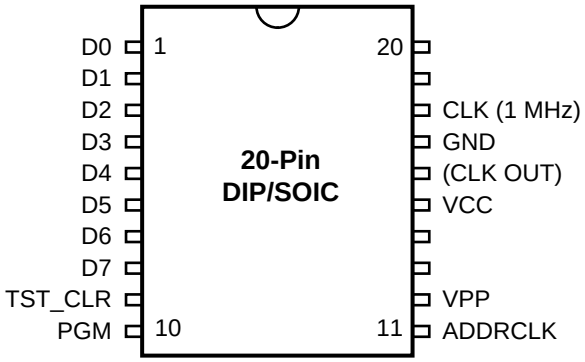


Figure 4. 20-Pin DIP/SOIC Pin Assignments: EPROM Programming Mode

Table 2. 20-Pin DIP/SOIC Pin Identification: EPROM Programming Mode

EPROM PROGRAMMING Mode			
Pin #	**Symbol**	**Function**	**Direction**
1–8	D0–D7	Data Bus	I/O
9	TST_CLR	Reset Internal Address Counter	In
10	PGM	Program Pin	In
11	ADDRCLK	Clock to Address Counter	In
12	V_{PP}	High Voltage to Program Device	Power
13–14		Unused	
15	V_{CC}	Power	Power
16	CLKOUT	Output from Clock Inverter	Out
17	GND	Power Ref	Power
18	CLK	1 MHz to chip	In
19		Unused	
20		Unused	

ABSOLUTE MAXIMUM RATINGS

Total Power Dissipation = V_{DD} x [I_{DD} – (sum of I_{OH})]
+ sum of [(V_{DD} – V_{OH}) x I_{OH}]
+ sum of (V_{0L} x I_{0L})

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 880 mW for the package. Power dissipation is calculated as follows:

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V_{SS}		80	mA	
Maximum Allowable Current into V_{DD}		80	mA	
Maximum Allowable Current into an Input Pin	–600	+600	µA	1
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	2
Maximum Allowable Sink Output Current by Any I/O Pin		25	mA	
Maximum Allowable Source Output Current by Any I/O Pin		25	mA	
Maximum Allowable Sink Output Current by Port A		40	mA	
Maximum Allowable Source Output Current by Port A		40	mA	
Maximum Allowable Sink Output Current by Port B		40	mA	
Maximum Allowable Source Output Current by Port B		40	mA	

Notes:
1. Excludes XTAL pins.
2. Device pin is not at an output Low state.

STANDARD TEST CONDITIONS

The characteristics listed here apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 5).

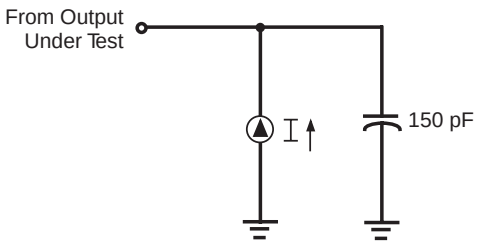


Figure 5. Test Load Diagram

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V; f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Max
Input Capacitance	12 pF
Output Capacitance	12 pF
I/O Capacitance	12 pF

Note: Frequency tolerance ±10%

DC CHARACTERISTICS: USB MODE

V_{CC} = 4.4V – 5.25V

			T_A = 0°C to +70°C				
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
V_{CH}	Clock Input High Voltage		0.7V_{CC}	V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage		V_{SS}–0.3	0.2V_{CC}	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+0.3	V		
V_{IL}	Input Low Voltage		V_{SS}–0.3	0.2V_{CC}	V		
V_{OH}	Output High Voltage (Port A, B)		V_{CC}–0.4		V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage (Port A, B)			0.6	V	I_{OL} = +4.0 mA	4
V_{OL2}	Output Low Voltage (Port A, B)			1.2	V	I_{OL} = +6 mA,	4
V_{OFFSET}	Comparator Input Offset Voltage			25.0	mV		
I_{IL}	Input Leakage		–1.0	2.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage		–1.0	2.0	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		V_{SS}–0.3	V_{CC} –1.0	V		
I_{CC}	Supply Current	6.0V	5.25	6.0	mA	@ 6 MHz (Internal open drain)	1,2
I_{CC1}	HALT Mode	6.0V		3.5	mA	@ 6 MHz (no CPU; RC/WDT & Detect; D+/D–; I/O active)	1,2
I_{CC2}	Stop Current			60	µA		
I_{CC3}	Stop Current w/o RC/WDT			40	µA		
D+, D–	Differential Signaling		D– > D+	D+ > D–	mV	@ >200 mV Difference	3

Notes:

1. All outputs unloaded, I/O pins floating, and all inputs are at V_{CC} or V_{SS} level.
2. CL1 = CL2 = 22 pF
3. Except for SE0 for EOP and Reset (see 7.1.4 of USB Specification)
4. General-Purpose I/O Mode.

DC CHARACTERISTICS: PS/2 MODE

V_{CC} = 4.5V – 5.5V

			T_A = 0°C to +70°C				
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
V_{CH}	Clock Input High Voltage		0.7V_{CC}	V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage		V_{SS}–0.3	0.2V_{CC}	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+0.3	V		
V_{IL}	Input Low Voltage		V_{SS}–0.3	0.2V_{CC}	V		
V_{OH}	Output High Voltage		V_{CC}–0.4		V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage			0.6	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage			1.2	V	I_{OL} = +6 mA,	
V_{OFFSET}	Comparator Input Offset Voltage			25.0	mV		
I_{IL}	Input Leakage		–1.0	2.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage		–1.0	2.0	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		V_{SS}–0.3	V_{CC} –1.0	V		
I_{CC}	Supply Current	5.5V		6.0	mA	@ 6 MHz	1,2
I_{CC1}	HALT Current	5.5V		3.5	mA	@ 6 MHz (no CPU; no SIE)	1,2
I_{CC2}	Stop Current			60	µA		
I_{CC3}	Stop Current w/o RC/WDT			40	µA		

Notes:

1. All outputs unloaded, I/O pins floating, and all inputs are at V_{CC} or V_{SS} level.
2. CL1 = CL2 = 22 pF.

DC CHARACTERISTICS: RS232 MODE

V_{CC} = 4.0V – 6.0V

			T_A = 0°C to +70°C				
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
V_{CH}	Clock Input High Voltage		0.7V_{CC}	V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage		V_{SS}–0.3	0.2V_{CC}	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+0.3	V		
V_{IL}	Input Low Voltage		V_{SS}–0.3	0.2V_{CC}	V		
V_{OH}	Output High Voltage		V_{CC}–0.4		V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage			0.6	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage			1.2	V	I_{OL} = +6 mA,	
V_{OFFSET}	Comparator Input Offset Voltage			25.0	mV		
I_{IL}	Input Leakage		–1.0	2.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage		–1.0	2.0	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		V_{SS}–0.3	V_{CC} –1.0	V		
I_{CC}	Supply Current	6.0V		4.0	mA	@ 3 MHz (6 MHz/2)	1,2
I_{CC1}	HALT Mode	6.0V		3.5	mA	@ 3 MHz	1,2
I_{CC2}	Stop Current			60	µA		
I_{CC3}	Stop Current w/o RC/WDT			40	µA		

Notes:

1. All outputs unloaded, I/O pins floating, and all inputs are at V_{CC} or V_{SS} level.
2. CL1 = CL2 = 22 pF.

DC CHARACTERISTICS: I/O MODE

V_{CC} = 4.0V – 6.0V

			T_A = 0°C to +70°C				
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
V_{CH}	Clock Input High Voltage		0.7V_{CC}	V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage		V_{SS}–0.3	0.2V_{CC}	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+0.3	V		
V_{IL}	Input Low Voltage		V_{SS}–0.3	0.2V_{CC}	V		
V_{OH}	Output High Voltage		V_{CC}–0.4		V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage			0.6	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage			1.2	V	I_{OL} = +6 mA,	
V_{OFFSET}	Comparator Input Offset Voltage			25.0	mV		
I_{IL}	Input Leakage		–1.0	2.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage		–1.0	2.0	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		V_{SS}–0.3	V_{CC} –1.0	V		
I_{CC}	Supply Current	6.0V		6.0	mA	@ 6 MHz	1,2
I_{CCA}		5.5V		6.0	mA	@ 5.5V	1,2
I_{CCB}				4.0	mA	@ 6.0V (6 MHz/2)	
I_{CC1}	HALT w/ RC and WDT			60	µA		
I_{CC2}				50	µA		

Notes:

1. All outputs unloaded, I/O pins floating, and all inputs are at V_{CC} or V_{SS} level.
2. CL1 = CL2 = 22 pF.

AC ELECTRICAL CHARACTERISTICS

Timing Diagram

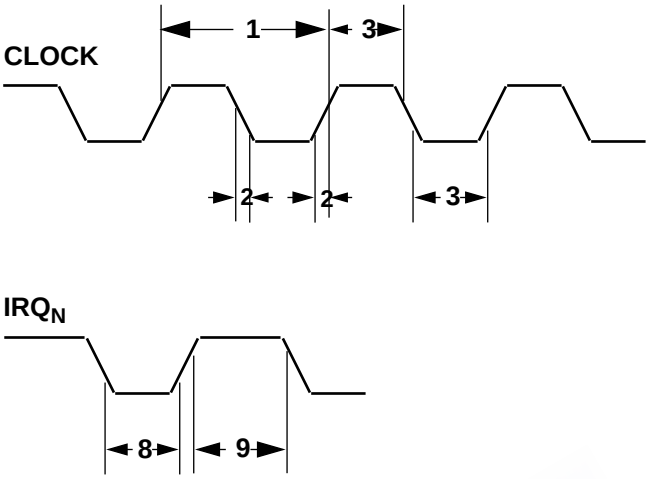


Figure 6. AC Electrical Timing Diagram

Timing Table

			T_A = 0°C to +70°C 6 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	83	DC	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times		5	ns	1
3	TwC	Input Clock Width	37		ns	1
4	TwTinL	Timer Input Low Width	70		ns	1
5	TwTinH	Timer Input High Width	2.5TpC			1
6	TpTin	Timer Input Period	4TpC			1
7	TrTin	Timer Input Rise & Fall Timer		100	ns	1
8	TwIL	Int. Request Low Time	70		ns	1,2
9	TwIH	Int. Request Input High Time	3TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	100TpC		ns	
11	Tost	Oscillator Start-Up Time		0.5	ms	
12	Twdt	Watch-Dog Timer	1000		ms	
13	D+, D–	Differential Rise and Fall Times (USB Mode)	70	300	nS	3
14	POR	Power supply; POR rate/Volt level				
15	TrC	RC Clock Period (internal)	12.5	50	µsec	4

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request
3. See USB Specification 7.1.1.2
4. Corresponds to frequencies of 80 KHz to 20 KHz

PIN FUNCTIONS

Port A. Port A (4–7) includes a Sink configuration. Port A (3–0) has a Switch configuration.

In Sink, the options include input wakeup, bidirectional, push-pull or open drain configurations (Figure 7). The Sink is programmable from 0–15 mA (in 1 mA increments).

In Switch, the options also include input wakeup, bidirectional, push-pull or open drain configurations (Figure 8). The only difference between the two is the programmable Sink option.

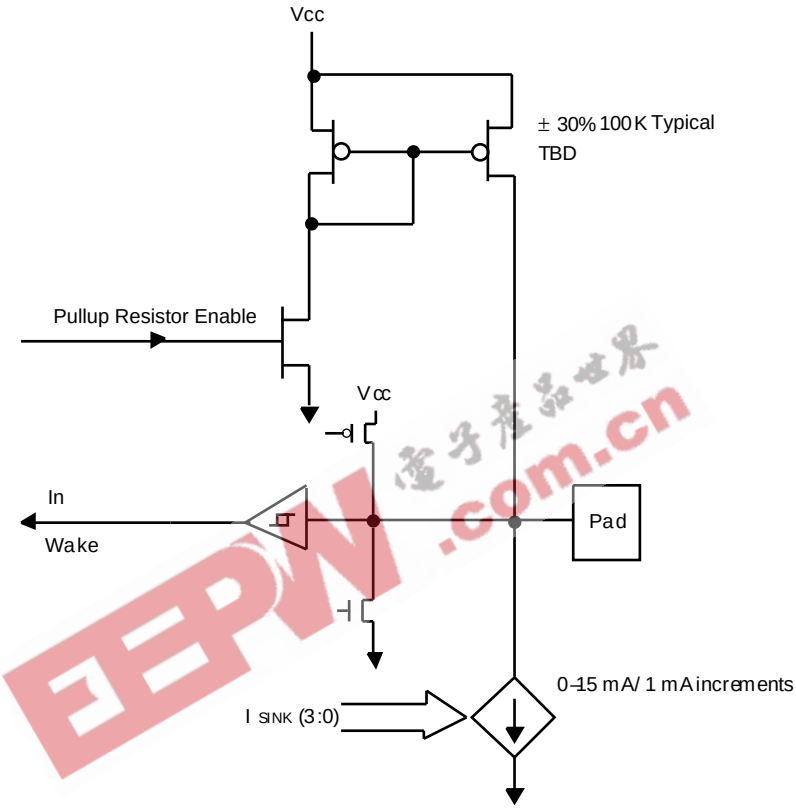


Figure 7. Port A (4–7) Sink Configuration

Table 3. Port A (4–7) Programmable Current Sink Table

Symbol	Parameter	Min.	Max.	Units	Conditions
N	Number of Bits			Bits	4 bits, 16 settings, 0–15 mA
DNL	Diff Non-Linearity		0.50	LSB	
I_0	Zero Code/Disable			µA	Disabled
I_{LSB}	LSB Current	0.65	1.35	mA	35%
I_F	Full Scale Current	9.75	20.25	mA	35%, Note 1
T_{settle}	Settling Time		1600	nS	Within 10% of final value
$I_{overshoot}$	Overshoot Current		$1.05*I_{set}$	µA	
V_{comp}	Compliance Voltage		1.1	V	Above V_{ss} with I_{FMAX}

Notes:
1. Setting all (4) I_{SNK} cells to full scale is a violation of the Absolute Maximum Rating Spec.

PIN FUNCTIONS (Continued)

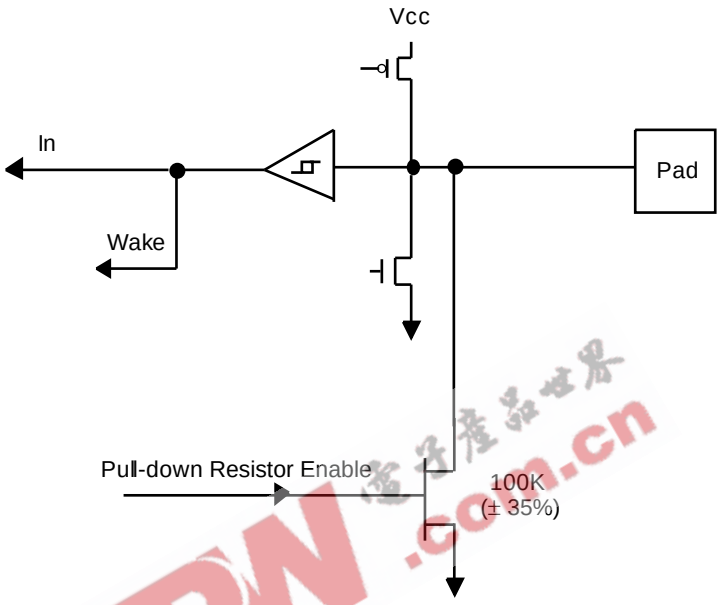
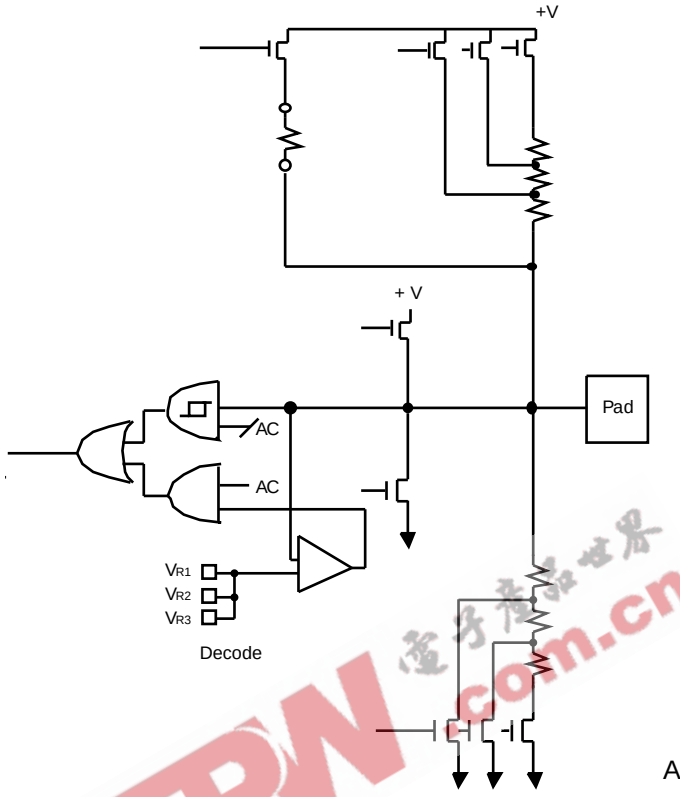


Figure 8. Port A (0–3) Switch Configuration

Port B. Port B (0–5) includes a Quadrature configuration (Figure 9), with programmable current sink and an analog comparator with programmable reference voltages (Tables 4–8).



AC = Analog Comparator Mode

Figure 9. Port B (0–5) Quadrature Configuration

PORT B (0–5) QUADRATURE CONFIGURATION

Table 4. Programmable Voltage Threshold

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{R1}	Voltage Reference 1	0.21 V_{CC}	0.29 V_{CC}	V	
V_{R2}	Voltage Reference 2	0.31 V_{CC}	0.39 V_{CC}	V	
V_{R3}	Voltage Reference 3	0.41 V_{CC}	0.49 V_{CC}	V	
Ratio	Ratio Accuracy		5	%	Note (1)

Note:
1. Greatest delta vs. specified delta.

PORT B (0–5) QUADRATURE CONFIGURATION (Continued)

Table 5. Programmable Voltage Bit Selections (Register Addresses DA–DF)

Comp Enable—Bit D7	V_{REF}— Bits D5:4	Selected	Conditions
0	xx	Comparator Off	Note (1)
1	01	0.25 V_{CC}	
1	10	0.35 V_{CC}	
1	11	0.45 V_{CC}	

Note:
1. If all comparators are off, V_{REF} can be powered off. If in Stop Mode, V_{REF} is powered off.

Table 6. Programmable Load Resistor

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{MID}	Midpoint Voltage	0.13 V_{CC}	0.15 V_{CC}	V	
R_{L1}	Load Resistor 1	5.25	8.75	K ohm	Pad to V_{SS}, track R_{L2}, R_{L3}
R_{L2}	Load Resistor 2	9.00	15.00	K ohm	Pad to V_{SS}, track R_{L1}, R_{L3}
R_{L3}	Load Resistor 3	13.50	22.50	K ohm	Pad to V_{SS}, track R_{L1}, R_{L2}
R_{L4}	Load Resistor 4	32.25	53.75	K ohm	Pad to V_{CC}
R_{L5}	Load Resistor 5	55.50	92.50	K ohm	Pad to V_{CC}
R_{L6}	Load Resistor 6	83.25	138.75	K ohm	Pad to V_{CC}
Ratio	Ratio Accuracy		5	%	Note (1)

Note:
1. Greatest ratio vs. specified ratio.

Table 7. Programmable Load Resistor Bit Selections (Register Addresses DA–DF

Divider Bits D2:0	Load Selected to V_{SS}	Load Selected to V_{CC}
000	No load Resistors	No load Resistors
001	7 K Selected	43 K Selected
010	12 K Selected	74 K Selected
100	18 K Selected	111 K Selected

Table 8. Comparator

Symbol	Parameter	Min.	Max.	Units	Conditions
VOS	Offset Voltage		25	mV	
HYS	Hysteresis	TBD	TBD	mV	Common Mode, Note (1)
VCM	Voltage Range	V_{SS}–0.3	V_{CC}–1.0	V	
T_{rf}	Response Time Fast		1	µs	700 mV/µs with 25 mV overdrive
T_{rs}	Response Time Slow		1	µs	15 mV/µs with 25 mV overdrive
IDD	Supply Current		100	µA	

Note:
1. Zilog will provide specification.

Port B. Port B (6–7) is configured as a serial communication port as follows:

	USB	PS/2	RS232	GPIO
Port B (6)	D–	Data	R x D	Port B (6)
Port B (7)	D+	Clock	T x D	Port B (7)

Port B (6) has a programmable internal pullup of 7.5 K ± 30%. For USB Mode, Port B (7) requires an external pullup of 7.5 K ± 1% to V_{CC} (Figure 10).

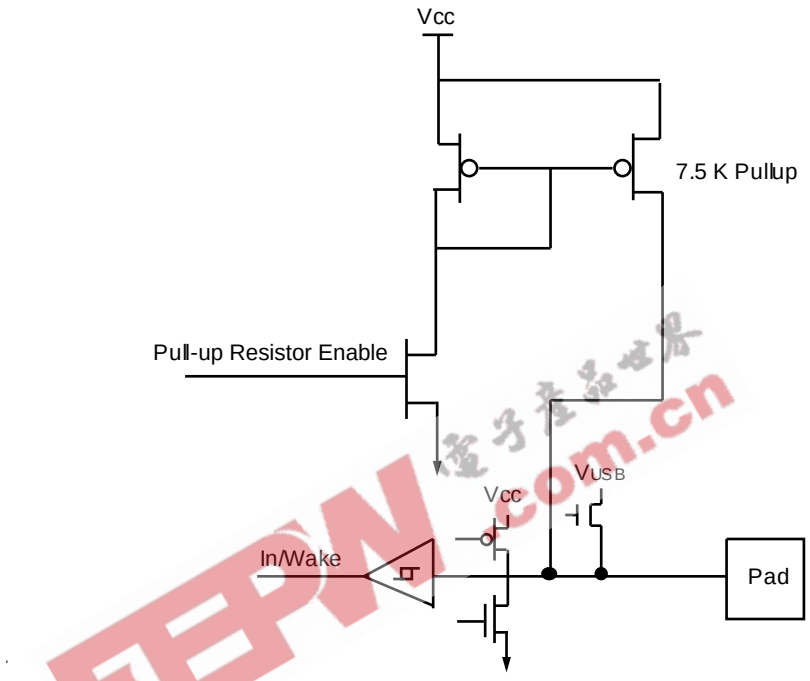


Figure 10. Port B (6–7) Serial Communication Port

FUNCTIONAL DESCRIPTION

Program Memory. The 16-bit program counter addresses 6 KB of program memory space at internal locations (Figure 11).

The first 14 bytes of program memory are reserved for the rollover and interrupt vectors. These locations have six 16-bit vectors that correspond to the six available interrupts.

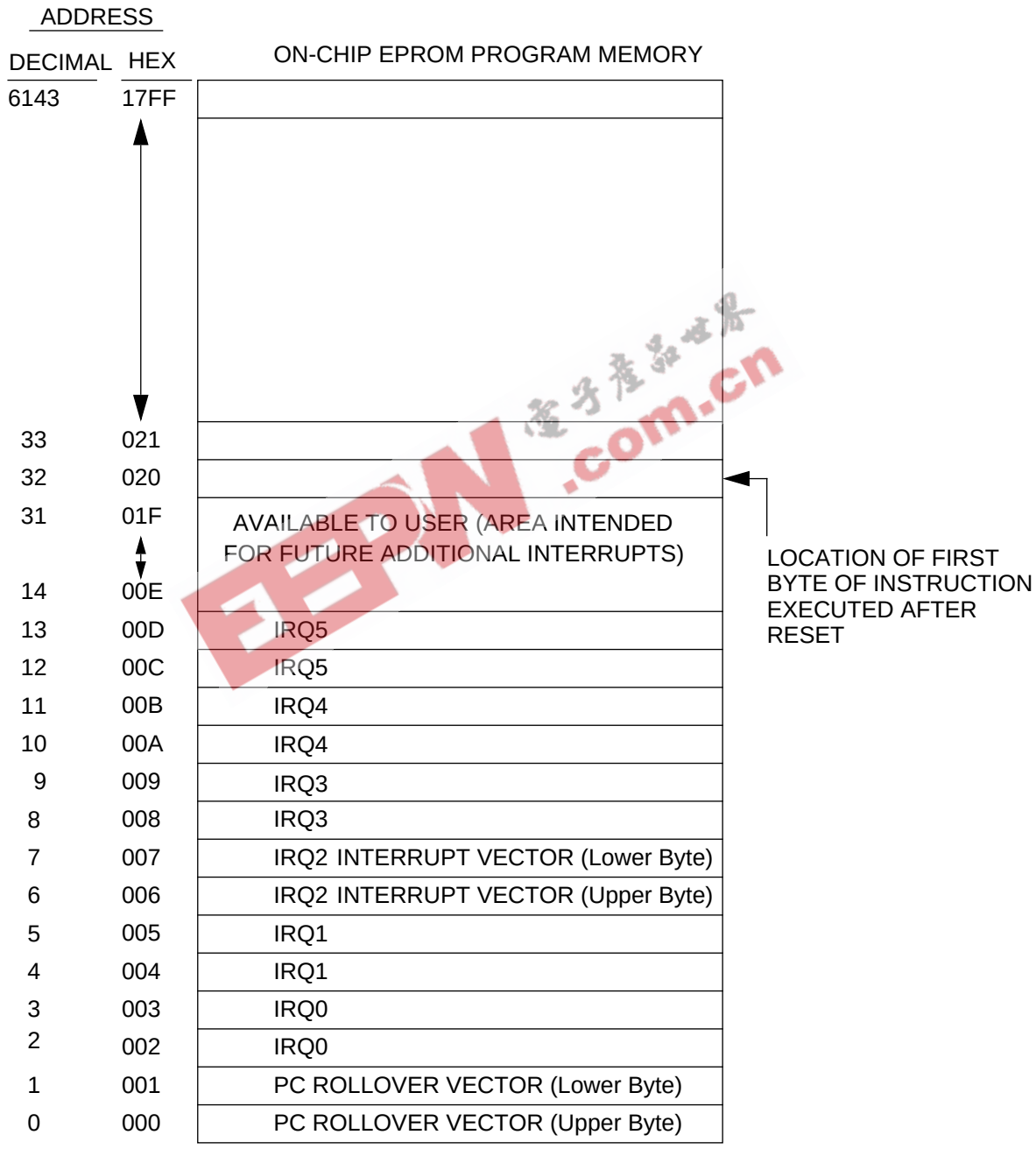


Figure 11. Z8E520 Program Memory Map

Register File. The register file consists of the following: 160 General-Purpose Registers in group 0–7, SIE Buffers in group 8–A, SIE Control in group B, Timer/Counters in group C, Configuration Registers in group D, Virtual Registers in group E and System Registers in Group F (Figure 12).

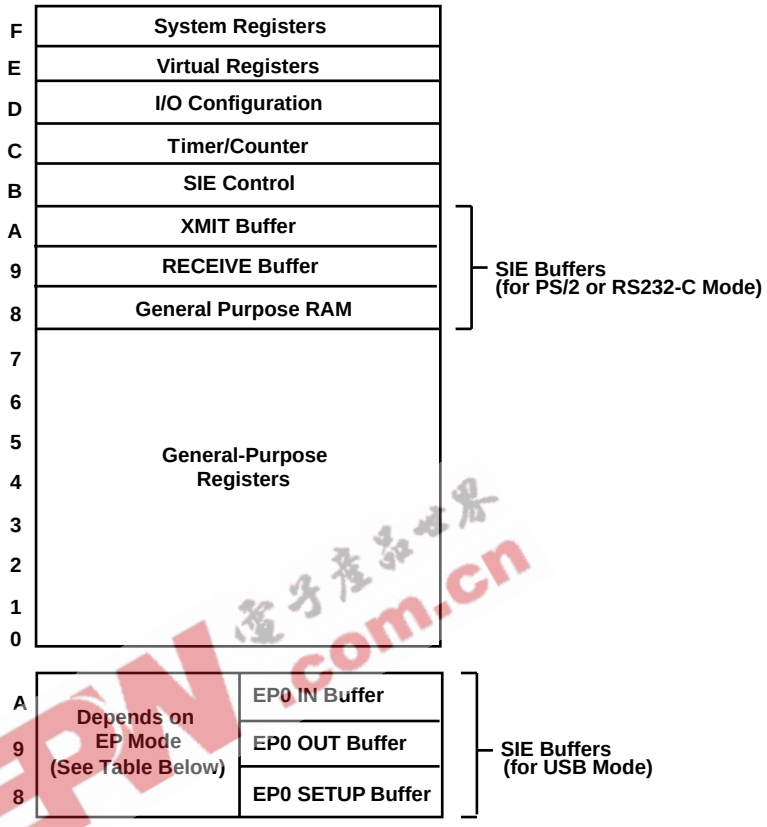


Figure 12. Register Files

Table 9. EP Modes for SIE Buffer (In USB Mode)

EP Mode	Description	Buffer Address		
		0x88–0x8F	0x98–0x9F	0xA8–0xAF
000	EP1 OFF, EP2 OFF	GPR	GPR	GPR
001	EP1 IN, EP2 OFF	GPR	GPR	EPI IN Buffer
010	EP1 OUT, EP2 OFF	GPR	GPR	EP1 OUT Buffer
011	EP1 CONTROL	EP1 SETUP Buffer	EP1 OUT Buffer	EP1 IN Buffer
100	EP1 OUT, EP2 OUT	GPR	EP2 OUT Buffer	EP1 OUT Buffer
101	EP1 IN, EP1 OUT	GPR	EP1 OUT Buffer	EP1 IN Buffer
110	EP1 OUT, EP1 IN	GPR	EP1 IN Buffer	EP1 OUT Buffer
111	EP1 IN, EP2 IN	GPR	EP2 IN Buffer	EP1 IN Buffer

FUNCTIONAL DESCRIPTION (Continued)

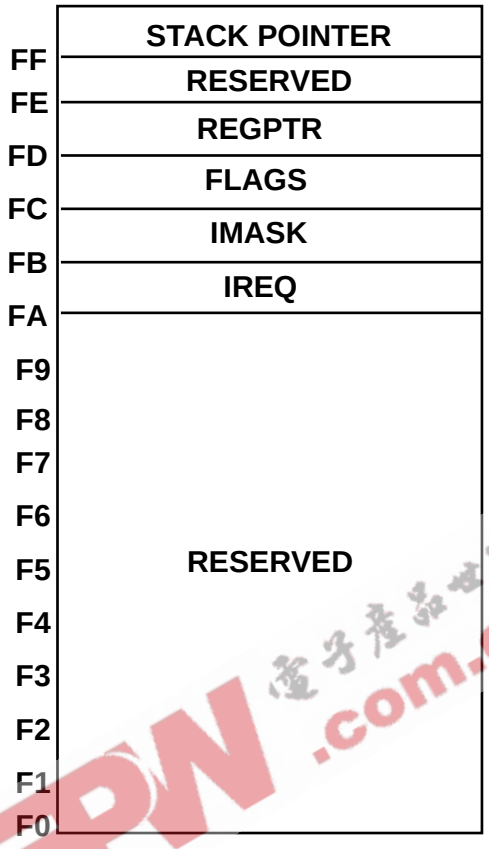


Figure 13. System Registers

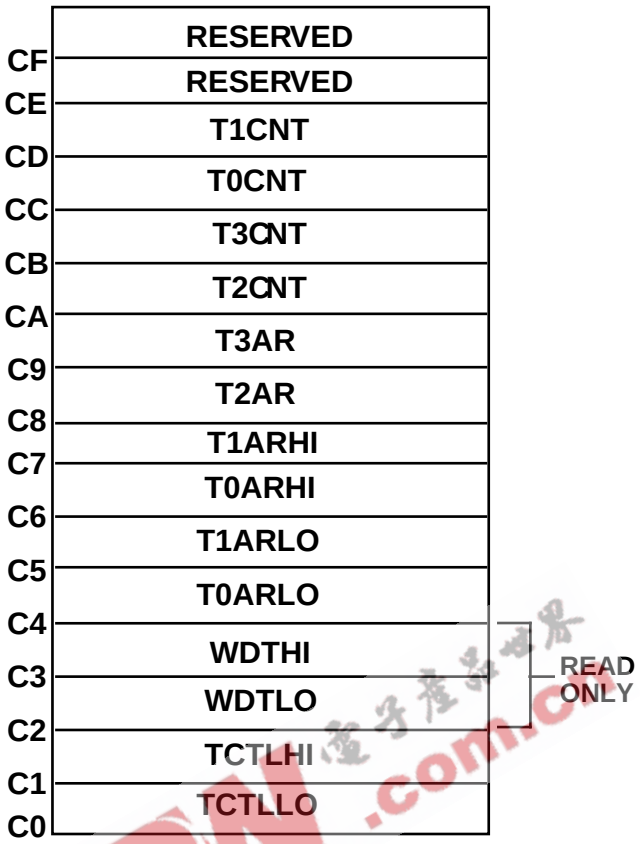


Figure 14. T/C Control Registers

FUNCTIONAL DESCRIPTION (Continued)

ADDR	NAME	D7	D6	D5	D4	D3	D2	D1	D0
B0	PORT A	A7	A6	A5	A4	A3	A2	A1	A0
B1	PORT B	B7	B6	B5	B4	B3	B2	B1	B0
B2	ADDR		USB ADDRESS 6:0						
B3	SIE MODE	SIE MODE 7:0					RS232	PS/2	USB
B4	USB CSR	SIE POWER	FORCE RESUME	ACTIVITY	J STATE		EP MODE 2:0		
B5	LOW PRIORITY INTR	DEPENDS ON EP MODE (SEE TABLE 10)							
B6	LOW PRIORITY MASK	DEPENDS ON EP MODE (SEE TABLE 10)							
B7	HIGH PRIORITY INTR	RESUME	NAK SENT EP1	NAK SENT EP0	STALL SENT EP2	STALL SENT EP1	STALL SENT EP0	SETUP EP1	SETUP EP0
B8	HIGH PRIORITY MASK	SAME AS HIGH PROIORITY INTR							
B9	EP0 CSR	ACK STATUS OUT	SETUP BUFFER VOLATILE	OUT SERVICED	OUT DATA TOGGLE	FORCE STALL	FORCE NAK	IN PACKET READY	IN DATA TOGGLE
BA	EP1/2 CSR	DEPENDS ON EP MODE (SEE TABLE 11)							
BB	EP0 COUNT	EP0 OUT COUNT 3:0				EP0 IN COUNT 3:0			
BC	EP1/2 COUNT	DEPENDS ON EP MODE (SEE TABLE 12)							
BD									
BE									
BF									

Figure 15. COMM Registers (USB Mode: B0–BF)

COMMUNICATION REGISTER DEFINITIONS (USB MODE)

The following definitions on pages 23–26 describe in detail the specific USB mode registers as illustrated in Figure 15.

PORT A, PORT B: I/O Port data registers. At all times, a read to this port should indicate the current state at the pins. Read/Write.

ADDR: Determines the USB Device Address. Cleared by USB or POR Reset. Read/Write.

SIE MODE: Determines the mode of the SIE communication pins (Port B7:6). Read/Write. The SIE modes are as follows:

SIE Mode	Description	Port B7	Port B6
00000000	GPIO	I/O	I/O
00000001	USB	D+	D–
00000010	PS/2	CLOCK	DATA
00000100	RS232-C 1200 Baud N81 Full Duplex	DATA IN	DATA OUT
Other	Reserved	Reserved	Reserved

GPIO: The SIE is off and the communication lines are standard I/O pins on Port B.

USB: Port B7 is D+, which connects to pin 3 on a series A, or series B USB connector and whose conductor is green. Port B6 is D–, which connects to pin 2 on a series A or series B USB connector and whose conductor is white. An external 7.5K pull-up should be provided for D–.

PS/2: Port B7 is CLOCK, which connects to pin 5 on a male 6-pin Mini-DIN connector and Port B6 is DATA, which connects to pin 1 on a male 6-pin Mini-DIN connector. These signals are open-drain. The CLOCK pin has an available 7.5 K ohm pull-up internal to the chip. An external 7.5 K ohm pull-up should be provided for DATA.

RS232: Port B7 is serial data out (T x D). Port B6 is serial data in (R x D). These signals are CMOS-level signals, positive logic. Appropriate transceiver circuitry must be added externally to comply with RS232-C signal levels at the device connector.

SIE POWER: Powers up the SIE when USB Resume signaling has been received, or shuts down SIE in preparation for USB Suspend. Read/Write.

FORCE RESUME: Forces a K state on the USB pins. Read/Write.

ACTIVITY: This bit is set by the SIE when the state of the USB pins changes. Read/Write.

J STATE: This bit is set when the USB is in the 'J' state and cleared when in 'K' or 'SE0'. Read only.

EP MODE: These bits define the operation of the non-zero endpoints of the SIE. Changing this mode resets the SIE, while writing the same value does not. Read/Write. The EP modes are as follows:

EP Mode	Description
000	EP1 OFF, EP2 OFF
001	EP1 IN, EP2 OFF
010	EP1 OUT, EP2 OFF
011	EP1 CONTROL
100	EP1 OUT, EP2 OUT
101	EP1 IN, EP1 OUT
110	EP1 OUT, EP1 IN
111	EP1 IN EP2 IN

COMMUNICATION REGISTER DEFINITIONS (USB MODE) (Continued)

LOW PRIORITY INTR: This register contains the IRQ source flags of a low-priority communications interrupt. The ISR should check these bits to determine the cause of the interrupt. The definition of these bits depends on the EP Mode as specified in the USB CSR. Writing a 1 to their position clears interrupt sources. Read/Write.

LOW PRIORITY MASK: This register contains mask bits for the IRQ sources specified in the LOW PRIORITY INTR register. A set bit indicates that the corresponding interrupt source is unmasked.

Table 10 illustrates both Low Priority MASK and INTR conditions according to EP Mode:

Table 10. Low Priority MASK and INTR Conditions

EP MODE	Description	EP 2		EP 1		EP 0			
000	EP1 OFF, EP2 OFF					OUT NAK SENT	OUT PACKET READY	IN NAK SENT	IN DONE
001	EP1 IN EP2 OFF			IN NAK SENT	IN DONE	OUT NAK SENT	OUT PACKET READY	IN NAK SENT	IN DONE
010	EP1 OUT, EP2 OFF			OUT NAK READY	OUT PACKET READY	OUT NAK SENT	OUT PACKET READY	IN NAK SENT	IN DONE
011	EP1 CONTROL	OUT NAK SENT	OUT PACKET READY	IN NAK SENT	IN DONE	OUT NAK SENT	OUT PACKET READY	IN NAK SENT	IN DONE
100	EP1 OUT, EP2 OUT	OUT NAK SENT	OUT PACKET READY	OUT NAK SENT	OUT PACKET READY	OUT NAK SENT	OUT PACKET READY	IN NAK SENT	IN DONE
101	EP1 IN, EP1 OUT	OUT NAK SENT	OUT PACKET READY	IN NAK SENT	IN DONE	OUT NACK SENT	OUT PACKET READY	IN NAK SENT	IN DONE
110	EP1 OUT, EP1 IN	IN NAK SENT	IN DONE	OUT NAK SENT	OUT PACKET READY	OUT NAK SENT	OUT PACKET READY	IN NAK SENT	IN DONE
111	EP1 IN EP2 IN	IN NAK SENT	IN DONE	IN NAK SENT	IN DONE	OUT NACK SENT	OUT PACKET READY	IN NAK SENT	IN DONE

IN DONE: The SIE received a valid IN token, sent the data packet and received an ACK from the host. Setting this bit by the SIE, clears IN PACKET READY and IN NAK SENT. SIE may never write to the IN buffer.

IN NAK SENT: The SIE sent a NAK on an IN transmission because IN PACKET READY was clear.

OUT PACKET READY: The SIE received a valid OUT packet and placed the received data, if any, in the buffer, thereby updating the OUT count register and sending an ACK. Setting this bit by the SIE clears OUT SERVICED and OUT NAK SENT. Firmware may never write to the OUT buffer.

OUT NAK SENT: The SIE sent a NAK on an OUT transaction because OUT SERVICED was clear. If an OUT packet was NAK'd, OUT DATA TOGGLE and the OUT buffer *must not be affected.*

HIGH PRIORITY INTR: This register contains the IRQ source flags of a high-priority communications interrupt. The ISR should check these bits to determine the cause of the interrupt. Writing a 1 to their position clears interrupt sources. Read/Write.

- **RESUME**: This bit is set when the ACTIVITY bit is set in the USB CSR, allowing the device to wake up on any activity of the USB.
- **STALL SENT EP2**: This bit is set when a STALL is sent on EP2. This bit is valid only in EP modes 100, 101, 110 and 111.
- **STALL SENT EP1**: This bit is set when a STALL is sent on EP1. This bit is not valid in EP mode 000.
- **STALL SENT EP0**: This bit is set when a STALL is sent on EP0.
- **SETUP EP1**: This bit is set after the completion of the setup stage of a control transfer on EP1. This bit is valid only in EP mode 011.
- **SETUP EP0**: This bit is set after the completion of the setup stage of a control transfer on EP0.

HIGH PRIORITY MASK: This register contains mask bits for the IRQ sources specified in the HIGH PRIORITY INTR register. A set bit indicates that the corresponding interrupt source is unmasked.

EP0 CSR: Control/Status register of Endpoint 0 (Control pipe).

EP1/2 CSR: Control/Status register of additional endpoints. The definition of these bits depends on the EP Mode as specified in the USB CSR. Read/Write.

Table 11 illustrates the EP1/2 CSR registers according to EP Mode:

Table 11. EP 1/2 CSR Registers (BA)

EP MODE	Description	EP 1							
000	EP1 OFF, EP2 OFF					FORCE STALL	FORCE NAK	IN PACKET READY	IN DATA TOGGLE
001	EP1 IN EP2 OFF					FORCE STALL	FORCE NAK	IN PACKET READY	IN DATA TOGGLE
010	EP1 OUT, EP2 OFF					FORCE STALL	FORCE NAK	OUT PACKET READY	OUT DATA TOGGLE
011	EP1 CONTROL	ACK STATUS OUT	SETUP BUFFER VOLATILE	OUT SERVICED	OUT DATA TOGGLE	FORCE STALL	FORCE NAK	IN PACKET READY	IN DATA TOGGLE
100	EP1 OUT, EP2 OUT	FORCE STALL	FORCE NAK	OUT SERVICED	OUT DATA TOGGLE	FORCE STALL	FORCE NAK	OUT PACKET READY	OUT DATA TOGGLE
101	EP1 IN, EP1 OUT	FORCE STALL	FORCE NAK	OUT SERVICED	OUT DATA TOGGLE	FORCE STALL	FORCE NAK	IN PACKET READY	IN DATA TOGGLE
110	EP1 OUT, EP1 IN	FORCE STALL	FORCE NAK	IN PACKET READY	IN DATA TOGGLE	FORCE STALL	FORCE NAK	OUT PACKET READY	OUT DATA TOGGLE
111	EP1 IN EP2 IN	FORCE STALL	FORCE NAK	IN PACKET READY	IN DATA TOGGLE	FORCE STALL	FORCE NAK	IN PACKET READY	IN DATA TOGGLE

FORCE STALL: Forces the SIE to stall all IN and OUT transactions. The successful receipt of a setup token clears this bit. STALL takes priority over NAK or ACK. Read/Write.

IN PACKET READY: When clear, IN transactions are NAK'd. This bit cannot be cleared by firmware. To clear it, firmware should be set FORCE NAK. Firmware must not write to the IN buffer or IN COUNT while this bit is set. It is cleared when the SIE sets IN DONE or when the SIE re-

COMMUNICATION REGISTER DEFINITIONS (USB MODE) (Continued)

ceives a valid setup token (via FORCE NAK). Setting IN PACKET READY clears IN NAK SENT. Read/Set.

FORCE NAK: Setting this bit clears IN PACKET READY if no IN transaction are in progress, and clears OUT SERVICED and ACK STATUS OUT if no OUT transactions are in progress. This bit is cleared by a setup token or by firmware. Read/Write.

IN DATA TOGGLE: Indicates what type of PID to use in the data phase of the next IN transaction. SIE may never write to this bit. Read/Write.

OUT SERVICED: When cleared, OUT transactions are NAK'd. It is cleared when the SIE sets OUT PACKET READY or receives a valid setup token (via FORCE NAK). This bit cannot be cleared by firmware. To clear it, firmware should be set FORCE NAK. When set, OUT COUNT and OUT buffer are volatile. Setting OUT SERVICED clears OUT N AK SENT. Read/Set.

OUT DATA TOGGLE: Indicates what type of PID was received in the data phase of the most recent successful OUT transaction. Read only.

SETUP BUFFER VOLATILE: Indicates that the SIE has entered the data stage of a control transfer. The successful receipt of a setup token sets and locks this bit. The bit remains locked as set until the data phase is complete and error free. If the data phase has an error, this bit will remained locked, but a setup interrupt will still occur to inform the firmware that a new transfer was attempted. After the data phase is received without errors, firmware may clear this bit. Read/Clear (if unlocked).

ACK STATUS OUT: This bit serves to filter the response to an OUT transaction. Setting this bit also sets OUT SERVICED. This bit cannot be cleared by firmware. To clear it, firmware should be set FORCE NAK. Read/Set.

While ACK STATUS OUT is set:

- If IN NAK SENT is clear, the SIE will ACK an empty OUT DATA 1 transaction.
- If IN NAK SENT is set, the SIE will NAK an empty OUT DATA 1 transaction.
- Any other kind of OUT transaction will be stalled and set the STALL SENT interrupt. It is possible to have both STALL SENT and OUT PACKET READY set on a single, incorrect OUT transaction.
- Any out transaction will cause the SIE to set FORCE NAK and OUT PACKET READY. As a result, ACK STATUS OUT is cleared. ACK STATUS OUT has "one-shot" behavior. It only handles one OUT transaction.
- The successful receipt of a setup token sets FORCE NAK, which clears this bit.

EP0 COUNT: Contains counts of bytes in the endpoint buffers.

EP1/2 COUNT: Contains counts of bytes in the endpoint buffers. Definition of this register depends on the EP Mode as illustrated in Table 12:

Table 12. EP 1/2 Counts

EP MODE	Description	EP1/2 COUNT	
000	EP1 OFF, EP2 OFF	GP R	
001	EP1 IN EP2 OFF	GPR	EP1 IN COUNT 3:0
010	EP1 OUT, EP2 OFF	GPR	EP1 OUT COUNT 3:0
011	EP1 CONTROL	EP1 OUT COUNT 3:0	EP1 IN COUNT 3:0
100	EP1 OUT, EP2 OUT	EP2 OUT COUNT 3:0	EP1 OUT COUNT 3:0
101	EP1 IN, EP1 OUT	EP1 OUT COUNT 3:0	EP1 IN COUNT 3:0
110	EP1 OUT, EP1 IN	EP1 IN COUNT 3:0	EP1 OUT COUNT 3:0
111	EP1 IN EP2 IN	EP2 IN COUNT 3:0	EP1 IN COUNT 3:0

EP OUT COUNT: Set by the SIE to indicate the number of bytes received in the most recent OUT transaction. Invalid while OUT SERVICED is set.

EP IN COUNT: Set by firmware to indicate the number of bytes to transfer in the next IN transaction. Invalid while IN PACKET READY is set.

ADDR	NAME	D7	D6	D5	D4	D3	D2	D1	D0
B0	PORT A	A7	A6	A5	A4	A3	A2	A1	A0
B1	PORT B	B7	B6	B5	B4	B3	B2	B1	B0
B2									
B3	SIE MODE	MODE 3:0					1200 BAUD SERIAL	PS/2	USB
B4									
B5	LOW PRIORITY INTR	PB7 INTR	PB6 INTR			HOST ABORT	COMM ERROR	BYTE RCV	XMIT DONE
B6	LOW PRIORITY MASK	PB7 MSK	PB6 MSK	SAME AS LOW PRIORITY INTR					
B7	HIGH PRIORITY INTR						OVER-RUN ERROR	RCV COMM ERROR	RCV DONE
B8	HIGH PRIORITY MASK	SAME AS HIGH PRIORITY INTR							
B9	COMM CSR				RCV READY				XMIT READY
BA									
BB	PACKET SIZE	RCV PACKET SIZE				XMIT PACKET SIZE			
BC	BYTE OFFSETS	LAST BYTE RECEIVED OFFSET				NEXT SEND BYTE OFFSET			
BD									
BE									
BF									

Figure 16. COMM Registers (Non-USB Modes: B0–BF)

COMMUNICATION REGISTER DEFINITIONS (NON-USB MODES)

The following definitions describe in detail the specific non-USB mode registers as illustrated in Figure 16.

PORT A, PORT B: Same as USB mode. Port B6 and B7 are I/O in the GPIO Mode.

SIE MODE: Same as USB mode.

LOW PRIORITY INTR: This register contains the IRQ flags of a low-priority communications interrupt. Read/Write.

LOW PRIORITY MASK: This register contains mask bits for the IRQ sources specified in the LOW PRIORITY INTR register. A set bit indicates that the corresponding interrupt source is unmasked.

- **XMIT COMM ERROR**: Indicates that a communications error occurred while transmitting a byte. Valid only when the SIE is in PS/2 mode. Indicates that the host aborted the transfer.
- **XMIT DONE**: Indicates that XMIT PACKET SIZE bytes have been sent since XMIT READY was set.

HIGH PRIORITY INTR: This register contains the IRQ source flags of a low-priority communications interrupt. The ISR should check these bits to determine the cause of the interrupt. Read/Write.

HIGH PRIORITY MASK: This register contains mask bits for the IRQ sources specified in the HIGH PRIORITY INTR register. A set bit indicates that the corresponding interrupt source is unmasked.

- **OVERRUN ERROR**: Indicates that RCV READY was clear when RCV DONE was set.
- **RCV COMM ERROR**: Indicates that a communications error occurred while receiving a byte, resulting in a framing or parity error. In PS/2 mode, it may also indicate that the host aborted its own transmission.
- **RCV DONE**: Indicates that RCV PACKET SIZE bytes have been received since RCV READY was set.

COMM CSR: Controls the SIE in PS/2 and RS232-C mode.

- **XMIT READY**: Indicates to the SIE that the XMIT buffer is valid. Cleared by SIE when XMIT DONE is set. Cannot be cleared by firmware. Read/Write.
- **RCV READY**: Indicates to the SIE that the most recent packet received has been handled. Cleared by the SIE after RCV DONE is set. Cannot be cleared by firmware. Read/Write.
- **RCV PACKET SIZE**: Number of bytes to receive before BYTE RECEIVED interrupt. Value may not exceed the size specified in RCV BUFFER SIZE. A “0” indicates that the packet size = the buffer size. Read/Write.
- **XMIT PACKET SIZE**: The number of bytes to send before the XMIT DONE interrupt. A “0” indicates that the packet size = the buffer size
- **LAST BYTE RECEIVED OFFSET**: Indicates the offset in the RECEIVE buffer of the most recent byte received. Read only.
- **NEXT SEND BYTE OFFSET**: Indicates the offset in the XMIT buffer of the next byte to be sent. If the host has aborted a PS/2 transmission, it is the offset of the byte that was aborted. Read only.

INITIAL STATES: COMM REGISTERS, UPON CHANGING MODES:

ADDR	NAME	D7	D6	D5	D4	D3	D2	D1	D0
0	PORT A	Cleared by POR,or not changed							
1	PORT B	Same as Port A							
2	SIE CONTROL REGS	ALL 0							
3									
4									
5									
6									
7									
8									
9									
A									
B									
C									
D		Uninitialized							
E									
F									

INITIAL STATES: PORT CONFIGURATION REGISTERS:

All Registers in this state are cleared to 0 on POR.

PORT CONFIGURATION REGISTERS

ADDR	NAME	D7	D6	D5	D4	D3	D2	D1	D0
D0	PORT A CONFIG 01	A0				A1			
		WAKE	PUSH/ PULL	PULLDWN ON	OUTPUT	WAKE	PUSH/ PULL	PULLDWN ON	OUTPUT
D1	PORT A CONFIG 23	A2				A3			
		WAKE	PUSH/ PULL	PULLUP ON	OUTPUT	WAKE	PUSH/ PULL	PULLDWN ON	OUTPUT
D2	PORT A CONFIG 45	A4				A5			
		WAKE	PUSH/ PULL	PULLUP ON	OUTPUT	WAKE	PUSH/ PULL	PULLUP ON	OUTPUT
D3	PORT A CONFIG 67	A6				A7			
		WAKE	PUSH/ PULL	PULLUP ON	OUTPUT	WAKE	PUSH/ PULL	PULLUP ON	OUTPUT
D4	PORT B CONFIG 01	B0				B1			
		WAKE	PUSH/ PULL	PULLUP ON	OUTPUT	WAKE	PUSH/ PULL	PULLUP ON	OUTPUT
D5	PORT B CONFIG 23	B2				B3			
		WAKE	PUSH/ PULL	PULLUP ON	OUTPUT	WAKE	PUSH/ PULL	PULLUP ON	OUTPUT
D6	PORT B CONFIG 45	B4				B5			
		WAKE	PUSH/ PULL	PULLUP ON	OUTPUT	WAKE	PUSH/ PULL	PULLUP ON	OUTPUT
D7	PORT B CONFIG 67	B6				B7			
			PUSH/ PULL	PULLUP ON	OUTPUT		PUSH/ PULL	PULLUP ON	OUTPUT
D8	PORT A SINK 45	A5				A4			
		SINK 3:0				SINK 3:0			
D9	PORT A SINK 67	A7				A6			
		SINK 3:0				SINK 3:0			
DA	PORT B0	B0							
		COMP ENABLE		VREF 5:4			DIVIDER 2:0		
DB	PORT B1	B1							
		COMP ENABLE		VREF 5:4			DIVIDER 2:0		
DC	PORT B2	B2							
		COMP ENABLE		VREF 5:4			DIVIDER 2:0		
DD	PORT B3	B3							
		COMP ENABLE		VREF 5:4			DIVIDER 2:0		
DE	PORT B4	B4							
		COMP ENABLE		VREF 5:4			DIVIDER 2:0		
DF	PORT B5	B5							
		COMP ENABLE		VREF 5:4			DIVIDER 2:0		

Figure 17. Port Configuration Registers (D0–DF)

PORT REGISTER DEFINITIONS

The following definitions describe in detail the specific port registers as illustrated in Figure 17.

WAKE: When set, this pin is capable of waking the device on any edge.

PUSH/PULL: When set, this pin is a push-pull output. When clear, this pin is an open-drain output. Ignored if OUTPUT is clear.

PULLUP ON: When set, the pull-up resistor is on.

OUTPUT: When set, the pin's output drivers are enabled. However, the pin may be read at any time regardless of the configuration.

SINK: Indicates the level of current drawn by the current sink on the pin. When SINK ≠ 0, the n-channel output transistor is disabled. When SINK = 0, the sink is off and the n-channel output transistor may be enabled according to the OUTPUT bit.

DIVIDER: Selects one of the three voltage dividers to be placed on the pin. Divider 0 indicates no divider.

VREF: Indicates the voltage reference level for the comparator. Ignored if COMP ENABLED is clear.

COMP ENABLE: When set, the comparator is powered. When clear, the comparator and VREF circuitry are powered down.

FUNCTIONAL DESCRIPTIONS

Counter/Timers. For the Z8E20, 8-bit timers T0 and T1 are available to function as a pair of independent 8-bit standard timers, or they can be cascaded to function as a 16-bit PWM timer. In addition, 8-bit timers T2 and T3 are provided but they can only operate in cascade to function as a 16-bit standard timer (Figure 18).

Each 8-bit timer is provided a pair of registers, which are both readable and writable. One of the registers is defined to contain the auto-initialization value for the timer, while the second register contains the current value for the timer. When a timer is enabled, the timer will decrement whatever value is currently held in its count register, and will then continue decrementing until it reaches 0, at which time an interrupt will be generated and the contents of the auto-initialization register are optionally copied into the count value register. If auto-initialization is not enabled, the timer will stop counting upon reaching 0 and control logic will clear the appropriate control register bit to disable the timer. This occurrence is referred to as "single-shot" operation. If auto-initialization is enabled, the timer will continue counting from the initialization value. Software should not attempt to use registers that are defined as having timer functionality.

Software is allowed to write to any register at any time, but it is not recommended that timer registers be updated while the timer is enabled. If software updates the count value while the timer is in operation, the timer will continue counting based upon the software-updated value. This occurrence can produce strange behavior if the software update occurred at exactly the point that the timer was reaching 0 to trigger an interrupt and/or reload.

Similarly, if software updates the initialization value register while the timer is active, the next time that the timer reaches 0, it will be initialized using the updated value. Again, strange behavior could result if the initialization value register is being written while the timer is in the process of being initialized. Whether initialization is done with the new or old value is a function of the exact timing of the write operation. In all cases, the Z8E520 will prioritize the software write above that of a decremented writeback. However, when hardware clears a control register bit for a timer that is configured for single-shot operation; the clearing of the control bit will override a software write. Reading either register can be done at any time, and will have no effect on the functionality of the timer.

If a timer pair is defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt will be generated, and the interrupt will correspond to the even 8-bit time. For example, timers T2 and T3 are cascaded to form a single 16-bit timer, so the interrupt for the combined timer will be defined to be that of timer T2 rather than T3. When a timer pair is specified to act as a single 16-bit timer, the even timer registers in the pair (timer T0 or T2) will be defined to hold the timer's least significant byte; while the odd timer in the pair will hold the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value will be initialized by copying the contents of the auto-initialization value register to the count value register.

Note: Any time that a timer pair is defined to act as a single 16-bit timer, that the auto-reload function will be performed automatically. All 16-bit timers will continue counting while their interrupt requests are active, and will operate in a free-running manner.

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt has been responded to. This occurrence is a degenerate case, and hardware is not required to detect this

FUNCTIONAL DESCRIPTIONS (Continued)

condition. When the timer control register is written, all timers that are enabled by the write will begin counting using the value that is held in their count register. An auto-initialization is not performed. All timers can receive an internal clock source only, so synchronization of timer updates is not an issue. Each standard timer that is enabled will be updated every 8th XTAL clock cycle.

If T0 and T1 are defined to work independently, then each will work as an 8-bit timer with a single auto-initialization register; T0ARLO for T0, and T1ARLO for T1. Each timer will assert its predefined interrupt when it times out, and will optionally perform the auto-initialization function. If T0 and T1 are cascaded to form a single 16-bit timer, then the single 16-bit timer will be capable of performing as a Pulse-Width Modulator (PWM). This timer is referred to as T01 to distinguish it as having special functionality that is not available when T0 and T1 act independently.

When T01 is enabled, it can use a pair of 16-bit auto-initialization registers. In this mode, one 16-bit auto-initialization value is composed of the concatenation of T1ARLO and T0ARLO, and the second auto-initialization value is composed of the concatenation of T1ARHI and T0ARHI. When T01 times out, it will alternately initialize its count value using the Lo auto-init pair followed by the Hi auto-init pair. This functionality corresponds to a PWM where the T1 interrupt will define the end of the High section of the waveform, and the T0 interrupt will mark the end of the Low portion of the PWM waveform.

To use the cascaded timers as a PWM, one must initialize the T0/T1 count registers to work in conjunction with the port pin. The user should initialize the T0 and T1 count registers to the PWM hi auto-init value to obtain the required PWM behavior. The PWM is arbitrarily defined to use the Low auto-reload registers first, implying that it had just timed out after beginning in the High portion of the PWM waveform. As such, the PWM is defined to assert the T1 interrupt after the first timeout interval.

After the auto-initialization has been completed, decrementing occurs for the number of counts defined by the auto-init_lo registers. When decrementing again reaches 0, the T0 interrupt is asserted; and auto-init using the auto-init_hi registers occurs. Decrementing occurs for the number of counts defined by the auto-init_hi registers until reaching 0, at which time the the T1 interrupt is asserted, and the cycle begins again. The internal timers can be used to trigger external events by toggling port output when generating an interrupt. This functionality can only be achieved in conjunction with the port unit defining the appropriate pin as an output signal with the timer output special function enabled. In this mode, the appropriate port output will be toggled when the timer count reaches 0, and will continue toggling each time that the timer times out.

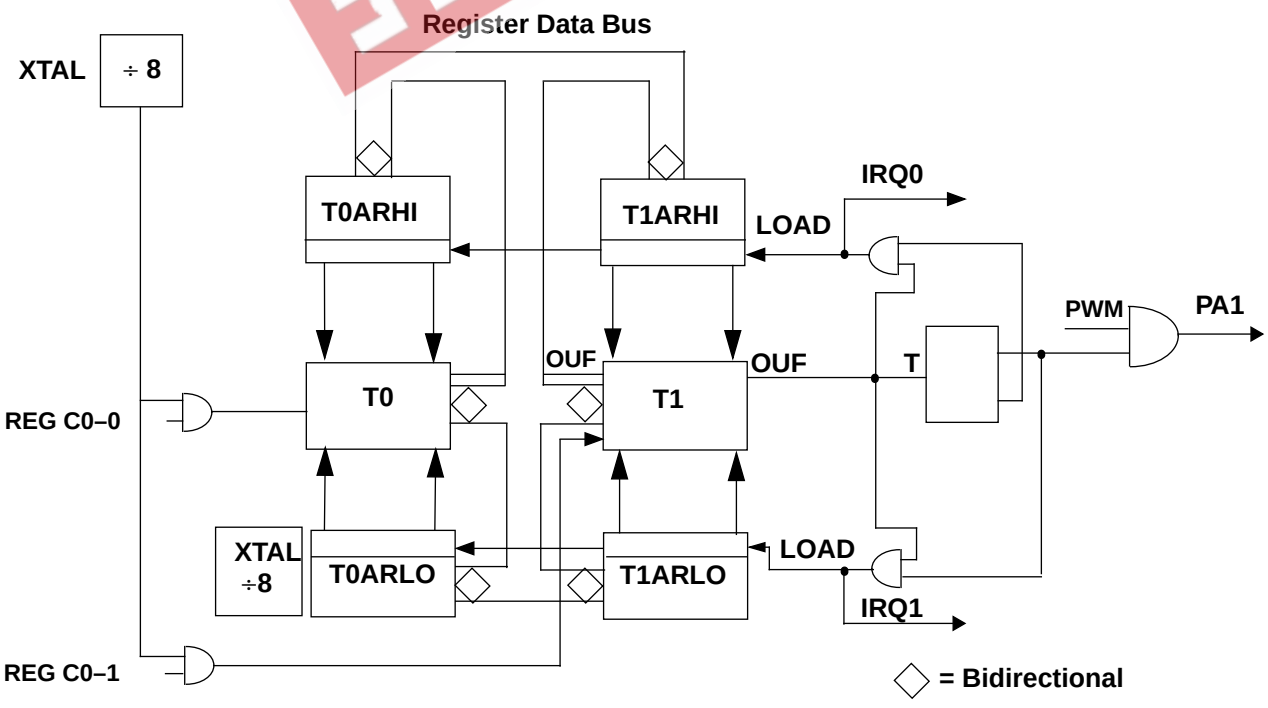


Figure 18. Z8E520 Timers Block Diagram

Watch-Dog Timer. The WDT can be programmed at anytime in the program operation.

Default value (Reset) = 98 ms

The RC oscillator is under firmware control. If the oscillator is enabled during USB Suspend/Chip Stop Mode, the device will be periodically woke up by the WDT timeout. If the application does not require “motion detect,” the current that drives the internal oscillator/WDT can be saved.

WDT Control Registers. Select time-out values for the WDT are programmable –0 to +100%.

Interrupts. The Z8E520 has six different interrupts. These interrupts are maskable and prioritized (Figure 19). The six sources are divided as follows:

Priority	IRQ
0	TCO
1	TC1
2	TC2
3	COMM HIGH
4	COMM LOW
5	Port

.

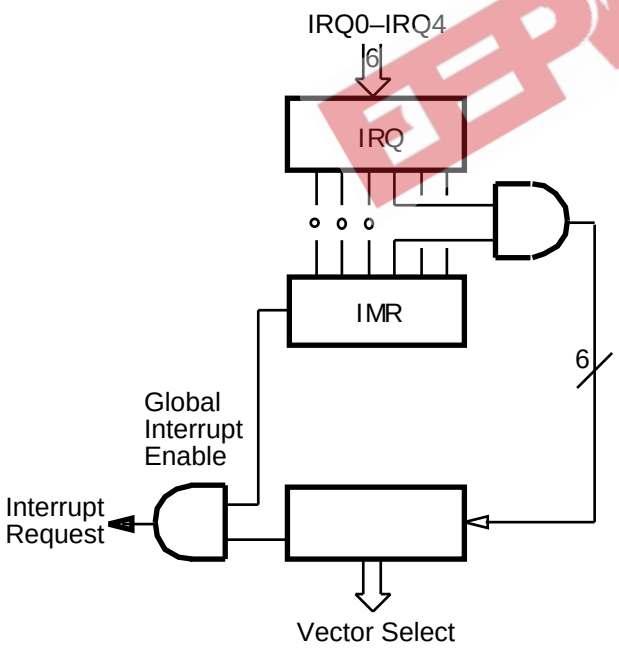


Figure 19. Interrupt Block Diagram

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated an interrupt request is granted. All of the subsequent interrupts are thus disabled, saving the Program Counter and status flags, and branching to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

EMI. Lower EMI on the Z8E520 is achieved through circuit modifications.

The Z8E520 also accepts external clock from XTAL IN pin (Figure 20).

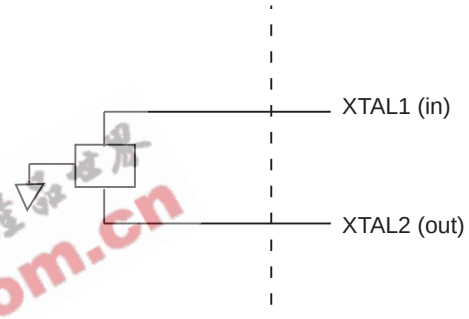


Figure 20. Oscillator Configuration

Power-On-Reset (POR)**.** A timer circuit is triggered by the system oscillator and is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. POR period is defined as:

$$\text{POR (ms)} = 98 \text{ ms}$$

The POR timer circuit is a one-shot timer triggered by power fail to Power OK status. The POR time is a nominal 100 ms at 6 MHz. The POR time is bypassed after Stop-Mode Recovery.

HALT. HALT turns off the internal CPU clock, but not the oscillator. The counter/timer and external interrupts IRQ0–5 remain active. The Z8E520 recovers by interrupts, either externally or internally.

USB Reset. Detection by the SIE of a reset from the Host will cause the chip to reset. The reset will be remembered so that the program can decide the source of the reset. The USB Reset will act even if the chip is in the STOP mode.

FUNCTIONAL DESCRIPTIONS (Continued)

V_{BO} Circuit. The Voltage Brown Out circuit will detect when voltage has dropped below the normal operating voltage. The chip will maintain full core functionality and RAM values will be preserved during the range from V_{MIN} (V_{CC} = 4V) to V_{BO}; however, it may not meet worst case AC and DC limits. At V_{BO}, the chip will be placed in reset and maintained in that state until V_{CC} exceeds V_{BO}. When this condition is reached, the chip will resume operation. V_{BO} is set by design to 2.7 V ± 0.2 V.

STOP. This instruction turns off the internal clock and external ceramic resonator oscillation. It reduces the standby current to less than 60 µA. The STOP Mode is terminated by an interrupt. An interrupt from any of the active (enabled) interrupts will remove the chip from the STOP Mode (Ports 31–33 including the USB reset.

Note: The timer cannot generate an interrupt in STOP Mode because the clock is stopped.

The interrupt causes the processor to restart the application program at the address or the vector of the interrupt and continue the program at the end of the interrupt service routine. In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. As a result, the user must execute a NOP (Opcode=FFH) immediately before the appropriate sleep instruction, such as:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
                or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

Z8PLUS SYSTEM REGISTERS

The registers displayed in Figures 21–27 represent Zilog's new Z8Plus architecture. For a complete overview of this new technology, please refer to the Z8Plus user's manual (UM97Z8X0300) available at your local Zilog sales office.

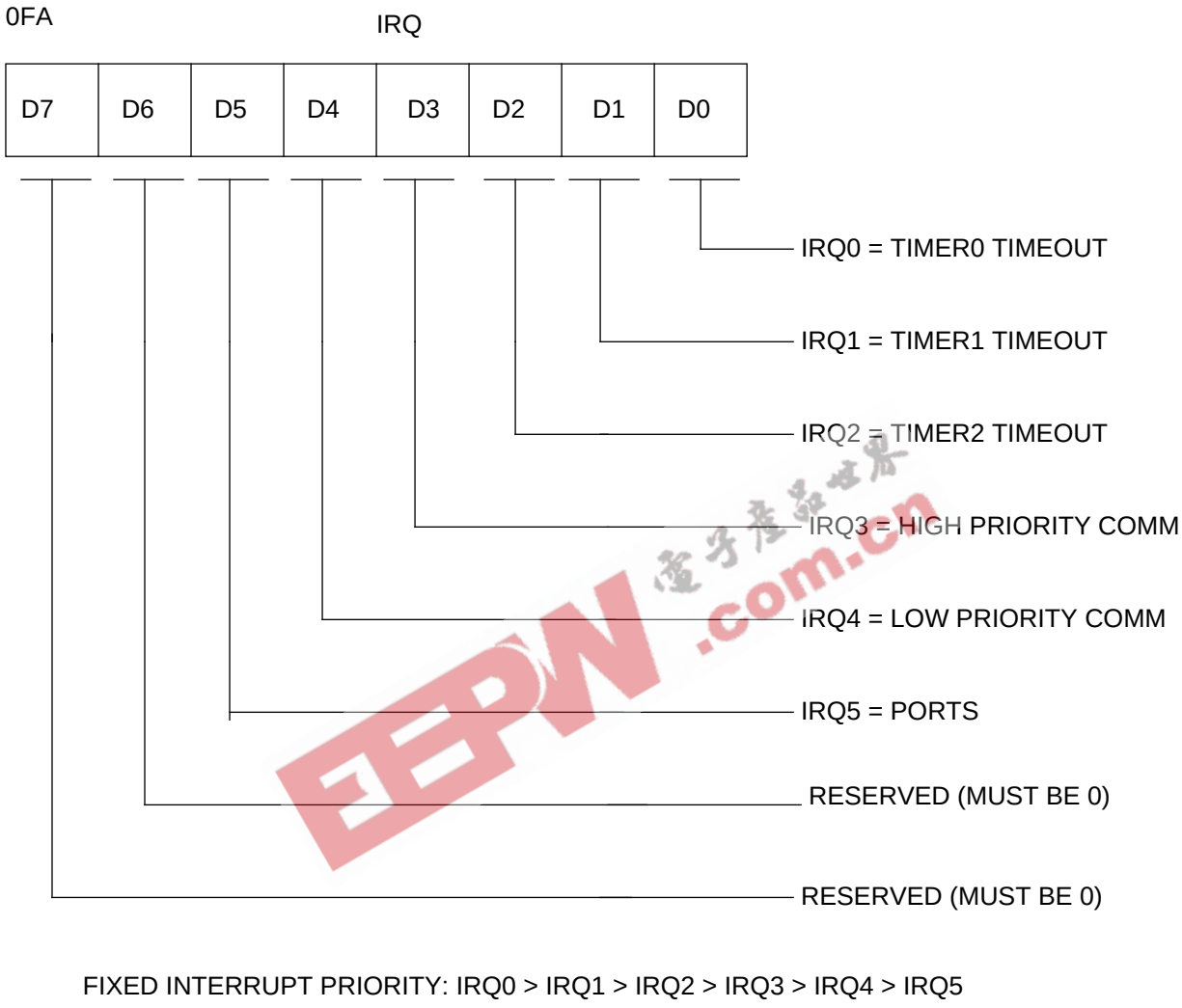


Figure 21. Interrupt Request Register

Z8PLUS SYSTEM REGISTERS (Continued)

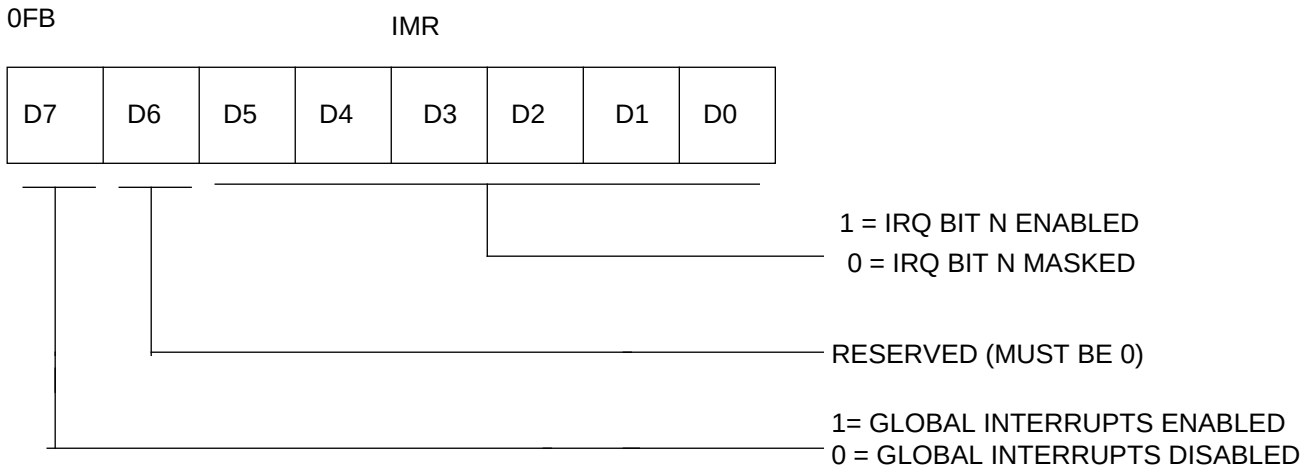


Figure 22. Interrupt Mask Register

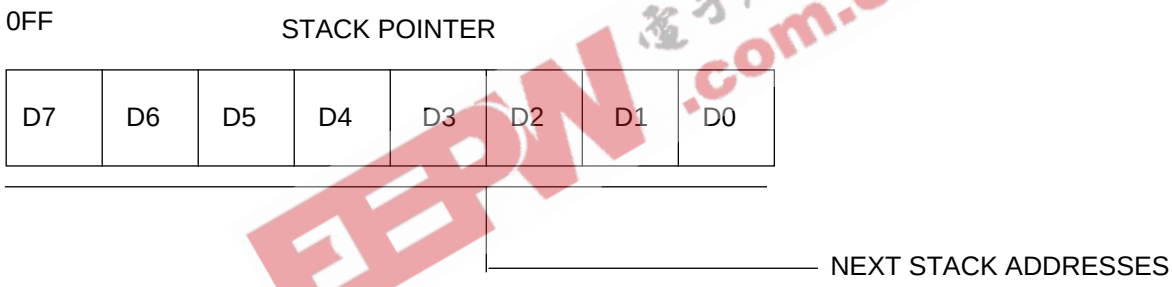


Figure 23. Stack Pointer

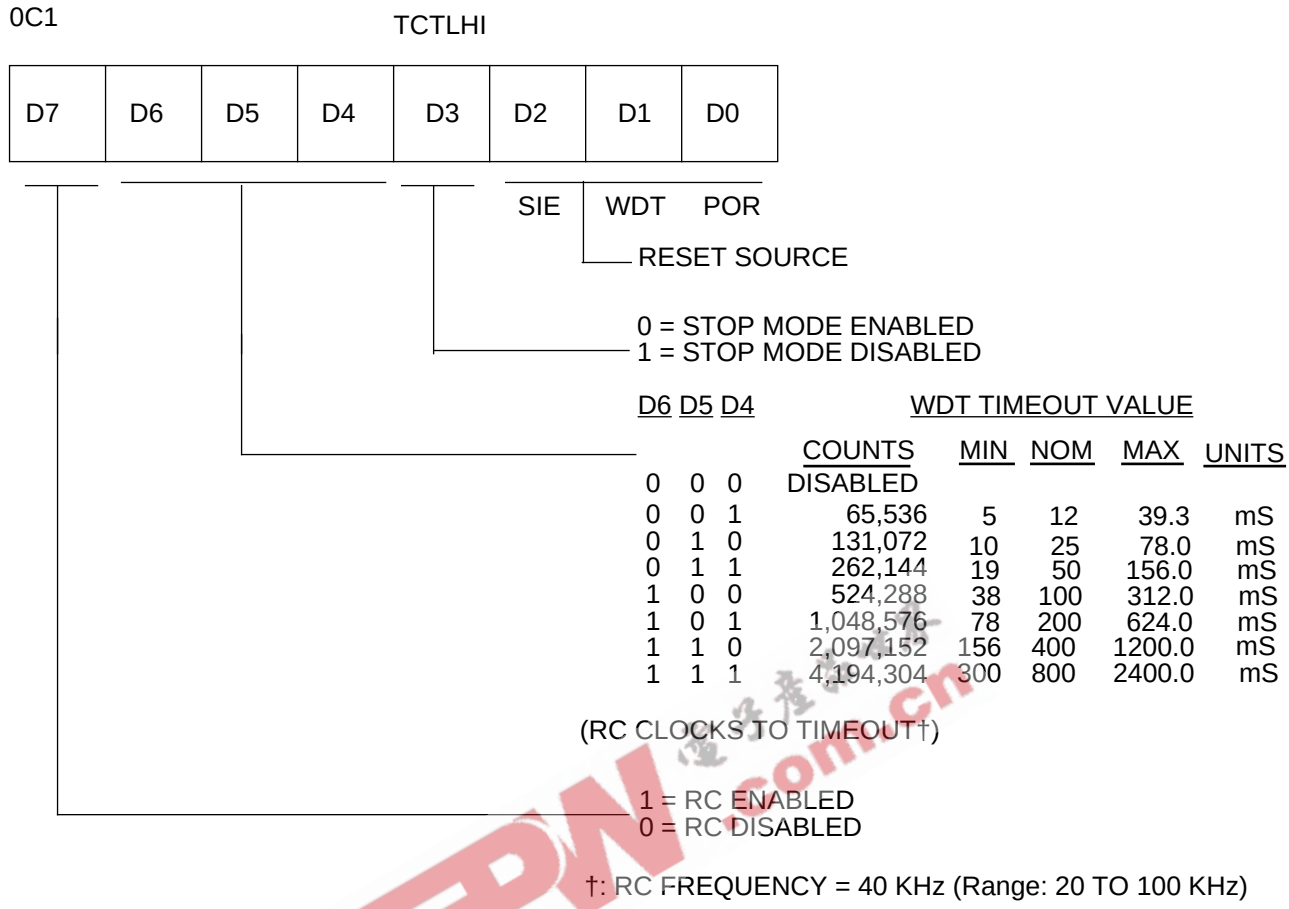
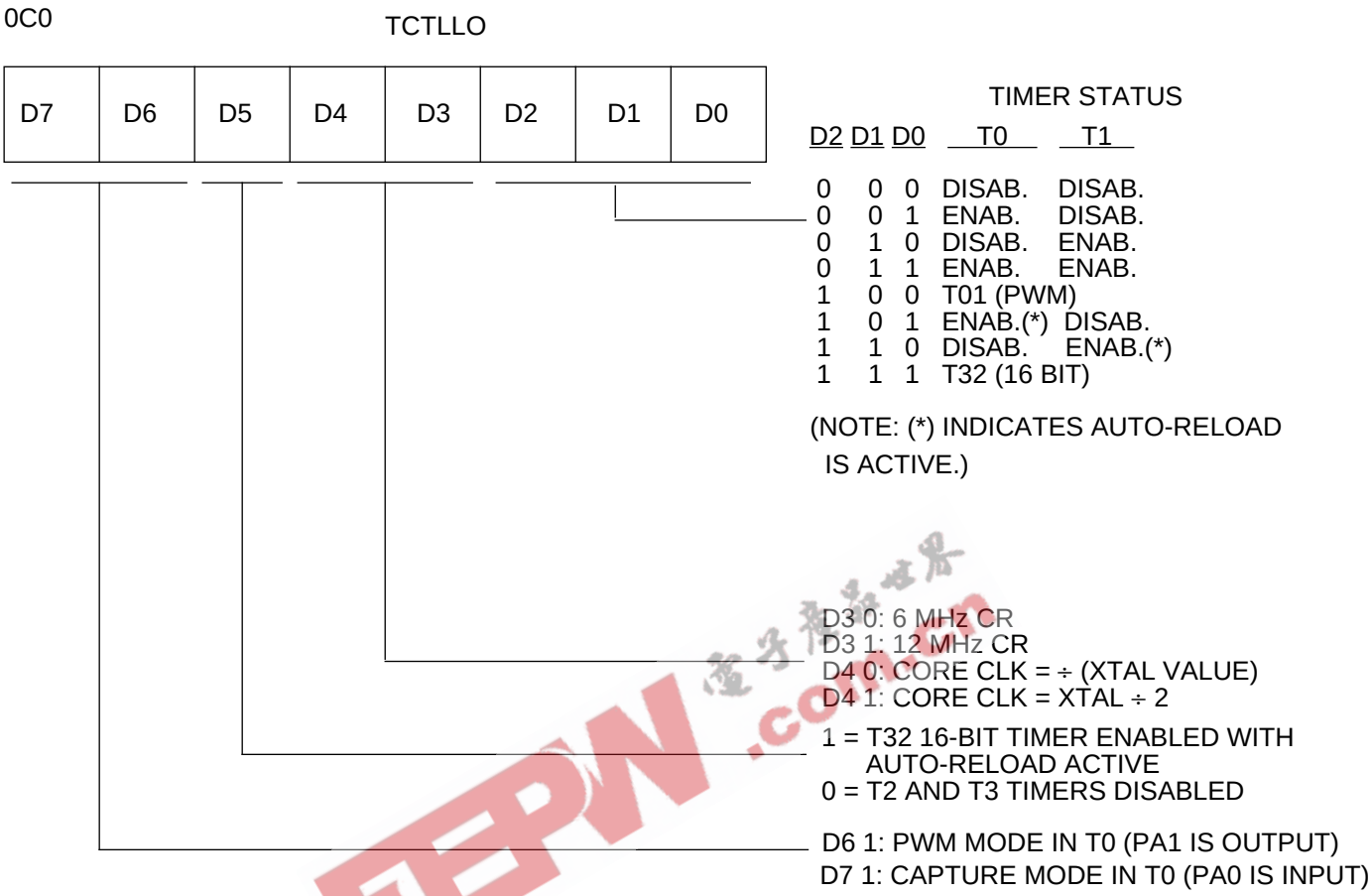


Figure 24. TCTLHI Register

Z8PLUS SYSTEM REGISTERS (Continued)



NOTE: TIMER T01 IS A 16-BIT PWM TIMER FORMED BY CASCADING 8-BIT TIMERS T1 (MSB) AND T0 (LSB). TIMER T32 IS A STANDARD 16-BIT TIMER FORMED BY CASCADING 8-BIT TIMERS T3(MSB) AND T2(LSB).

NOTE: CLOCK "DIVIDE BY" MODE (÷) ALLOWS FOR LOWER POWER FOR RS232 OR FASTER CPU EXECUTION WITH ZIE AT NORMAL 6 MHZ CLOCK RATE.

Figure 25. TCTLLO Register

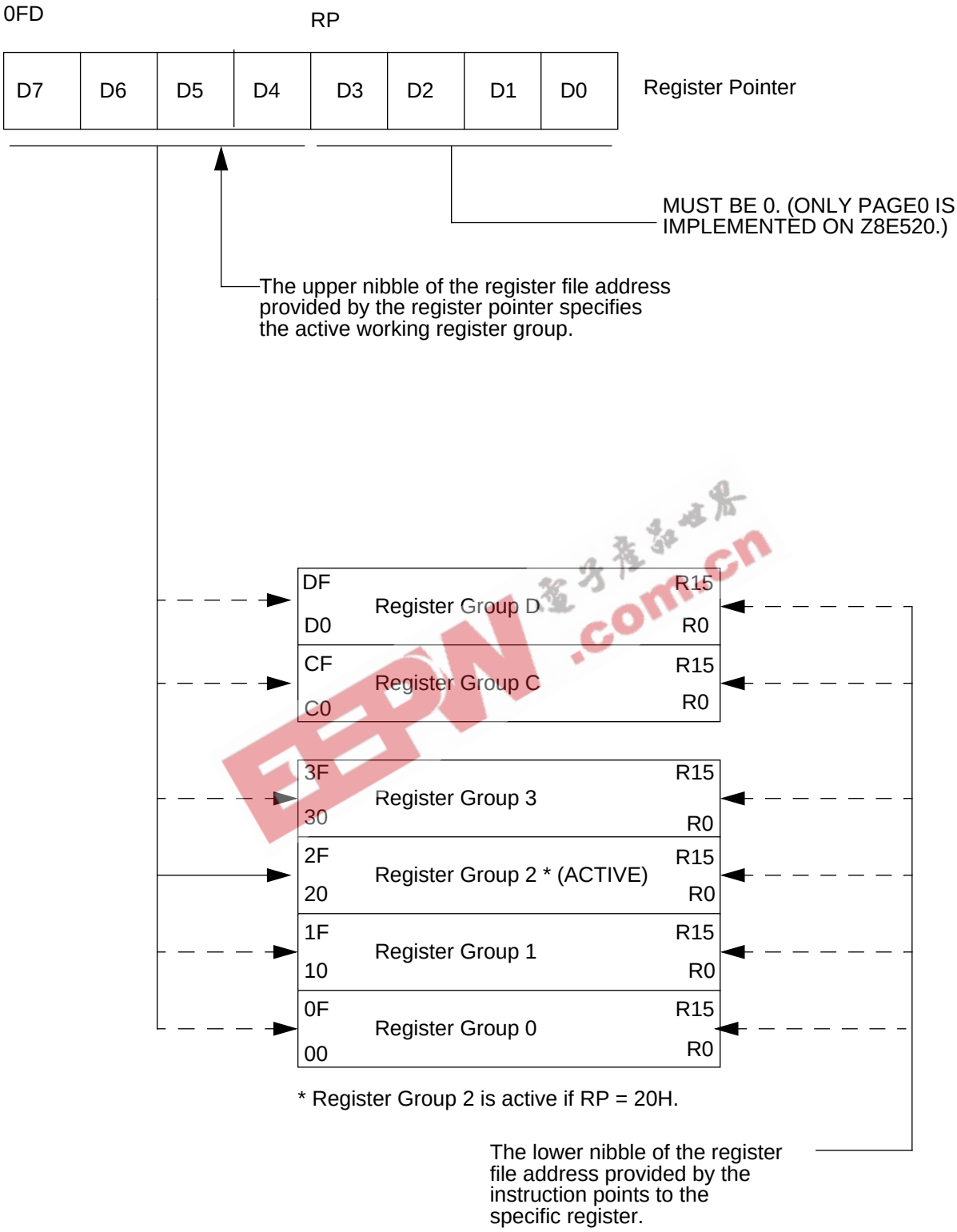


Figure 26. Z8E520 Register Pointe

Z8PLUS SYSTEM REGISTERS (Continued)

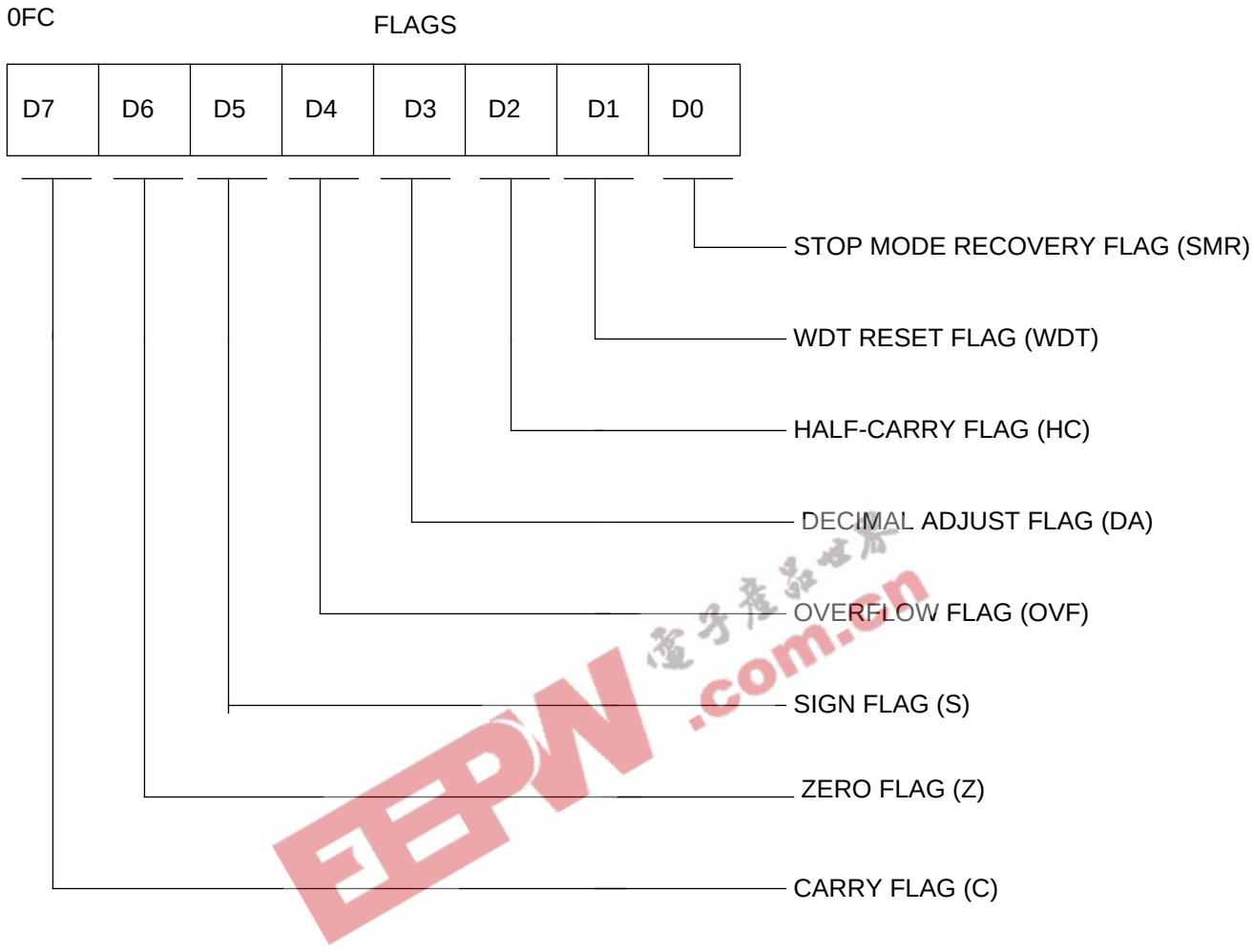
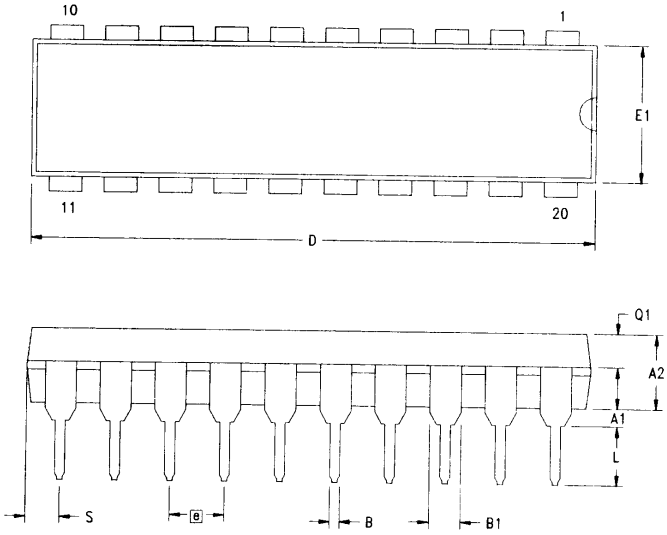


Figure 27. Flags Register

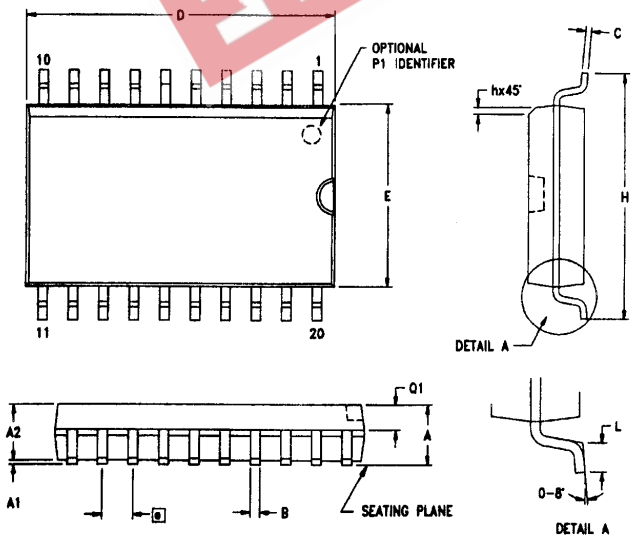
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

Figure 28. 20-Pin DIP Package



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	.496	.510
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 29. 20-Pin SOIC Package

ORDERING INFORMATION

6 MHz	6 MHz
20-Pin DIP	**20-Pin SOIC**
Z8E520PSC	Z8E520SSC
Z8C520PSC	Z8C520SSC

For fast results, contact your Zilog sales office for assistance in ordering the part required.

CODES

Package
P = Plastic DIP
V = Plastic Leaded Chip Carrier
F = Quad Flat Pack

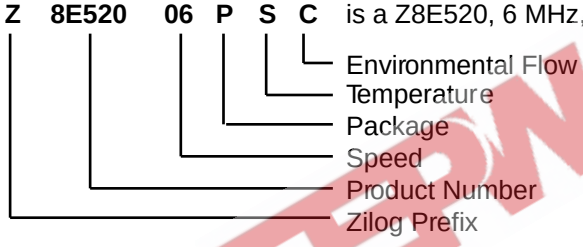
Speed
06 = 6 MHz

Environment
C = Plastic Standard

Temperature
S = 0°C to +70°C

Example:

Z 8E520 06 P S C is a Z8E520, 6 MHz, SOIC, 0°C to +70°C, Plastic Standard Flow



Development Projects:

Customer is cautioned that while reasonable efforts will be employed to meet performance objectives and milestone dates, development is subject to unanticipated problems and delays. No production release is authorized or committed until the Customer and Zilog have agreed upon a Customer Procurement Specification for this product.

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or nonconformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Low Margin:

Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgment, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com