

**Features**

- 128Kx8-bit Organization
- Address Access Time: 45, 70, 90 ns
- Single 5V  $\pm$  10% Power Supply
- Sector Erase Mode Operation
- 8KB Boot Block (lockable)
- 512 bytes per Sector, 256 Sectors
  - Sector-Erase Cycle Time: 10ms (Max)
  - Byte-Program Cycle Time: 20 $\mu$ s (Max)
- Minimum 10,000 Erase-Program Cycles
- Low power dissipation
  - Active Read Current: 20mA (Typ)
  - Active Program Current: 30mA (Typ)
  - Standby Current: 100 $\mu$ A (Max)
- Hardware Data Protection
- Low V<sub>CC</sub> Program Inhibit Below 2.5V
- Self-timed program/erase operations with end-of-cycle detection
  - $\overline{\text{DATA}}$  Polling
  - Toggle Bit
- CMOS and TTL Interface
- Available in two versions
  - V29C51001T (Top Boot Block)
  - V29C51001B (Bottom Boot Block)
- Packages:
  - 32-pin Plastic DIP
  - 32-pin TSOP-I
  - 32-pin PLCC

**Description**

The V29C51001T/V29C51001B is a high speed 131,072 x 8 bit CMOS flash memory. Programming or erasing the device is done with a single 5 Volt power supply. The device has separate chip enable CE, program enable WE, and output enable OE controls to eliminate bus contention.

The V29C51001T/V29C51001B offers a combination of features: Boot Block with Sector Erase Mode. The end of program/erase cycle is detected by DATA Polling of I/O<sub>7</sub> or by the Toggle Bit I/O<sub>6</sub>.

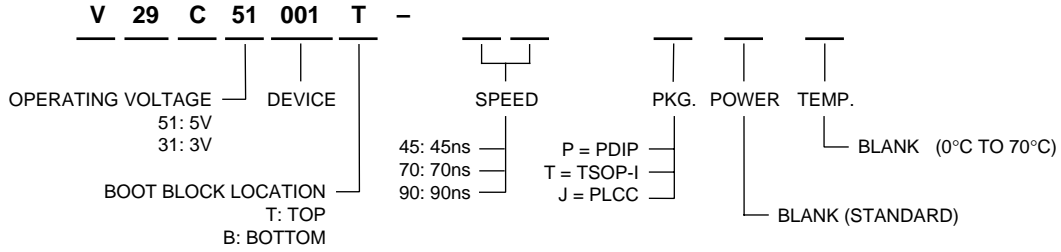
The V29C51001T/V29C51001B features a sector erase operation which allows each sector to be erased and reprogrammed without affecting data stored in other sectors. The device also supports full chip erase.

Boot block architecture enables the device to boot from a protected sector loaded either at the top (V29C51001T) or the bottom (V29C51001B) sector. All inputs and outputs are CMOS and TTL compatible.

The V29C51001T/V29C51001B is ideal for applications that require updatable code and data storage.

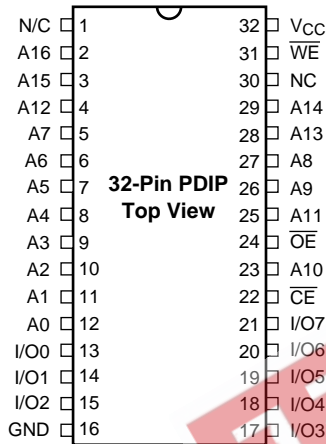
**Device Usage Chart**

Operating Temperature Range	Package Outline			Access Time (ns)			Power	Temperature Mark
	P	T	J	45	70	90	Std.	
0°C to 70°C	•	•	•	•	•	•	•	Blank



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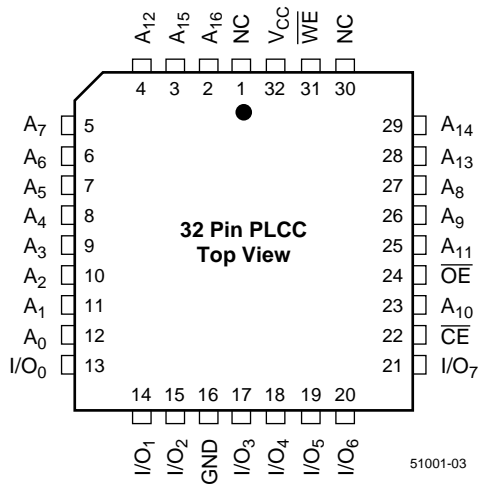
**Pin Configurations**



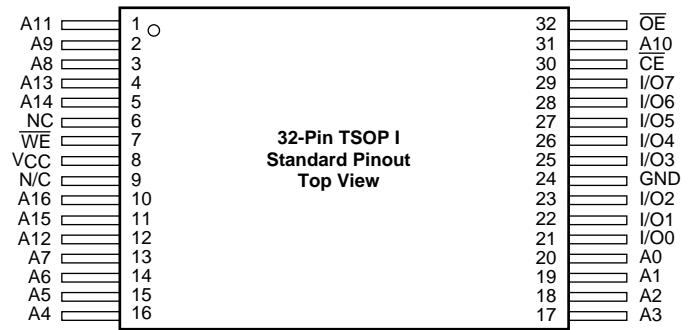
51001-02

**Pin Names**

A <sub>0</sub> -A <sub>16</sub>	Address Inputs
I/O <sub>0</sub> -I/O <sub>7</sub>	Data Input/Output
CE	Chip Enable
OE	Output Enable
WE	Program Enable
V <sub>CC</sub>	5V ± 10% Power Supply
GND	Ground
NC	No Connect

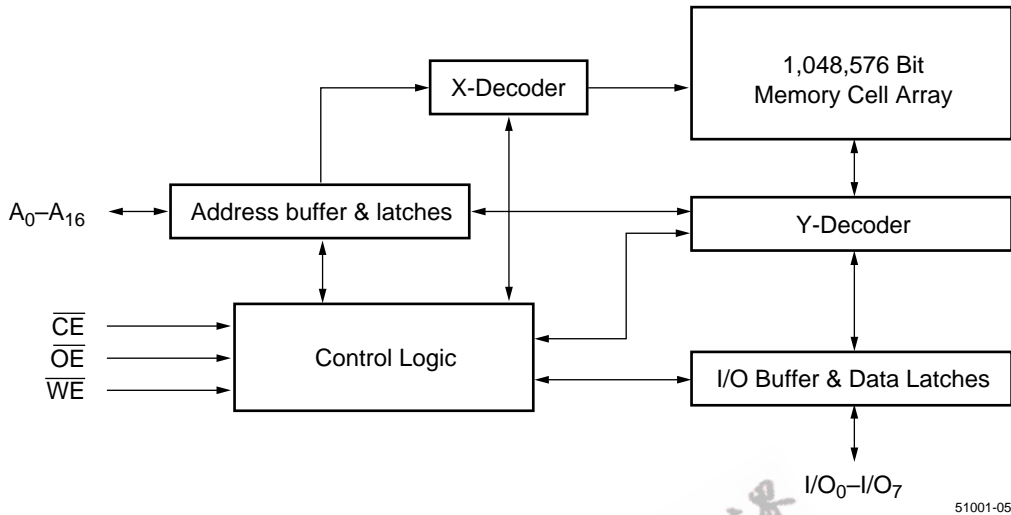


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**Functional Block Diagram**



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**Capacitance (1,2)**

Symbol	Parameter	Test mSetup	Typ.	Max.	Units
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0	6	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0	8	12	pF
C <sub>IN2</sub>	Control Pin Capacitance	V <sub>IN</sub> = 0	8	10	pF

**NOTE:**

1. Capacitance is sampled and not 100% tested.
2. T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5V ± 10%, f = 1 MHz.

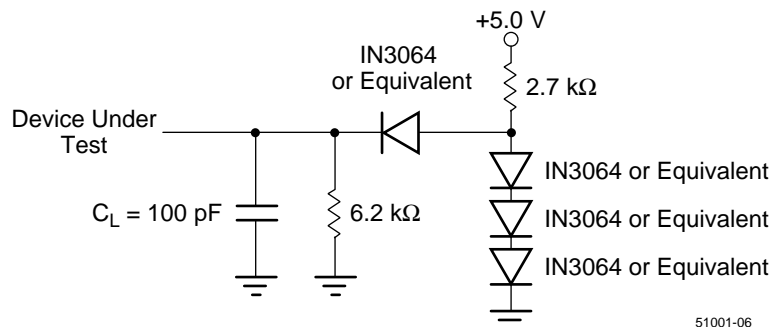
**Latch Up Characteristics<sup>(1)</sup>**

Parameter	Min.	Max.	Unit
Input Voltage with Respect to GND on A <sub>9</sub> , $\overline{OE}$	-1	+13	V
Input Voltage with Respect to GND on I/O, address or control pins	-1	V <sub>CC</sub> + 1	V
V <sub>CC</sub> Current	-100	+100	mA

**NOTE:**

1. Includes all pins except V<sub>CC</sub>. Test conditions: V<sub>CC</sub> = 5V, one pin at a time.

**AC Test Load**



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**Absolute Maximum Ratings<sup>(1)</sup>**

Symbol	Parameter	Commercial	Unit
$V_{IN}$	Input Voltage (input or I/O pins)	-2 to +7	V
$V_{IN}$	Input Voltage ( $A_9$ pin, $\overline{OE}$ )	-2 to +13	V
$V_{CC}$	Power Supply Voltage	-0.5 to +5.5	V
$T_{STG}$	Storage Temperature (Plastic)	-65 to +125	°C
$T_{OPR}$	Operating Temperature	0 to +70	°C
$I_{OUT}$	Short Circuit Current <sup>(2)</sup>	200 (Max.)	mA

**NOTE:**

- Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- No more than one output maybe shorted at a time and not exceeding one second long.

**DC Electrical Characteristics**

(over the commercial operating range)

Parameter Name	Parameter	Test Conditions	Min.	Max.	Unit
$V_{IL}$	Input LOW Voltage	$V_{CC} = V_{CC} \text{ Min.}$	—	0.8	V
$V_{IH}$	Input HIGH Voltage	$V_{CC} = V_{CC} \text{ Max.}$	2	—	V
$I_{IL}$	Input Leakage Current	$V_{IN} = \text{GND to } V_{CC}, V_{CC} = V_{CC} \text{ Max.}$	—	$\pm 1$	$\mu\text{A}$
$I_{OL}$	Output Leakage Current	$V_{OUT} = \text{GND to } V_{CC}, V_{CC} = V_{CC} \text{ Max.}$	—	$\pm 1$	$\mu\text{A}$
$V_{OL}$	Output LOW Voltage	$V_{CC} = V_{CC} \text{ Min.}, I_{OL} = 2.1\text{mA}$	—	0.4	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = V_{CC} \text{ Min.}, I_{OH} = -400\mu\text{A}$	2.4	—	V
$I_{CC1}$	Read Current	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH},$ all I/Os open, Address input = $V_{IL}/V_{IH}$ , at $f = 1/t_{RC} \text{ Min.},$ $V_{CC} = V_{CC} \text{ Max.}$	—	40	mA
$I_{CC2}$	Program Current	$\overline{CE} = \overline{WE} = V_{IL}, \overline{OE} = V_{IH}, V_{CC} = V_{CC} \text{ Max.}$	—	50	mA
$I_{SB}$	TTL Standby Current	$\overline{CE} = \overline{OE} = \overline{WE} = V_{IH}, V_{CC} = V_{CC} \text{ Max.}$	—	2	mA
$I_{SB1}$	CMOS Standby Current	$\overline{CE} = \overline{OE} = \overline{WE} = V_{CC} - 0.3\text{V}, V_{CC} = V_{CC} \text{ Max.}$	—	150	$\mu\text{A}$
$V_H$	Device ID Voltage for $A_9$	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	11.5	12.5	V
$I_H$	Device ID Current for $A_9$	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}, A_9 = V_H \text{ Max.}$	—	50	$\mu\text{A}$

**AC Electrical Characteristics**

(over all temperature ranges)

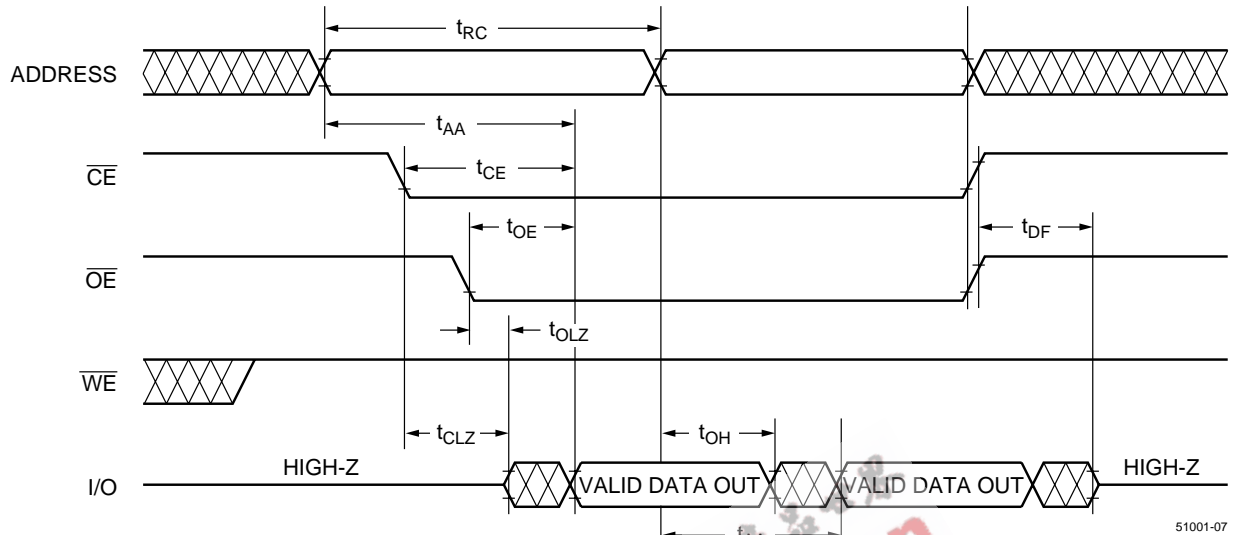
**Read Cycle**

Parameter Name	Parameter	-45		-70		-90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	45	—	70	—	90	—	ns
t <sub>AA</sub>	Address Access Time	—	45	—	70	—	90	ns
t <sub>CE</sub>	Chip Enable Access Time	—	45	—	70	—	90	ns
t <sub>OE</sub>	Output Enable Access Time	—	25	—	35	—	45	ns
t <sub>CLZ</sub>	$\overline{\text{CE}}$ Low to Output Active	0	—	0	—	0	—	ns
t <sub>OLZ</sub>	$\overline{\text{OE}}$ Low to Output Active	0	—	0	—	0	—	ns
t <sub>DF</sub>	Output Enable or Chip Disable to Output in High Z	0	15	0	20	0	30	ns
t <sub>OH</sub>	Output Hold from Address Change	0	—	0	—	0	—	ns

**Program (Erase/Program) Cycle**

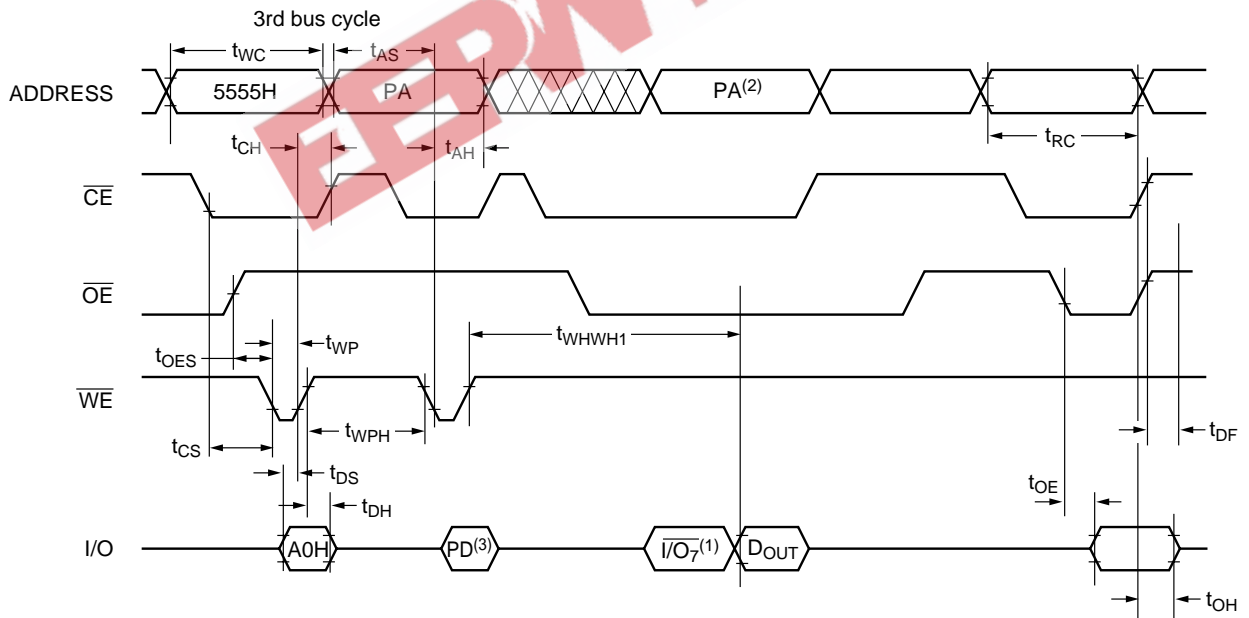
Parameter Name	Parameter	-45			-70			-90			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t <sub>WC</sub>	Program Cycle Time	45	—	—	70	—	—	90	—	—	ns
t <sub>AS</sub>	Address Setup Time	0	—	—	0	—	—	0	—	—	ns
t <sub>AH</sub>	Address Hold Time	35	—	—	45	—	—	45	—	—	ns
t <sub>CS</sub>	$\overline{\text{CE}}$ Setup Time	0	—	—	0	—	—	0	—	—	ns
t <sub>CH</sub>	$\overline{\text{CE}}$ Hold Time	0	—	—	0	—	—	0	—	—	ns
t <sub>OES</sub>	$\overline{\text{OE}}$ Setup Time	0	—	—	0	—	—	0	—	—	ns
t <sub>OEH</sub>	$\overline{\text{OE}}$ High Hold Time	0	—	—	0	—	—	0	—	—	ns
t <sub>WP</sub>	$\overline{\text{WE}}$ Pulse Width	25	—	—	35	—	—	45	—	—	ns
t <sub>WPH</sub>	$\overline{\text{WE}}$ Pulse Width High	20	—	—	35	—	—	38	—	—	ns
t <sub>DS</sub>	Data Setup Time	20	—	—	25	—	—	30	—	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	—	0	—	—	0	—	—	ns
t <sub>WHWH1</sub>	Programming Cycle	—	—	20	—	—	20	—	—	20	μs
t <sub>WHWH2</sub>	Sector Erase Cycle	—	—	10	—	—	10	—	—	10	ms
t <sub>WHWH3</sub>	Chip Erase Cycle	—	2	—	—	2	—	—	2	—	sec

**Waveforms of Read Cycle**



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**Waveforms of  $\overline{WE}$  Controlled-Program Cycle**

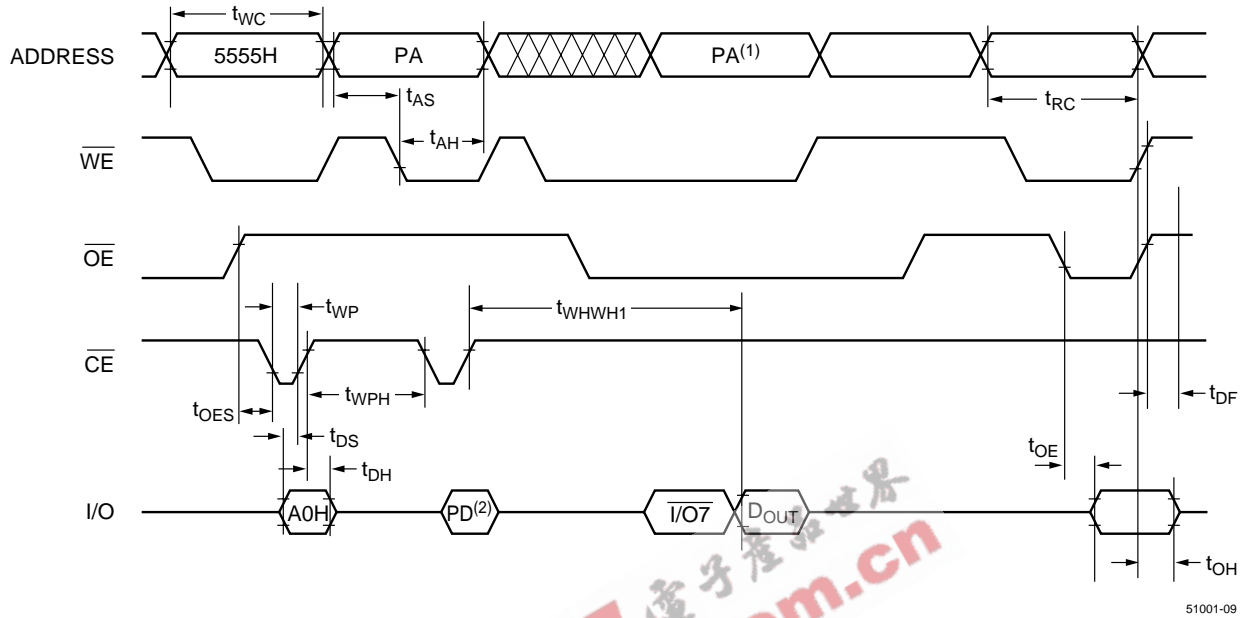


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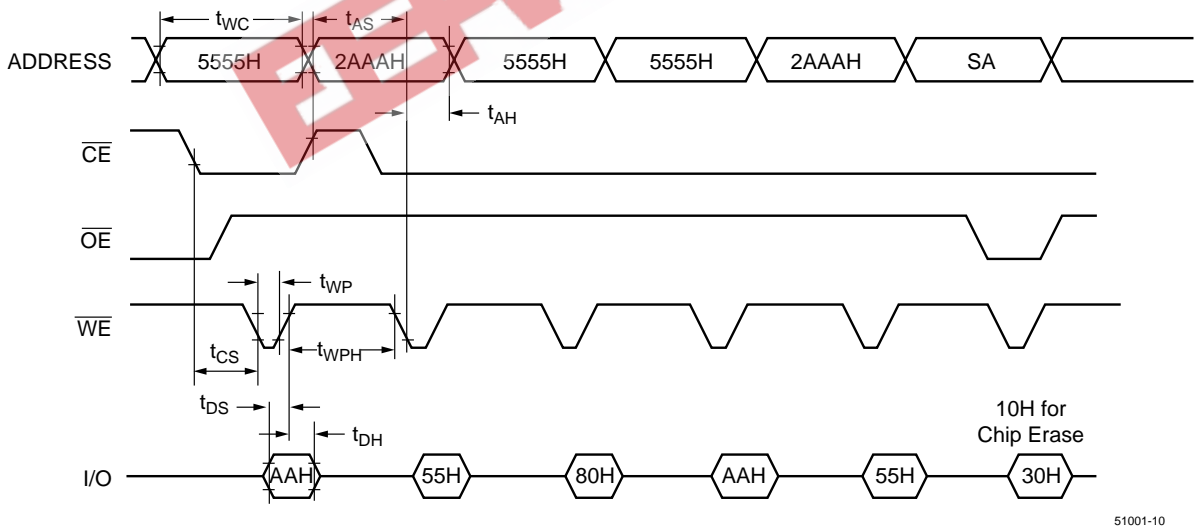
**NOTES:**

1. I/O<sub>7</sub>: The output is the complement of the data written to the device.
2. PA: The address of the memory location to be programmed.
3. PD: The data at the byte address to be programmed.

**Waveforms of CE Controlled-Program Cycle**



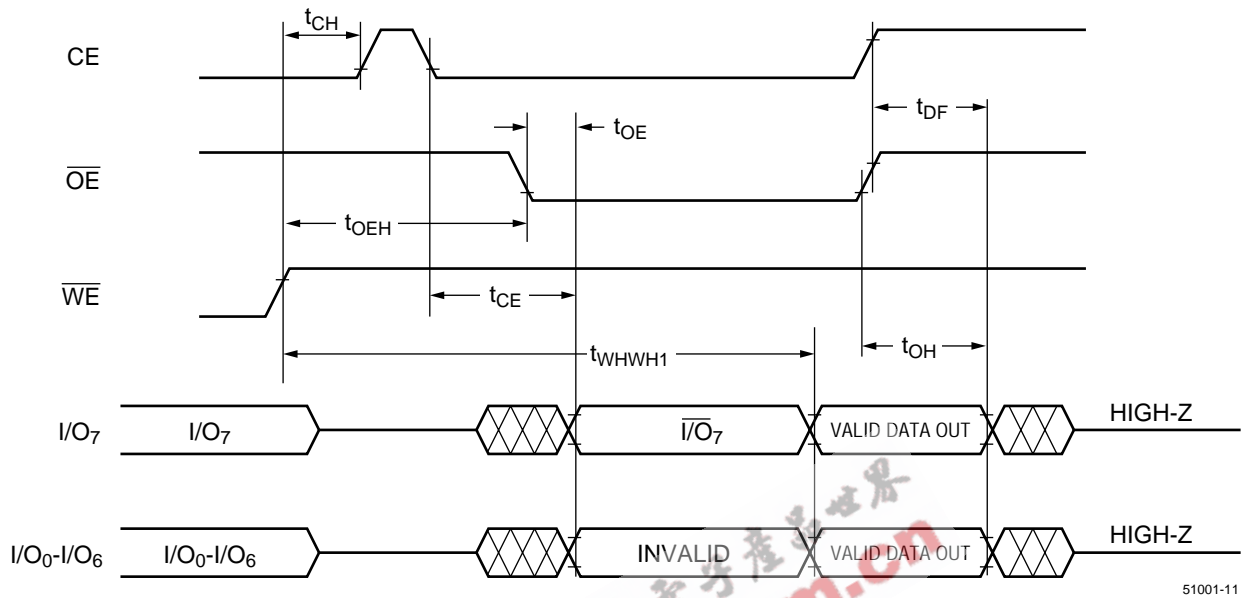
**Waveforms of Erase Cycle<sup>(1)</sup>**



**NOTES:**

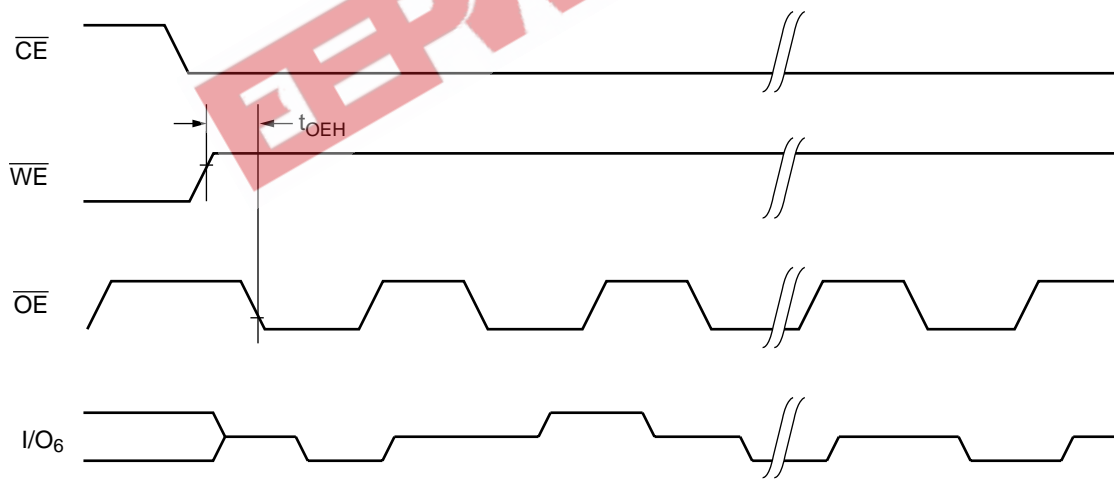
1. PA: The address of the memory location to be programmed.
2. PD: The data at the byte address to be programmed.
3. SA: The sector address for Sector Erase. Address = don't care for Chip Erase.

**Waveforms of  $\overline{DATA}$  Polling Cycle**



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**Waveforms of Toggle Bit Cycle**



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**Functional Description**

The V29C51001T/V29C51001B consists of 256 equally-sized sectors of 512 bytes each. The 8 KB lockable Boot Block is intended for storage of the system BIOS boot code. The boot code is the first piece of code executed each time the system is powered on or rebooted.

The V29C51001 is available in two versions: the V29C51001T with the Boot Block address starting from 1E000H to 1FFFFH, and the V29C51001B with the Boot Block address starting from 00000H to 1FFFFH.

**Read Cycle**

A read cycle is performed by holding both  $\overline{CE}$  and  $\overline{OE}$  signals LOW. Data Out becomes valid only when these conditions are met. During a read cycle  $\overline{WE}$  must be HIGH prior to  $\overline{CE}$  and  $\overline{OE}$  going LOW.  $\overline{WE}$  must remain HIGH during the read operation for the read to complete (see Table 1).

**Output Disable**

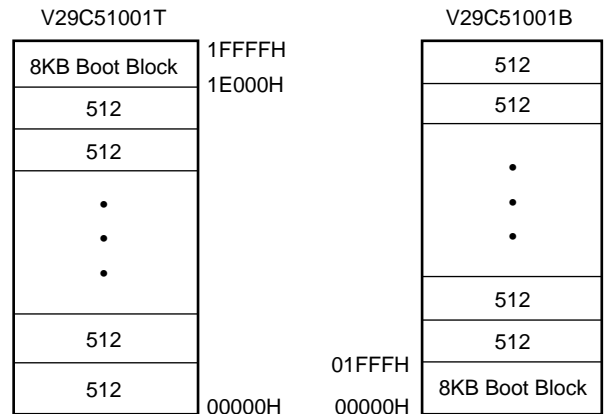
Returning  $\overline{OE}$  or  $\overline{CE}$  HIGH, whichever occurs first will terminate the read operation and place the I/O pins in the HIGH-Z state.

**Standby**

The device will enter standby mode when the  $\overline{CE}$  signal is HIGH. The I/O pins are placed in the HIGH-Z, independent of the  $\overline{OE}$  signal.

**Command Sequence**

The V29C51001T/V29C51001B does not provide the "reset" feature to return the chip to its normal state when an incomplete command



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**8KB Boot Block = 16 Sectors**

sequence or an interruption has happened. In this case, normal operation (Read Mode) can be restored by issuing a "non-existent" command sequence, for example Address: 5555H, Data FFH.

**Byte Program Cycle**

The V29C51001T/V29C51001B is programmed on a byte-by-byte basis. The byte program operation is initiated by using a specific four-bus-cycle sequence: two unlock program cycles, a program setup command and program data program cycles (see Table 2).

During the byte program cycle, addresses are latched on the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever is last. Data is latched on the rising edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever is first. The byte program cycle can be  $\overline{CE}$  controlled or  $\overline{WE}$  controlled.

**Table 1. Operation Modes Decoding**

Decoding Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A <sub>0</sub>	A <sub>1</sub>	A <sub>9</sub>	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	A <sub>0</sub>	A <sub>1</sub>	A <sub>9</sub>	READ
Byte Write	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	A <sub>0</sub>	A <sub>1</sub>	A <sub>9</sub>	PD
Standby	V <sub>IH</sub>	X	X	X	X	X	HIGH-Z
Autoselect Device ID	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>H</sub>	CODE
Autoselect Manufacture ID	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>H</sub>	CODE
Enabling Boot Block Protection Lock	V <sub>IL</sub>	V <sub>H</sub>	V <sub>IL</sub>	X	X	V <sub>H</sub>	X
Disabling Boot Block Protection Lock	V <sub>H</sub>	V <sub>H</sub>	V <sub>IL</sub>	X	X	V <sub>H</sub>	X
Output Disable	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	X	X	HIGH-Z

**NOTES:**

1. X = Don't Care, V<sub>IH</sub> = HIGH, V<sub>IL</sub> = LOW. V<sub>H</sub> = 12.5V Max.
2. PD: The data at the byte address to be programmed.

**Table 2. Command Codes**

Command Sequence	First Bus Program Cycle		Second Bus Program Cycle		Third Bus Program Cycle		Fourth Bus Program Cycle		Fifth Bus Program Cycle		Six Bus Program Cycle	
	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read	XXXXH	F0H										
Read	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	5555H	AAH	2AAAH	55H	5555H	90H	00H	40H				
							01H	01H <sup>(1)</sup> A1H <sup>(2)</sup>				
Byte Program	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD <sup>(4)</sup>				
Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	PA <sup>(3)</sup>	30H

**NOTES:**

1. Top Boot Sector
2. Bottom Boot Sector
3. PA: The address of the memory location to be programmed.
4. PD: The data at the byte address to be programmed.

**Sector Erase Cycle**

The V29C51001T/V29C51001B features a sector erase operation which allows each sector to be erased and reprogrammed without affecting data stored in other sectors. Sector erase operation is initiated by using a specific six-bus-cycle sequence: Two unlock program cycles, a setup command, two additional unlock program cycles, and the sector erase command (see Table 2). A sector must be first erased before it can be reprogrammed. While in the internal erase mode, the device ignores any program attempt into the device. The internal erase completion can be determined via DATA polling or toggle bit.

The V29C51001T/V29C51001B is shipped with pre-erased sectors (all bits = 1).

**Chip Erase Cycle**

The V29C51001T/V29C51001B features a chip-erase operation. The chip erase operation is initiated by using a specific six-bus-cycle sequence: two unlock program cycles, a setup command, two additional unlock program cycles, and the chip erase command (see Table 2).

The chip erase operation is performed sequentially, one sector at a time. When the automated on chip erase algorithm is requested with the chip erase command sequence, the device automatically programs and verifies the entire memory array for an all zero pattern prior to erasure

The automatic erase begins on the rising edge of the last  $\overline{WE}$  or  $\overline{CE}$  pulse in the command sequence and terminates when the data on DQ7 is "1".

**Program Cycle Status Detection**

There are two methods for determining the state of the V29C51001T/V29C51001B during a program (erase/program) cycle:  $\overline{DATA}$  Polling (I/O<sub>7</sub>) and Toggle Bit (I/O<sub>6</sub>).

 **$\overline{DATA}$  Polling (I/O<sub>7</sub>)**

The V29C51001T/V29C51001B features  $\overline{DATA}$  polling to indicate the end of a program cycle. When the device is in the program cycle, any attempt to read the device will receive the complement of the loaded data on I/O<sub>7</sub>. Once the program cycle is completed, I/O<sub>7</sub> will show true data, and the device is then ready for the next cycle.

**Toggle Bit (I/O<sub>6</sub>)**

The V29C51001T/V29C51001B also features another method for determining the end of a program cycle. When the device is in the program cycle, any attempt to read the device will result in I/O<sub>6</sub> toggling between 1 and 0. Once the program is completed, the toggling will stop. The device is then ready for the next operation. Examining the toggle bit may begin at any time during a program cycle.

### Boot Block Protection

The V29C51001T/V29C51001B features hardware Boot Block Protection. The boot block sector protection is enabled when high voltage (12.5V) is applied to  $\overline{OE}$  and A9 pins with  $\overline{CE}$  pin LOW and  $\overline{WE}$  pin IOW. The sector protection is disabled when high voltage is applied to  $\overline{OE}$ ,  $\overline{CE}$  and A9 pins with  $\overline{WE}$  pin LOW. Other pins can be HIGH or LOW. This is shown in table 1.

### Autoselect

The V29C51001T/V29C51001B features an Autoselect mode to identify the *Boot Block (protected/unprotected), the Device (Top/Bottom), and the manufacturer ID.*

To get to the Autoselect mode, a high voltage ( $V_H$ ) must be applied to the A<sub>9</sub> pin. Once the A<sub>9</sub> signal is returned to LOW or HIGH, the device will return to the previous mode.

### Boot Block Protection Status

In Autoselect mode, performing a read at address XXX2H will indicate if the Top Boot Block sector or the Bottom Boot Block sector is locked out. If the data is 01H, the Top/Bottom Boot Block is protected. If the data is 00H, the Top/Bottom Boot Block is unprotected. (see Table 3.)

### Device ID

In Autoselect mode, performing a read at address XXX1H will determine whether the device is a Top Boot Block device or a Bottom Boot Block device. If the data is 01H, the device is a Top Boot Block. If the data is A1H, the device is a Bottom Boot Block device (see Table 3).

In addition, the device ID can also be read via the command register when the device is erased or programmed in a system without applying high voltage to the A<sub>9</sub> pin. When A<sub>0</sub> is HIGH, the device ID is presented at the outputs.

### Manufacturer ID

In Autoselect mode, performing a read at address XXXX0H will determine the manufacturer ID. 40H is the manufacturer code for Mosel Vitelic Flash.

In addition the manufacturer ID can also be read via the command register when the device is erased or programmed in a system without applying high voltage to the A<sub>9</sub> pin. when A<sub>0</sub> is LOW, the manufacturer ID is presented at the outputs.

### Hardware Data Protection

*V<sub>CC</sub> Sense Protection:* the program operation is inhibited when VCC is less than 2.5V.

*Noise Protection:* a CE or WE pulse of less than 5ns will not initiate a program cycle.

*Program Inhibit Protection:* holding any one of OE LOW, CE HIGH or WE HIGH inhibits a program cycle.

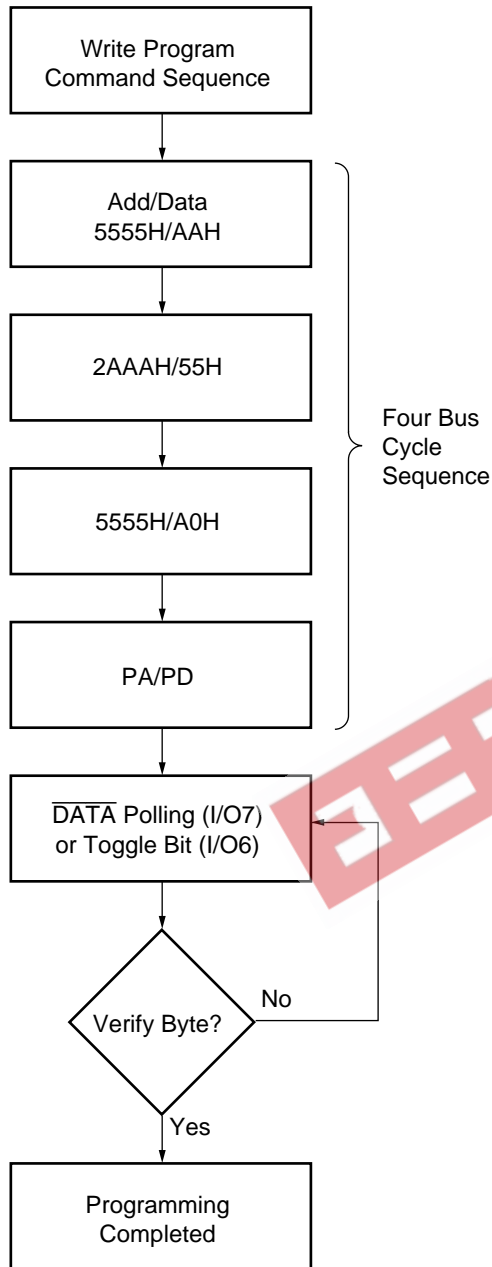
**Table 3. Autoselect Decoding**

Decoding Mode	Boot Block	Address				Data I/O <sub>0</sub> -I/O <sub>7</sub>
		A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub> -A <sub>13</sub>	A <sub>14</sub> -A <sub>16</sub>	
Boot Block Protection	Top	V <sub>IL</sub>	V <sub>IH</sub>	X	X	01H: protected
	Bottom	V <sub>IL</sub>	V <sub>IH</sub>	X	X	00H: unprotected
Device ID	Top	V <sub>IH</sub>	V <sub>IL</sub>	X	X	01H
	Bottom					A1H
Manufacture ID		V <sub>IL</sub>	V <sub>IL</sub>	X	X	40H

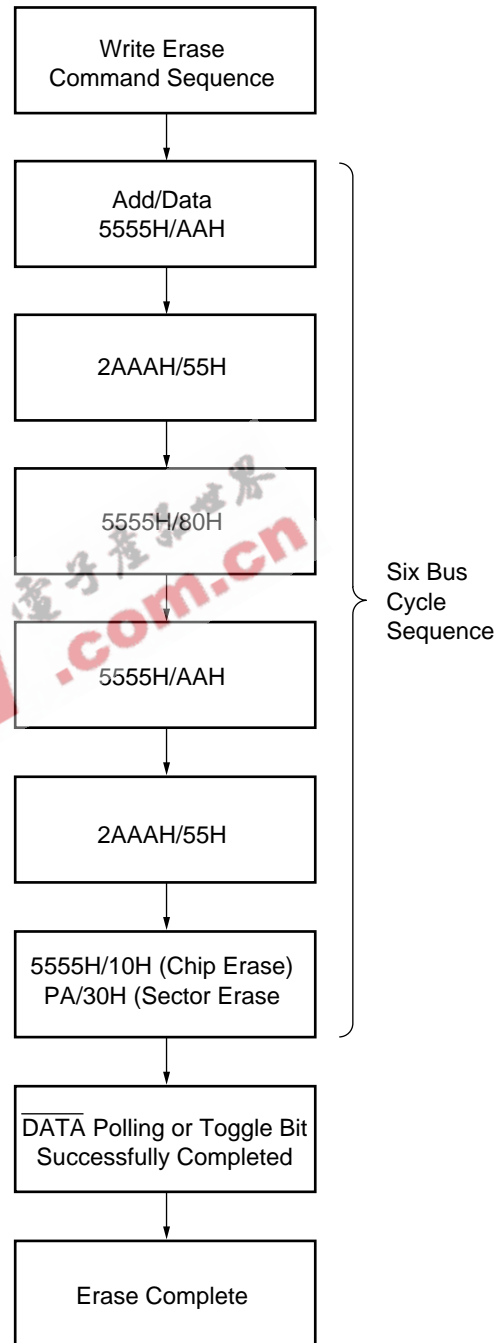
**NOTE:**

1. X = Don't Care, V<sub>IH</sub> = HIGH, V<sub>IL</sub> = LOW.

**Byte Program Algorithm**

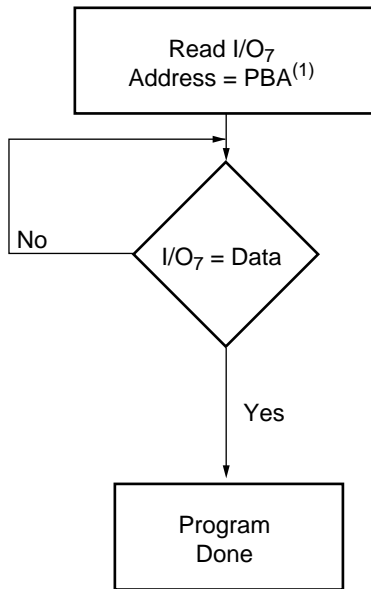


**Chip/Sector Erase Algorithm**

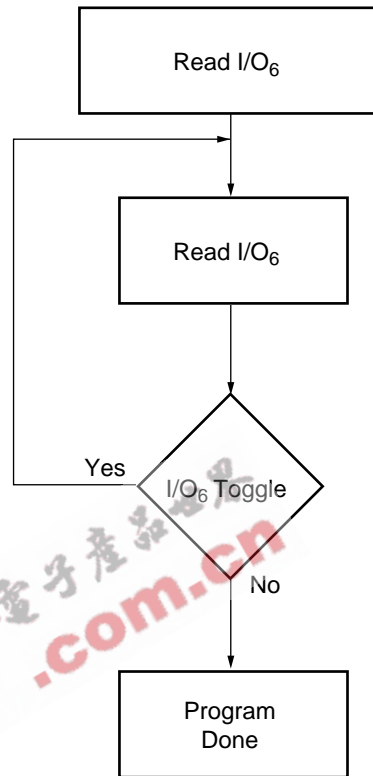


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**DATA Polling Algorithm**



**Toggle Bit Algorithm**



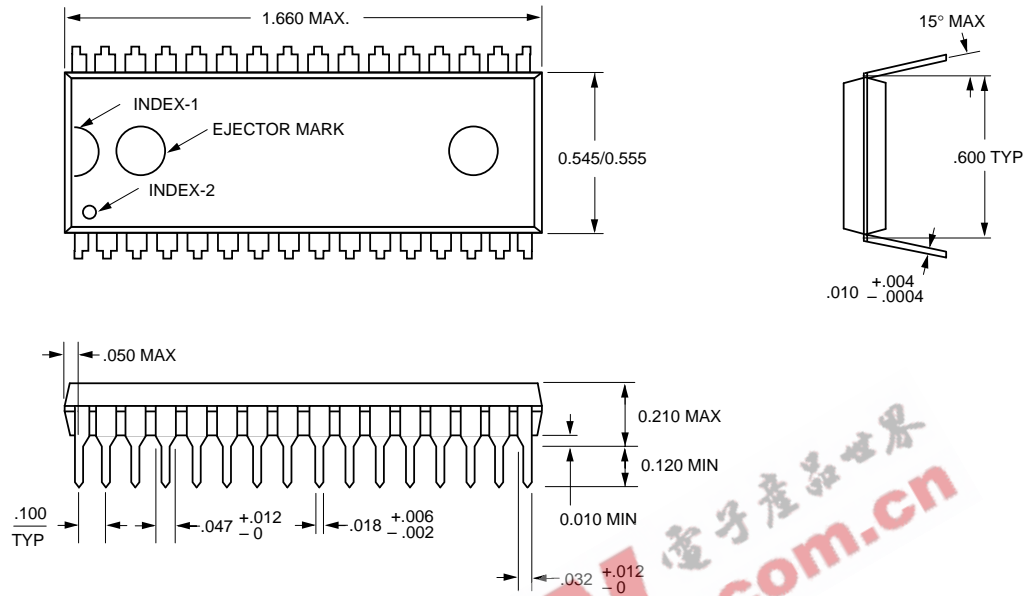
**NOTE:**

1. PBA: The byte address to be programmed.

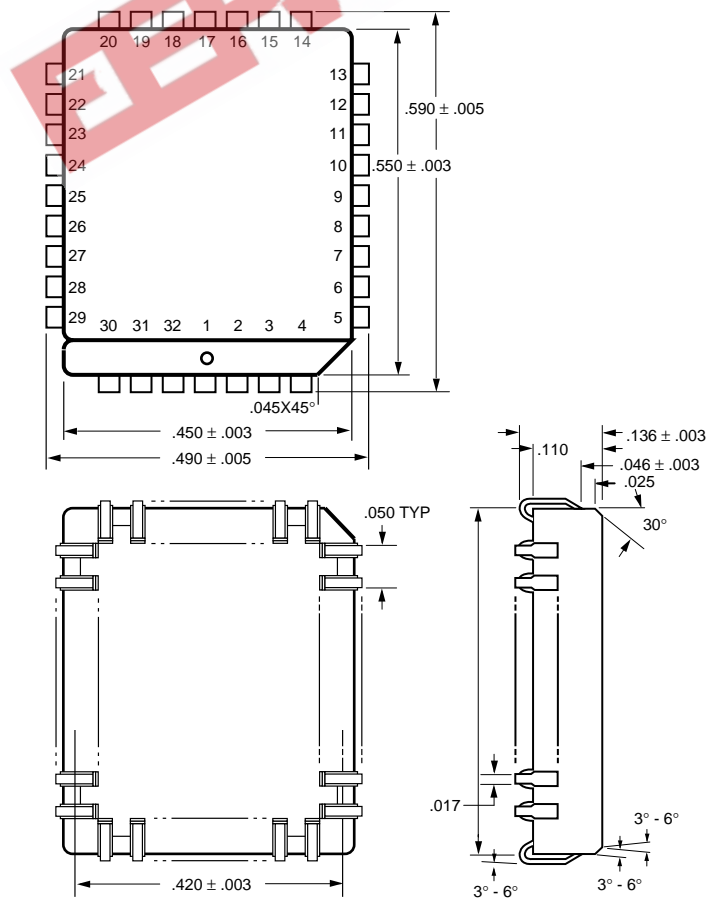
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**Package Diagrams**

**32-pin Plastic DIP**

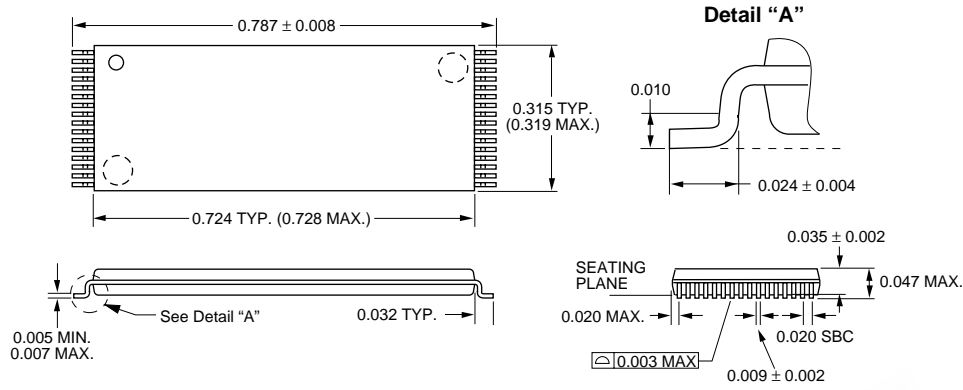


**32-pin PLCC**



32-pin TSOP-I

Units in inches



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