Lattice Semiconductor Corporation

ispGDX™*240VA*

In-System Programmable
## 3.3V Generic Digital Crosspoint™

Features

- **IN-SYSTEM PROGRAMMABLE GENERIC DIGITAL CROSSPOINT FAMILY**
  - **Advanced Architecture Addresses Programmable PCB Interconnect, Bus Interface Integration and Jumper/Switch Replacement**
  - **"Any Input to Any Output" Routing**
  - **Fixed HIGH or LOW Output Option for Jumper/DIP Switch Emulation**
  - **Space-Saving PQFP and BGA Packaging**
  - **Dedicated IEEE 1149.1-Compliant Boundary Scan Test**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **3.3V Core Power Supply**
  - **4.5ns Input-to-Output/4.5ns Clock-to-Output Delay**
  - **200MHz Maximum Clock Frequency**
  - **TTL/3.3V/2.5V Compatible Input Thresholds and Output Levels (Individually Programmable)**
  - **Low-Power: 16.5mA Quiescent Icc**
  - **24mA I_{OL} Drive with Programmable Slew Rate Control Option**
  - **PCI Compatible Drive Capability**
  - **Schmitt Trigger Inputs for Noise Immunity**
  - **Electrically Erasable and Reprogrammable**
  - **Non-Volatile E²CMOS Technology**
- **ispGDXVA™ OFFERS THE FOLLOWING ADVANTAGES**
  - **3.3V In-System Programmable Using Boundary Scan Test Access Port (TAP)**
  - **Change Interconnects in Seconds**
- **FLEXIBLE ARCHITECTURE**
  - **Combinatorial/Latched/Registered Inputs or Outputs**
  - **Individual I/O Tri-state Control with Polarity Control**
  - **Dedicated Clock/Clock Enable Input Pins (four) or Programmable Clocks/Clock Enables from I/O Pins (60)**
  - **Single Level 4:1 Dynamic Path Selection (Tpd = 4.5ns)**
  - **Programmable Wide-MUX Cascade Feature Supports up to 16:1 MUX**
  - **Programmable Pull-ups, Bus Hold Latch and Open Drain on I/O Pins**
  - **Outputs Tri-state During Power-up ("Live Insertion" Friendly)**
- **DESIGN SUPPORT THROUGH LATTICE'S ispGDX DEVELOPMENT SOFTWARE**
  - **MS Windows or NT / PC-Based or Sun O/S**
  - **Easy Text-Based Design Entry**
  - **Automatic Signal Routing**
  - **Program up to 100 ISP Devices Concurrently**
  - **Simulator Netlist Generation for Easy Board-Level Simulation**

Functional Block Diagram
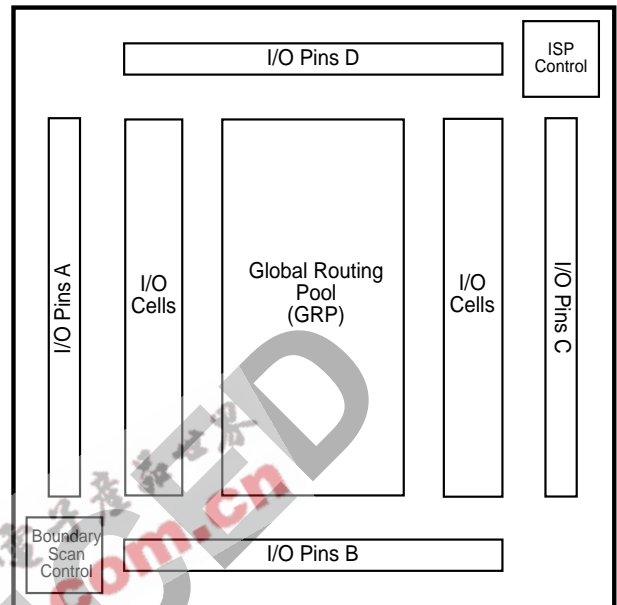
Description

The ispGDXVA architecture provides a family of fast, flexible programmable devices to address a variety of system-level digital signal routing and interface requirements including:

- Multi-Port Multiprocessor Interfaces
- Wide Data and Address Bus Multiplexing (e.g. 16:1 High-Speed Bus MUX)
- Programmable Control Signal Routing (e.g. Interrupts, DMAREQs, etc.)
- Board-Level PCB Signal Routing for Prototyping or Programmable Bus Interfaces

The devices feature fast operation, with input-to-output signal delays (Tpd) of 4.5ns and clock-to-output delays of 4.5ns.

The architecture of the devices consists of a series of programmable I/O cells interconnected by a Global Routing Pool (GRP). All I/O pin inputs enter the GRP directly or are registered or latched so they can be routed to the required I/O outputs. I/O pin inputs are defined as four sets (A,B,C,D) which have access to the four MUX inputs

September 2000

Description (Continued)

found in each I/O cell. Each output has individual, programmable I/O tri-state control (OE), output latch clock (CLK), clock enable (CLKEN), and two multiplexer control (MUX0 and MUX1) inputs. Polarity for these signals is programmable for each I/O cell. The MUX0 and MUX1 inputs control a fast 4:1 MUX, allowing dynamic selection of up to four signal sources for a given output. A wider 16:1 MUX can be implemented with the MUX expander feature of each I/O and a propagation delay increase of 2.0ns. OE, CLK, CLKEN, and MUX0 and MUX1 inputs can be driven directly from selected sets of I/O pins. Optional dedicated clock input pins give minimum clock-to-output delays. CLK and CLKEN share the same set of I/O pins. CLKEN disables the register clock when CLKEN = 0.

Through in-system programming, connections between I/O pins and architectural features (latched or registered inputs or outputs, output enable control, etc.) can be defined. In keeping with its data path application focus, the ispGDXVA devices contain no programmable logic arrays. All input pins include Schmitt trigger buffers for noise immunity. These connections are programmed into the device using non-volatile E^2CMOS technology. Non-volatile technology means the device configuration is saved even when the power is removed from the device.

In addition, there are no pin-to-pin routing constraints for 1:1 or 1:n signal routing. That is, *any* I/O pin configured as an input can drive one or more I/O pins configured as outputs.

The device pins also have the ability to set outputs to fixed HIGH or LOW logic levels (Jumper or DIP Switch mode). Device outputs are specified for 24mA sink and 12mA source current (at JEDEC LVTTL levels) and can be tied together in parallel for greater drive. On the ispGDXVA, each I/O pin is individually programmable for 3.3V or 2.5V output levels as described later. Programmable output slew rate control can be defined independently for each I/O pin to reduce overall ground bounce and switching noise.

All I/O pins are equipped with IEEE1149.1-compliant Boundary Scan Test circuitry for enhanced testability. In addition, in-system programming is supported through the Test Access Port via a special set of private commands.

The ispGDXVA I/Os are designed to withstand "live insertion" system environments. The I/O buffers are disabled during power-up and power-down cycles. When designing for "live insertion," absolute maximum rating conditions for the Vcc and I/O pins must still be met.

Table 1. ispGDXV/VA Family Members

	ispGDXV/VA Device		
	ispGDX80VA	ispGDX160V/VA	ispGDX240VA
I/O Pins	80	160	240
I/O-OE Inputs*	20	40	60
I/O-CLK / CLKEN Inputs*	20	40	60
I/O-MUXsel1 Inputs*	20	40	60
I/O-MUXsel2 Inputs*	20	40	60
Dedicated Clock Pins**	2	4	4
EPEN	1	1	1
TOE	1	1	1
BSCAN Interface	4	4	4
RESET	1	1	1
Pin Count/Package	100-Pin TQFP	208-Pin PQFP 208-Ball fpBGA 272-Ball BGA	388-Ball fpBGA

* The CLK/CLK_EN, OE, MUX0 and MUX1 terminals on each I/O cell can each be assigned to 25% of the I/Os.

** Global clock pins Y0, Y1, Y2 and Y3 are multiplexed with CLKEN0, CLKEN1, CLKEN2 and CLKEN3 respectively in all devices.

Architecture

The ispGDXVA architecture is different from traditional PLD architectures, in keeping with its unique application focus. The block diagram is shown below. The programmable interconnect consists of a single Global Routing Pool (GRP). Unlike ispLSI devices, there are no programmable logic arrays on the device. Control signals for OEs, Clocks/Clock Enables and MUX Controls must come from designated sets of I/O pins. The polarity of these signals can be independently programmed in each I/O cell.

Each I/O cell drives a unique pin. The OE control for each I/O pin is independent and may be driven via the GRP by one of the designated I/O pins (I/O-OE set). The I/O-OE set consists of 25% of the total I/O pins. Boundary Scan test is supported by dedicated registers at each I/O pin. In-system programming is accomplished through the standard Boundary Scan protocol.

The various I/O pin sets are also shown in the block diagram below. The A, B, C, and D I/O pins are grouped together with one group per side.

I/O Architecture

Each I/O cell contains a 4:1 dynamic MUX controlled by two select lines as well as a 4x4 crossbar switch controlled by software for increased routing flexiability (Figure 1). The four data inputs to the MUX (called M0, M1, M2, and M3) come from I/O signals in the GRP and/or adjacent I/O cells. Each MUX data input can access one quarter of the total I/Os. For example, in a 240-I/O ispGDXVA, each data input can connect to one of 60 I/O pins. MUX0 and MUX1 can be driven by designated I/O pins called MUXsel1 and MUXsel2. Each MUXsel input covers 25% of the total I/O pins (e.g. 60 out of 240). MUX0 and MUX1 can be driven from either MUXsel1 or MUXsel2.

Figure 1. ispGDXVA I/O Cell and GRP Detail (240 I/O Device)
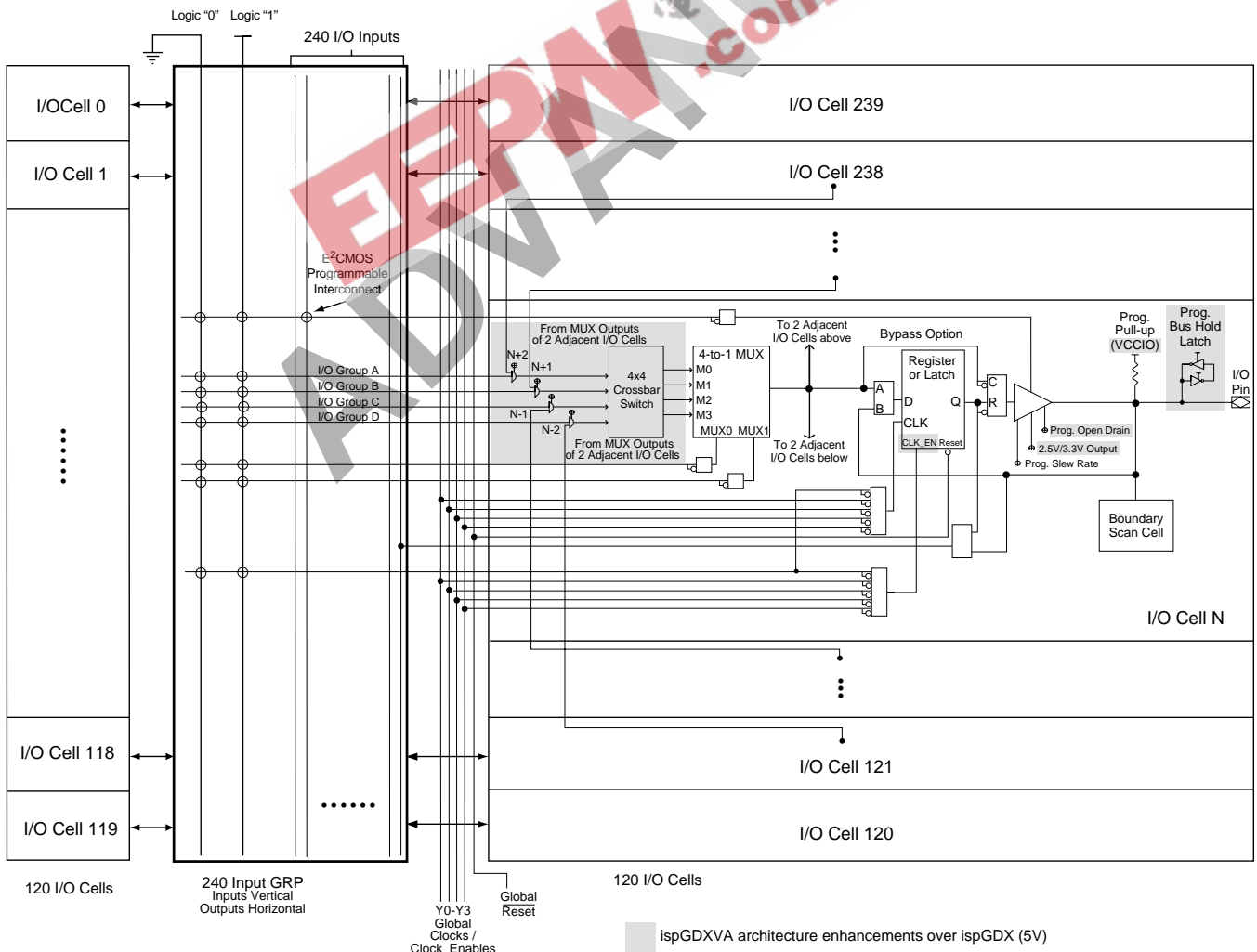
I/O MUX Operation

MUX1	MUX0	Data Input Selected
0	0	M0
0	1	M1
1	1	M2
1	0	M3

Flexible mapping of $MUXsel_x$ to MUX_x allows the user to change the MUX select assignment after the ispGDXVA device has been soldered to the board. Figure 1 shows that the I/O cell can accept (by programming the appropriate fuses) inputs from the MUX outputs of four adjacent I/O cells, two above and two below. This enables cascading of the MUXes to enable wider (up to 16:1) MUX implementations.

The I/O cell also includes a programmable flow-through latch or register that can be placed in the input or output path and bypassed for combinatorial outputs. As shown in Figure 1, when the input control MUX of the register/latch selects the "A" path, the register/latch gets its inputs from the 4:1 MUX and drives the I/O output. When selecting the "B" path, the register/latch is directly driven by the I/O input while its output feeds the GRP. The programmable polarity Clock to the latch or register can be connected to any I/O in the I/O-CLK/CLKEN set (one-quarter of total I/Os) or to one of the dedicated clock input pins (Y_x). The programmable polarity Clock Enable input to the register can be programmed to connect to any of the I/O-CLK/CLKEN input pin set or to the global clock enable inputs ($CLKEN_x$). Use of the dedicated clock inputs gives minimum clock-to-output delays and minimizes delay variation with fanout. Combinatorial output mode may be implemented by a dedicated architecture bit and bypass MUX. I/O cell output polarity can be programmed as active high or active low.

MUX Expander Using Adjacent I/O Cells

The ispGDXVA allows adjacent I/O cell MUXes to be cascaded to form wider input MUXes (up to 16 x 1) without incurring an additional full Tpd penalty. However, there are certain dependencies on the locality of the adjacent MUXes when used along with direct MUX inputs.
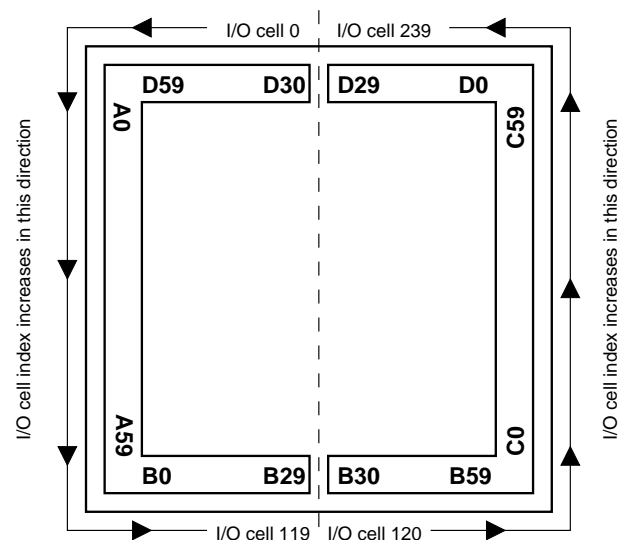
Adjacent I/O Cells

Expansion inputs MUXOUT[n-2], MUXOUT[n-1], MUXOUT[n+1], and MUXOUT[n+2] are fuse-selectable for each I/O cell MUX. These expansion inputs share the same path as the standard A, B, C and D MUX inputs, and

allow adjacent I/O cell outputs to be directly connected without passing through the global routing pool. The relationship between the [N+i] adjacent cells and A, B, C and D inputs will vary depending on where the I/O cell is located on the physical die. The I/O cells can be grouped into "normal" and "reflected" I/O cells or I/O "hemispheres." These are defined as:

Device	Normal I/O Cells	Reflected I/O Cells
ispGDX80VA	B9-B0, A19-A0, D19-D10	B10-B19, C0-C19, D0-D9
ispGDX160V/VA	B19-B0, A39-A0, D39-D20	B20-B39, C0-C39, D0-D19
ispGDX240VA	B29-B0, A59-A0, D59-D30	B30-B59, C0-C59, D0-D29

Table 2 shows the relationship between adjacent I/O cells as well as their relationship to direct MUX inputs. Note that the MUX expansion is circular and that I/O cell B30, for example, draws on I/Os B29 and B28, as well as B31 and B32, even though they are in different hemispheres of the physical die. Table 2 shows some typical cases and all boundary cases. All other cells can be extrapolated from the pattern shown in the table.
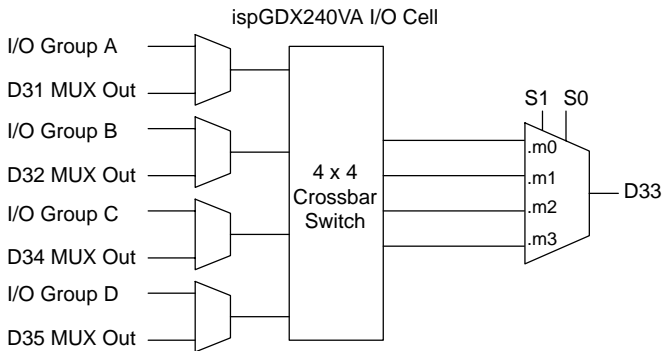
Figure 2. I/O Hemisphere Configuration of ispGDX240VA

Direct and Expander Input Routing

Table 2 also illustrates the routing of MUX direct inputs that are accessible when using adjacent I/O cells as inputs. Take I/O cell D33 as an example, which is also shown in Figure 3.

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Figure 3. Adjacent I/O Cells vs. Direct Input Path for ispGDX240VA, I/O D33

It can be seen from Figure 3 that if the D11 adjacent I/O cell is used, the I/O group "A" input is no longer available as a direct MUX input.

The ispGDXVA can implement MUXes up to 16 bits wide in a single level of logic, but care must be taken when combining adjacent I/O cell outputs with direct MUX inputs. Any particular combination of adjacent I/O cells as MUX inputs will dictate what I/O groups (A, B, C or D) can be routed to the remaining inputs. By properly choosing the adjacent I/O cells, all of the MUX inputs can be utilized.

Table 2. Adjacent I/O Cells (Mapping of ispGDX240VA)

		Data A/ MUXOUT	Data B/ MUXOUT	Data C/ MUXOUT	Data D/ MUXOUT
Reflected I/O Cells		B30	B32	B31	B29	B28
		B31	B33	B32	B30	B29
		B32	B34	B33	B31	B30
		B33	B35	B34	B32	B31
		D26	D28	D27	D25	D24
		D27	D29	D28	D26	D25
		D28	D30	D29	D27	D26
		D29	D31	D30	D28	D27
Normal I/O Cells		D30	D28	D29	D31	D32
		D31	D29	D30	D32	D33
		D32	D30	D31	D33	D34
		D33	D31	D32	D34	D35
		B26	B24	B25	B27	B28
		B27	B25	B26	B28	B29
		B28	B26	B27	B29	B30
		B29	B27	B28	B30	B31

Special Features

Slew Rate Control

All output buffers contain a programmable slew rate control that provides software-selectable slew rate options.

Open Drain Control

All output buffers provide a programmable Open-Drain option which allows the user to drive system level reset, interrupt and enable/disable lines directly without the need for an off-chip Open-Drain or Open-Collector buffer. Wire-OR logic functions can be performed at the printed circuit board level.

Pull-up Resistor

All pins have a programmable active pull-up. A typical resistor value for the pull-up ranges from 50kΩ to 80kΩ.

Output Latch (Bus Hold)

All pins have a programmable circuit that weakly holds the previously driven state when all drivers connected to the pin (including the pin's output driver as well as any other devices connected to the pin by external bus) are tristated.

User-Programmable I/Os

The ispGDX240VA features user-programmable I/Os supporting either 3.3V or 2.5V output voltage level options. The ispGDX240VA uses a VCCIO pin to provide the 2.5V reference voltage when used.

PCI Compatible Drive Capability

The ispGDX240VA supports PCI compatible drive capability for all I/Os.

Applications

The ispGDXVA Family architecture has been developed to deliver an in-system programmable signal routing solution with high speed and high flexibility. The devices are targeted for three similar but distinct classes of end-system applications:

Programmable, Random Signal Interconnect (PRSI)

This class includes PCB-level programmable signal routing and may be used to provide arbitrary signal swapping between chips. It opens up the possibilities of programmable system hardware. It is characterized by the need to provide a large number of 1:1 pin connections which are statically configured, i.e., the pin-to-pin paths do not need to change dynamically in response to control inputs.

Programmable Data Path (PDP)

This application area includes system data path transceiver, MUX and latch functions. With today's 32- and 64-bit microprocessor buses, but standard data path glue components still relegated primarily to eight bits, PCBs are frequently crammed with a dozen or more data path glue chips that use valuable real estate. Many of these applications consist of "on-board" bus and memory interfaces that do not require the very high drive of standard glue functions but can benefit from higher integration. Therefore, there is a need for a flexible means to integrate these on-board data path functions in an analogous way to programmable logic's solution to control logic integration. Lattice's CPLDs make an ideal control logic complement to the ispGDXVA in-system programmable data path devices as shown below.

Figure 4. ispGDXVA Complements Lattice CPLDs
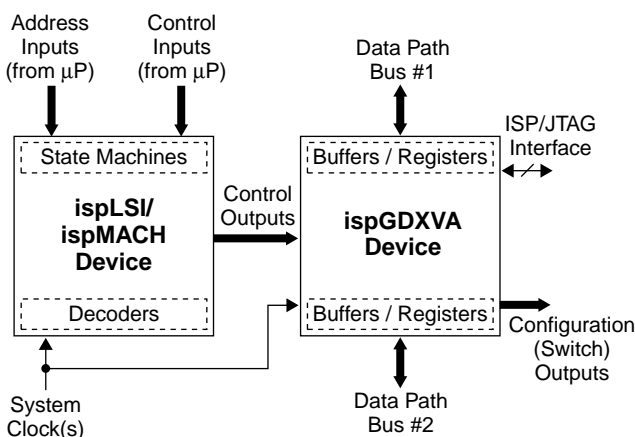
Programmable Switch Replacement (PSR)

Includes solid-state replacement and integration of mechanical DIP Switch and jumper functions. Through in-system programming, pins of the ispGDXVA devices can be driven to HIGH or LOW logic levels to emulate the traditional device outputs. PSR functions do not require any input pin connections.

These applications actually require somewhat different silicon features. PRSI functions require that the device support arbitrary signal routing on-chip between any two pins with no routing restrictions. The routing connections are static (determined at programming time) and each input-to-output path operates independently. As a result, there is little need for dynamic signal controls (OE, clocks, etc.). Because the ispGDXVA device will interface with control logic outputs from other components (such as ispLSI or ispMACH) on the board (which frequently change late in the design process as control logic is finalized), there must be no restrictions on pin-to-pin signal routing for this type of application.

PDP functions, on the other hand, require the ability to dynamically switch signal routing (MUXing) as well as latch and tri-state output signals. As a result, the programmable interconnect is used to define *possible* signal routes that are then selected dynamically by control signals from an external MPU or control logic. These functions are usually formulated early in the conceptual design of a product. The data path requirements are driven by the microprocessor, bus and memory architecture defined for the system. This part of the design is the earliest portion of the system design frozen, and will not usually change late in the design because the result would be total system and PCB redesign. As a result, the ability to accommodate *arbitrary* any pin-to-any pin re-routing is not a strong requirement as long as the designer has the ability to define his functions with a reasonable degree of freedom initially.

As a result, the ispGDXVA architecture has been defined to support PSR and PRSI applications (including bidirectional paths) with no restrictions, while PDP applications (using dynamic MUXing) are supported with a minimal number of restrictions as described below. In this way, speed and cost can be optimized and the devices can still support the system designer's needs.

The following diagrams illustrate several ispGDXVA applications.

Applications (Continued)
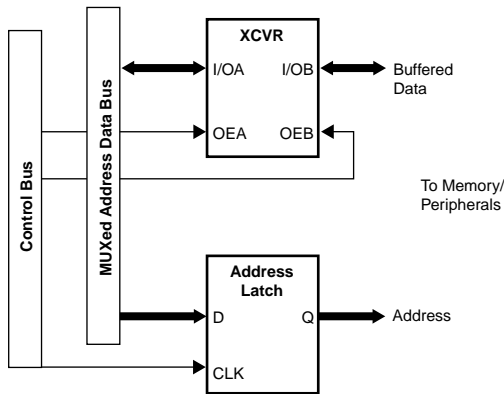
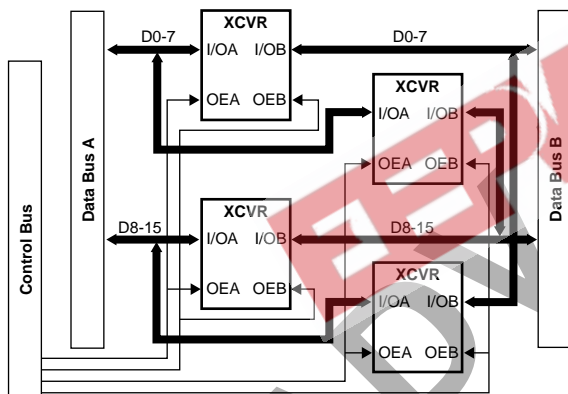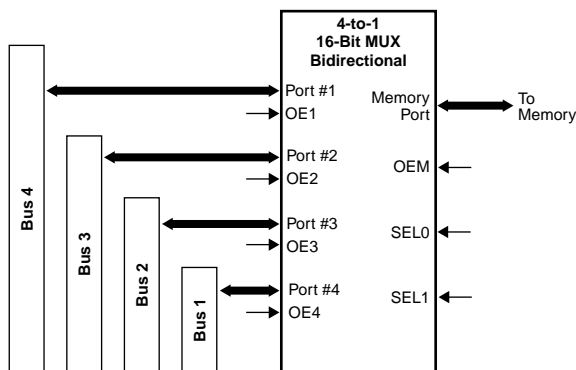**Figure 5. Address Demultiplex/Data Buffering**

Designing with the ispGDXVA

As mentioned earlier, this architecture satisfies the PRSI class of applications without restrictions: any I/O pin as a single input or bidirectional can drive any other I/O pin as output.

For the case of PDP applications, the designer does have to take into consideration the limitations on pins that can be used as control (MUX0, MUX1, OE, CLK) or data (MUXA-D) inputs. The restrictions on control inputs are not likely to cause any major design issues because the input possibilities span 25% of the total pins.

The MUXA-D input partitioning requires that designers consciously assign pinouts so that MUX inputs are in the appropriate, disjoint groups. For example, since the MUXA group includes I/O A0-39 (240 I/O device), it is not possible to use I/O A0 and I/O A9 in the same MUX function. As previously discussed, data path functions will be assigned early in the design process and these restrictions are reasonable in order to optimize speed and cost.

Figure 6. Data Bus Byte Swapper

User Electronic Signature

The ispGDXVA Family includes dedicated User Electronic Signature (UES) E^{2}CMOS storage to allow users to code design-specific information into the devices to identify particular manufacturing dates, code revisions, or the like. The UES information is accessible through the boundary scan programming port via a specific command. This information can be read even when the security cell is programmed.

Security

The ispGDXVA Family includes a security feature that prevents reading the device program once set. Even when set, it does not inhibit reading the UES or device ID code. It can be erased only via a device bulk erase.

Figure 7. Four-Port Memory Interface

Note: All OE and SEL lines driven by external arbiter logic (not shown).

Absolute Maximum Ratings [1,2]

Supply Voltage V_{CC} .... -0.5 to +5.4V

Input Voltage Applied .... -0.5 to +5.6V

Off-State Output Voltage Applied .... -0.5 to +5.6V

Storage Temperature .... -65 to 150°C

Case Temp. with Power Applied .... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).
2. Compliance with the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM is a requirement.

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	$T_A = 0°C$ to +70°C	3.00	3.60	V
		Industrial	$T_A = -40°C$ to +85°C	3.00	3.60	V
V_{CCIO}	I/O Reference Voltage			2.3	3.60	V

Table 2-0005/gdxva

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	PACKAGE TYPE	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	TQFP	7	pf	V_{CC} = 3.3V, $V_{I/O}$ = 2.0V
C_2	Dedicated Clock Capacitance	TQFP	8	pf	V_{CC} = 3.3V, V_Y = 2.0V

Table 2-0006/gdxva

Erase/Reprogram Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10,000	—	Cycles

Switching Test Conditions

| Input Pulse Levels	GND to $V_{CCIO(MIN)}$
Input Rise and Fall Time	≤ 1.5ns 10% to 90%
Input Timing Reference Levels	$V_{CCIO(MIN)}/2$
Output Timing Reference Levels	$V_{CCIO(MIN)}/2$
Output Load	See Figure 8

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (See Figure 8)

TEST CONDITION		3.3V R1	R2	2.5V R1	R2	CL
A		153Ω	134Ω	156Ω	144Ω	35pF
B	Active High	∞	134Ω	∞	144Ω	35pF
	Active Low	153Ω	∞	156Ω	∞	35pF
C	Active High to Z at V_{OH}-0.5V	∞	134Ω	∞	144Ω	5pF
	Active Low to Z at V_{OL}+0.5V	153Ω	∞	156Ω	∞	5pF
D	Slow Slew	∞	∞	∞	∞	35pF

Table 2-0004A/gdxva

Figure 8. Test Load
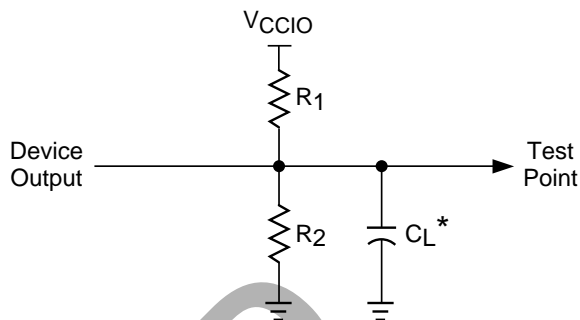
*C_L includes Test Fixture and Probe Capacitance.

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DC Electrical Characteristics for 3.3V Range

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[1]	MAX.	UNITS
V_{CCIO}	I/O Reference Voltage	–		3.0	–	3.6	V
V_{IL}	Input Low Voltage	$V_{OH} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL\,(MAX)}$		-0.3	–	0.8	V
V_{IH}	Input High Voltage	$V_{OH} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(MAX)}$		2.0	–	5.25	V
V_{OL}	Output Low Voltage	$V_{CC} = V_{CC\,(MIN)}$	$I_{OL} = +100\mu A$	–	–	0.2	V
			$I_{OL} = +24mA$	–	–	0.55	V
V_{OH}	Output High Voltage	$V_{CC} = V_{CC\,(MIN)}$	$I_{OH} = -100\mu A$	2.8	–	–	V
			$I_{OH} = -12mA$	2.4	–	–	V

1. Typical values are at $V_{CC} = 3.3V$ and $T_A = 25°C$.

Table 2-0007/gdxva

DC Electrical Characteristics for 2.5V Range

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCIO}	I/O Reference Voltage	–	2.3	–	2.7	V
V_{IL}	Input Low Voltage	$V_{OH(MIN)} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(MAX)}$	-0.3	–	0.7	V
V_{IH}	Input High Voltage	$V_{OH(MIN)} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(MAX)}$	1.7	–	5.25	V
V_{OL}	Output Low Voltage	$V_{CCIO=MIN}$, $I_{OL} = 100\mu A$	–	–	0.2	V
		$V_{CCIO=MIN}$, $I_{OL} = 8mA$	–	–	0.6	V
V_{OH}	Output High Voltage	$V_{CCIO=MIN}$, $I_{OH} = -100\mu A$	2.1	–	–	V
		$V_{CCIO=MIN}$, $I_{OH} = -8mA$	1.8	–	–	V

2.5V/gdxva

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL\ (MAX)}$	–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	$(V_{CCIO}\text{-}0.2) \leq V_{IN} \leq V_{CCIO}$	–	–	10	μA
		$V_{CCIO} \leq V_{IN} \leq 5.25V$	–	–	50	μA
I_{PU}	I/O Active Pullup Current	$0V \leq V_{IN} \leq V_{IL\ (MAX)}$	–	–	-200	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL\ (MAX)}$	40	–	–	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = V_{IH\ (MIN)}$	-40	–	–	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \leq V_{IN} \leq V_{CCIO}$	–	–	550	μA
I_{BHHO}	Bus Hold High Overdrive Current	$0V \leq V_{IN} \leq V_{CCIO}$	–	–	-550	μA
I_{BHT}	Bus Hold Trip Points		V_{IL}	–	V_{IH}	V
I_{OS}[1]	Output Short Circuit Current	$V_{CC} = 3.3V$, $V_{OUT} = 0.5V$, $T_A = 25°C$	–	–	-250	mA
I_{CCQ}[4]	Quiescent Power Supply Current	$V_{IL} = 0.5V$, $V_{IH} = V_{CC}$	–	16.5	–	mA
I_{CC}	Dynamic Power Supply Current per Input Switching	One input toggling at 50% duty cycle, outputs open.	–	See Note 3	–	mA/MHz
I_{CONT}[5]	Maximum Continuous I/O Pin Sink Current Through Any GND Pin	–	–	–	160	mA

DC Char_gdxva

1. One output at a time for a maximum of one second. $V_{OUT} = 0.5V$ was selected to avoid test problems by tester ground degradation. Characterized, but not 100% tested.
2. Typical values are at $V_{CC} = 3.3V$ and $T_A = 25°C$.
3. I_{CC} / MHz = (0.0025 x I/O cell fanout) + 0.042.
   e.g. An input driving four I/O cells at 40MHz results in a dynamic I_{CC} of approximately ((0.0025 x 4) + 0.042) x 40 = 2.08mA.
4. For a typical application with 50% of I/O pins used as inputs, 50% used as outputs or bi-directionals.
5. This parameter limits the total current sinking of I/O pins surrounding the nearest GND pin.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[1] COND.	#	DESCRIPTION	-4 MIN.	-4 MAX.	-7 MIN.	-7 MAX.	UNITS
t_{pd}[2]	A	1	Data Prop. Delay from Any I/O pin to Any I/O Pin (4:1 MUX)	–	4.5	–	7.0	ns
t_{sel}[2]	A	2	Data Prop. Delay from MUXsel Inputs to Any Output (4:1 MUX)	–	4.5	–	7.0	ns
f_{max} (Tog.)	–	3	Clock Frequency, Max. Toggle	200	–	100	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su3}+t_{gco1}}\right)$	111	–	80	–	MHz
t_{su1}	–	5	Input Latch or Register Setup Time Before Y_x	4.0	–	5.5	–	ns
t_{su2}	–	6	Input Latch or Register Setup Time Before I/O Clock	3.0	–	4.5	–	ns
t_{su3}	–	7	Output Latch or Register Setup Time Before Y_x	4.0	–	5.5	–	ns
t_{su4}	–	8	Output Latch or Register Setup Time Before I/O Clock	3.0	–	4.5	–	ns
t_{suce1}	–	9	Global Clock Enable Setup Time Before Y_x	2.5	–	3.5	–	ns
t_{suce2}	–	10	Global Clock Enable Setup Time Before I/O Clock	1.5	–	2.5	–	ns
t_{suce3}	–	11	I/O Clock Enable Setup Time Before Y_x	4.5	–	6.5	–	ns
t_{h1}	–	12	Input Latch or Reg. Hold Time (Y_x)	0.0	–	0.0	–	ns
t_{h2}	–	13	Input Latch or Reg. Hold Time (I/O Clock)	1.5	–	2.5	–	ns
t_{h3}	–	14	Output Latch or Reg. Hold Time (Y_x)	0.0	–	0.0	–	ns
t_{h4}	–	15	Output Latch or Reg. Hold Time (I/O Clock)	1.5	–	2.5	–	ns
t_{hce1}	–	16	Global Clock Enable Hold Time (Y_x)	0.0	–	0.0	–	ns
t_{hce2}	–	17	Global Clock Enable Hold Time (I/O Clock)	1.5	–	2.5	–	ns
t_{hce3}	–	18	I/O Clock Enable Hold Time (Y_x)	0.0	–	0.0	–	ns
t_{gco1}[2]	A	19	Output Latch or Reg. Clock (from Y_x) to Output Delay	–	4.5	–	7.0	ns
t_{gco2}[2]	A	20	Input Latch or Register Clock (from Y_x) to Output Delay	–	8.5	–	11.0	ns
t_{co1}[2]	A	21	Output Latch or Register Clock (from I/O pin) to Output Delay	–	6.0	–	9.0	ns
t_{co2}[2]	A	22	Input Latch or Register Clock (from I/O pin) to Output Delay	–	9.5	–	13.0	ns
t_{en}[2]	B	23	Input to Output Enable	–	6.0	–	8.5	ns
t_{dis}[2]	C	24	Input to Output Disable	–	6.0	–	8.5	ns
t_{toeen}[2]	B	25	Test OE Output Enable	–	7.0	–	8.5	ns
t_{toedis}[2]	C	26	Test OE Output Disable	–	7.0	–	8.5	ns
t_{wh}	–	27	Clock Pulse Duration, High	3.5	–	5.0	–	ns
t_{wl}	–	28	Clock Pulse Duration, Low	3.5	–	5.0	–	ns
t_{rst}	–	29	Register Reset Delay from RESET Low	–	14.0	–	18.0	ns
t_{rw}	–	30	Reset Pulse Width	10.0	–	14.0	–	ns
t_{sl}	D	31	Output Delay Adder for Output Timings Using Slow Slew Rate	–	4.5	–	7.0	ns
t_{sk}	A	32	Output Skew (t_{gco1} Across Chip)	–	0.5	–	0.5	ns

1. All timings measured with one output switching, fast output slew rate setting, except t_{sl}.
2. The delay parameters are measured with Vcc as I/O voltage reference. An additional 0.5ns delay is incurred when Vccio is used as I/O voltage reference.

External Timing Parameters (Continued)

ispGDX240VA timings are specified with a GRP load (fanout) of four I/O cells. The figure below shows the Δ GRP Delay with increased GRP loads. These deltas apply to any signal path traversing the GRP (MUXA-D, OE, CLK/CLKEN, MUXsel0-1). Global Clock signals which do not use the GRP have no fanout delay adder.

**ispGDX240VA Maximum Δ GRP Delay vs. I/O Cell Fanout**
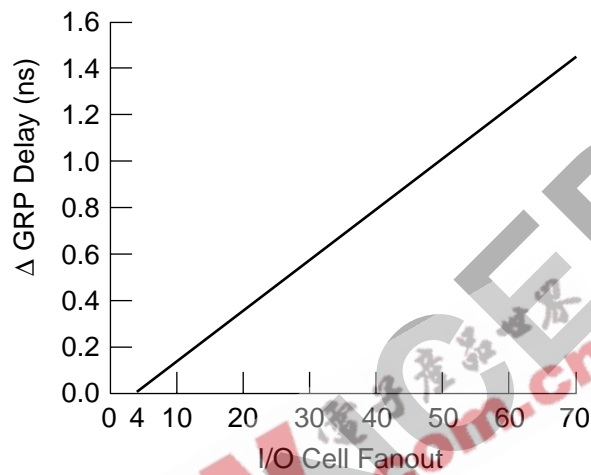
Internal Timing Parameters[1]
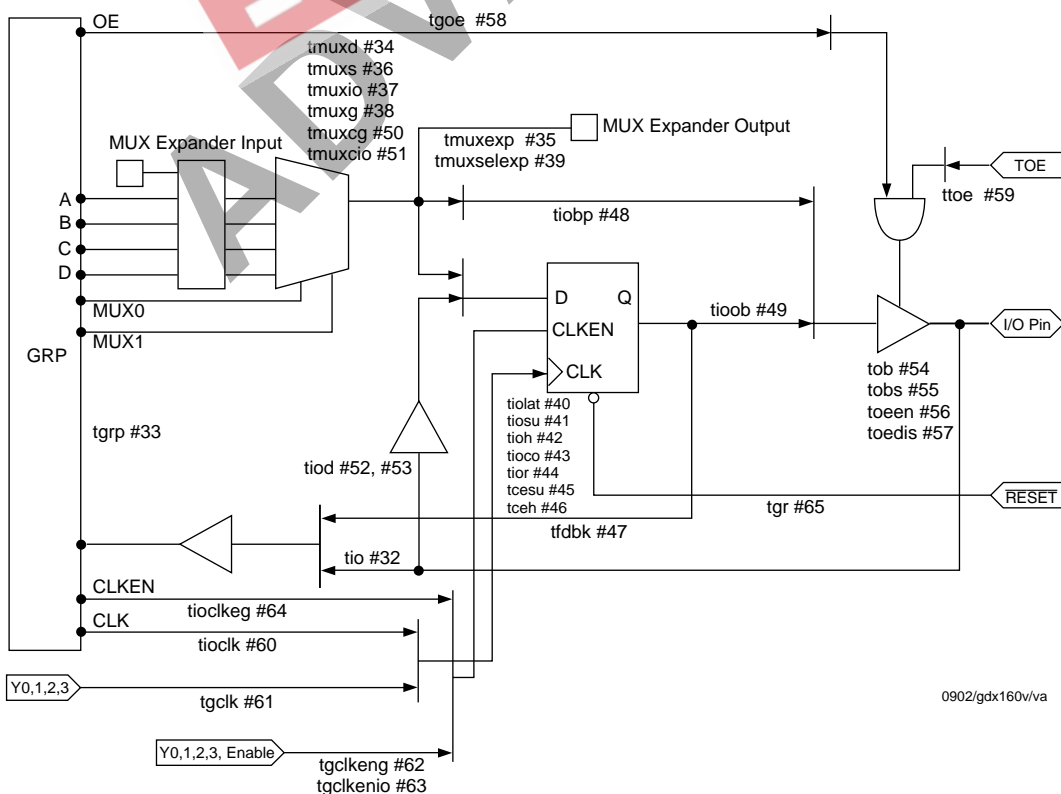
Over Recommended Operating Conditions

PARAMETER	#	DESCRIPTION[1]	-4		-7		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	32	Input Buffer Delay	—	0.4	—	0.9	ns
GRP							
t_{grp}	33	GRP Delay	—	1.1	—	1.1	ns
MUX							
t_{muxd}	34	I/O Cell MUX A/B/C/D Data Delay	—	1.0	—	1.5	ns
t_{muxexp}	35	I/O Cell MUX A/B/C/D Expander Delay	—	1.5	—	2.0	ns
t_{muxs}	36	I/O Cell Data Select	—	1.0	—	1.5	ns
t_{muxsio}	37	I/O Cell Data Select (I/O Clock)	—	1.5	—	3.0	ns
t_{muxsg}	38	I/O Cell Data Select (Yx Clock)	—	1.5	—	2.0	ns
$t_{muxselexp}$	39	I/O Cell MUX Data Select Expander Delay	—	1.5	—	2.0	ns
Register							
t_{iolat}	40	I/O Latch Delay	—	1.0	—	1.0	ns
t_{iosu}	41	I/O Register Setup Time Before Clock	—	0.8	—	2.0	ns
t_{ioh}	42	I/O Register Hold Time After Clock	—	1.7	—	1.5	ns
t_{ioco}	43	I/O Register Clock to Output Delay	—	1.2	—	0.5	ns
t_{ior}	44	I/O Reset to Output Delay	—	1.0	—	1.5	ns
t_{cesu}	45	I/O Clock Enable Setup Time Before Clock	—	2.3	—	2.0	ns
t_{ceh}	46	I/O Clock Enable Hold Time After Clock	—	0.2	—	0.5	ns
Data Path							
t_{fdbk}	47	I/O Register Feedback Delay	—	0.6	—	0.9	ns
t_{iobp}	48	I/O Register Bypass Delay	—	0.0	—	0.0	ns
t_{ioob}	49	I/O Register Output Buffer Delay	—	0.0	—	0.0	ns
t_{muxcg}	50	I/O Register A/B/C/D Data Input MUX Delay (Yx Clock)	—	1.5	—	2.0	ns
t_{muxcio}	51	I/O Register A/B/C/D Data Input MUX Delay (I/O Clock)	—	1.5	—	3.0	ns
t_{iodg}	52	I/O Register I/O MUX Delay (Yx Clock)	—	3.5	—	4.0	ns
t_{iodio}	53	I/O Register I/O MUX Delay (I/O Clock)	—	3.5	—	5.0	ns
Outputs							
t_{ob}	54	Output Buffer Delay	—	1.0	—	1.5	ns
t_{obs}	55	Output Buffer Delay (Slow Slew Option)	—	4.5	—	6.5	ns
t_{oeen}	56	I/O Cell OE to Output Enable	—	3.5	—	4.0	ns
t_{oedis}	57	I/O Cell OE to Output Disable	—	3.5	—	4.0	ns
t_{goe}	58	GRP Output Enable and Disable Delay	—	0.0	—	0.0	ns
t_{toe}	59	Test OE Enable and Disable Delay	—	2.5	—	2.0	ns
Clocks							
t_{ioclk}	60	I/O Clock Delay	—	0.3	—	2.0	ns
t_{gclk}	61	Global Clock Delay	—	1.3	—	2.0	ns
$t_{gclkeng}$	62	Global Clock Enable (Yx Clock)	—	1.5	—	2.5	ns
$t_{gclkenio}$	63	Global Clock Enable (I/O Clock)	—	1.0	—	3.5	ns
$t_{ioclkeng}$	64	I/O Clock Enable (Yx Clock)	—	0.5	—	2.5	ns
Global Reset							
t_{gr}	65	Global Reset to I/O Register Latch	—	6.0	—	11.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to the Timing Model in this data sheet for further details.

Switching Waveforms

Combinatorial Output

Registered Output

I/O Output Enable/Disable

Clock Width

Reset
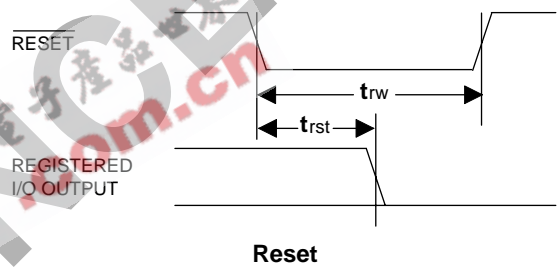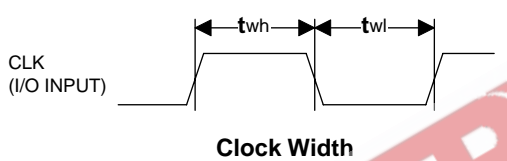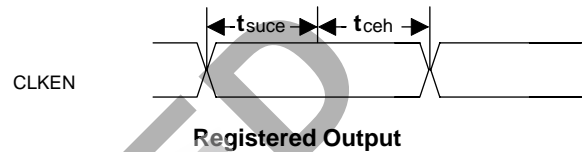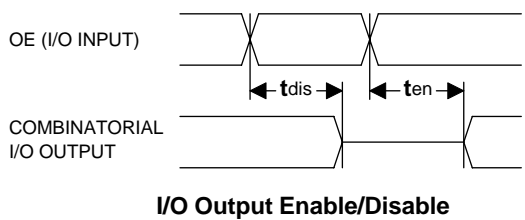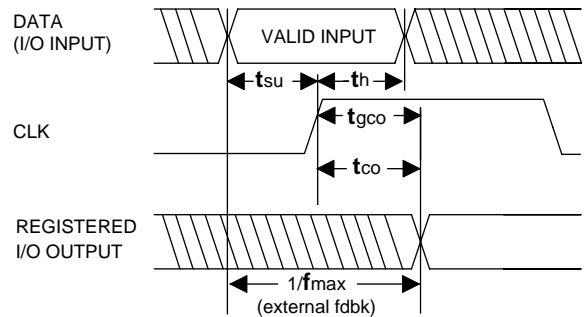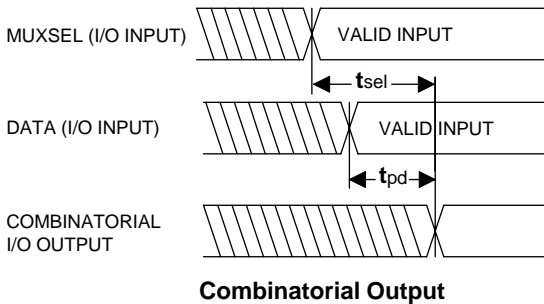
ispGDXVA Timing Model

0902/gdx160v/va

ispGDX Development System

The ispGDX Development System supports ispGDX design using a simple language syntax and an easy-to-use Graphical User Interface (GUI) called Design Manager. From creation to In-System Programming, the ispGDX system is an easy-to-use, self-contained design tool delivered on CD-ROM media.
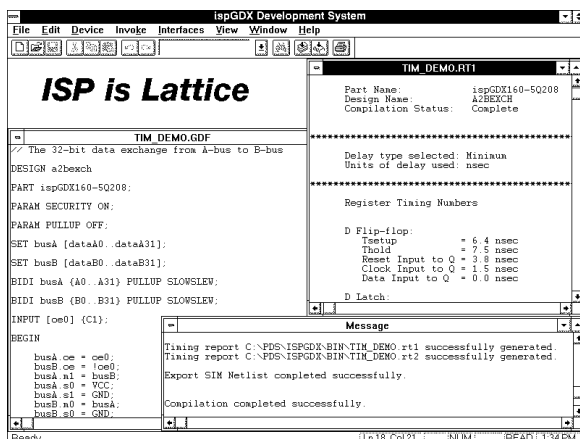
Features

- Easy-to-use Text Entry System
- ispGDX Design Compiler
    - Design Rule Checker
    - I/O Connectivity Checker
    - Automatic Compiler Function
- Industry Standard JEDEC File for Programming
- Min / Max Timing Report
- Interfaces To Popular Timing Simulators
- User Electronic Signature (UES) Support
- Detailed Log and Report Files For Easy Design Debug
- On-Line Help
- Windows® 3.1x, Windows 95, Windows 98 and Windows NT® Compatible Graphical User Interface
- SUN O/S, Command Line Driven version available

PC Version

With the ispGDX GUI for the PC, command line entry is not required. The tools run under Microsoft Windows 3.1, Windows 95, Windows 98 and Windows NT. When the ispGDX software is invoked, the Design Manager and an accompanying message window are displayed. The Design Manager consists of the Menu Bar, Tool Bar,

Status Bar and the work area. The figure below shows these elements of the ispGDX GUI.

The Menu Bar displays topics related to functions used in the design process. Access the various drop-down menus and submenus by using the mouse or "hot" keys. The menu items available in the ispGDX system are FILE, EDIT, DEVICE, INVOKE, INTERFACES, VIEW, WINDOW and HELP.

The Tool Bar is a quick and easy way to perform many of the functions found in the menus with a single click of the mouse. File, Edit, Undo, Redo, Find, Print Download and Compiler are just some of the Icons found in the ispGDX Tool Bar. For instance, the Compiler Icon performs the same function as the Invoke => Compiler menu commands, including design analysis and rule checking and the fitting operation.

The Status Bar displays action prompts and the line and column numbers reflect the location of the cursor within the message window or the work area.

Workstation Version

The ispGDX software is also available for use under the Sun O/S 4.1.x or Solaris 2.4 or 2.5. The Sun version of the ispGDX software is invoked from the command line under the UNIX operating system. A GUI is not supported in this environment.

In the UNIX environment, the ispGDX Design File (GDF) must be created using a text editor. Once the GDF has been created, invoke the ispGDX workstation software from the UNIX command line. The following is an example of how to invoke ispGDX software.

Lattice's ispGDX Development System Interface

Usage:

```
ispGDX
[-i input_file]
[-of[edif|orcad|viewlogic|verilog|vhdl]]
[-p part name]
[-r par_file]
```

Where:

-i input_file	ispGDX design file
-of [edif | orcad | viewlogic | verilog | vhdl]	Output format
-p part_name	ispGDX part number
-r par_file	Read parameters from parameter file

ispGDX Development System (Continued)

The GDF File

The GDF file is a simple text description of the design function, device and pin parameters. The file has four parts: device selection, set and constant statements, a pin section and a connection section. A sample file looks like this:

```
// 32-Bit Data 3 to 1 Mux

DESIGN      datamux;

PART ispGDX160V-7Q208;
PARAM SECURITY ON;
PARAM OPENDRAIN ON;      // USE OPEN DRAIN
                        // OPTION
PARAM PULL HOLD;        // USE BUS HOLD
                        // LATCH OPTION


SET BUS_A   [dataA31..dataA0];
SET BUS_B   [dataB31..dataB0];
SET BUS_C   [dataC31..dataC0];
SET BUS_D   [dataD31..dataD0];


INPUT  BUS_A     {A31..A0};
INPUT  BUS_B     {B31..B0};
INPUT  BUS_C     {C31..C0};
OUTPUT BUS_D     {D31..D0};


INPUT [oe] {B37};
INPUT [clk] {B36};

INPUT [sel1]     {B38};
INPUT [sel0]     {B39};

BEGIN

      BUS_D.m0 = BUS_A;
      BUS_D.m1 = BUS_B;
      BUS_D.m2 = BUS_C;
      BUS_D.m3 = VCC;     // Default all
                        // outputs to VCC

      BUS_D.s1 = sel1;
      BUS_D.s0 = sel0;

      BUS_D.oe = oe;
      BUS_D.clk = clk;

END
```

This example shows a simple, but complete, 32-bit 3:1 MUX design. Once completed, the compiler takes over.

Powerful Syntax

Lattice's ispGDX Design System uses simple, but powerful, syntax to easily define a design. The !(bang) operator controls pin polarity and can be used in both the pin and connection sections of the design definition. Dot extensions define data inputs, select controls for the 4:1 multiplexor, and control inputs of sequential elements and tri-state buffers. Dot extensions are .M# (MUX Input), .S# (MUX Select), and control functions, such as .CLK, .EN, .OE and .A (shown in adjacent table). Pin Attributes are assigned in the pin section of the GDF as well. SLOWSLEW selects the slow slew rate for an output buffer. The Pull parameter can be used to select the internal pull-up or bus hold latch. OPEN drain can be used to select open drain operation. The COMB attribute distinguishes the structure for bidirectional pins. If COMB is used, the input register, or latch, of an output buffer will be applied to bidirectional pins.

Please consult the ispGDX Development System Manual for full details.

ispGDX GDF File Dot Extensions

Type	Dot Ext.	Description
MUX Input	.M0	MUXA Data input to 4:1 MUX
	.M1	MUXB Data input to 4:1 MUX
	.M2	MUXC Data Input to 4:1 MUX
	.M3	MUXD Data input to 4:1 MUX
MUX Selection	.S0	MUX0 Selection input to 4:1 MUX
	.S1	MUX1 Selection input to 4:1 MUX
Control	.CLK	Clock for a register
	.EN	Latch enable for a latch signal
	.OE	Output enable for 3-state output or bidirectional signal
	.CE	Clock enable for register clock
MUX Output	.A	Adjacent MUX output of an I/O cell

ispGDXV Dot Ext

ispGDX Development System (Continued)

The ispGDX Design System Compiler

After the GDF file is created, the compiler checks the syntax and provides helpful hints and the location of any syntax errors. The compiler performs design rule checks, such as, clock and enable designations, the use of input/output/BIDI usage, and the proper use of attributes. I/O connectivity is also checked to ensure polarity, MUX selection controls, and connections are properly made. Compilation is completed automatically and report and programming files are saved.

Reports Generated

When the ispGDX system compiles a design and generates the specified netlists, the following output files are created:

Report Files:
    .log   Compiler History
    .rpt   Compiler Report
    .mfr   Maximum Frequency Timing Report
    .tsu   Set-up and Hold Timing Report
    .tco   Clock to Out Timing Report
    .tpt   Timing Report

Simulation File:
    .sim   Post-Route Simulation With LAC Format

Netlists:
    .edo   EDIF Output
    .vlo   Verilog Output
    .ifo   OrCAD Output
    .vho   VHDL non-VITAL with Maximum Delays Output
    .vhn   VHDL non-VITAL with Maximum Delays Output
    .vto   VHDL VITAL Output

Download:
    .jed   JEDEC Device Programming File

Third-Party Timing Simulation

The ispGDX Design System will generate simulation netlists as specified by a user. The simulation netlist formats available are: EDIF, Verilog (OVI compliant), VHDL (VITAL compliant), Viewlogic, and OrCAD.

For In-System Programming, Lattice's ispGDX devices may be programmed, alone or in a chain with up to 100 other Lattice ISP devices, using Lattice's ISP Daisy Chain Download software. This powerful Windows-based tool can be launched from the Tool Bar or by Invoking the Download option from the drop down menu within the ispGDX Design System. ISP Daisy Chain Download version 7.1 or above supports the ispGDX Family devices.

In-System Programmability

All necessary programming of the ispGDXVA is done via four TTL level logic interface signals. These four signals are fed into the on-chip programming circuitry where a state machine controls the programming.

On-chip programming can be accomplished using an IEEE 1149.1 boundary scan protocol. The IEEE 1149.1-compliant interface signals are Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK) and Test Mode Select (TMS) control. The EPEN pin is also used to enable or disable the JTAG port.

The embedded controller port enable pin (EPEN) is used to enable the JTAG tap controller and in that regard has similar functionality to a TRST pin. When the pin is driven high, the JTAG TAP controller is enabled. This is also true

when the pin is left unconnected, in which case the pin is pulled high by the permanent internal pullup. This allows ISP programming and BSCAN testing to take place as specified by the Instruction Table.

When the pin is driven low, the JTAG TAP controller is driven to a reset state asynchronously. It stays there while the pin is held low. After pulling the pin high the JTAG controller becomes active. The intent of this feature is to allow the JTAG interface to be directly controlled by the data bus of an embedded controller (hence the name Embedded Port Enable). The EPEN signal is used as a "device select" to prevent spurious programming and/or testing from occuring due to random bit patterns on the data bus. Figure 9 illustrates the block diagram for the ispJTAG interface.

Figure 9. ispJTAG Device Programming Interface
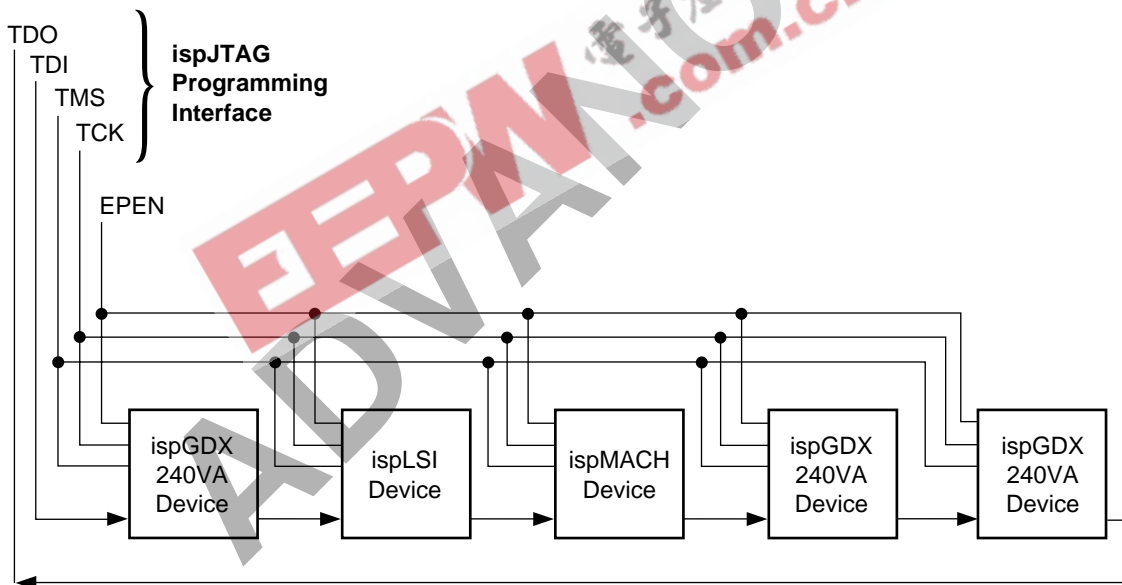
Boundary Scan

The ispGDXV/VA devices provide IEEE1149.1a test capability and ISP programming through a standard Boundary Scan Test Access Port (TAP) interface.

The boundary scan circuitry on the ispGDXVA Family operates independently of the programmed pattern. This allows customers using boundary scan test to have full test capability with only a single BSDL file.

The ispGDXVA devices are identified by the 32-bit JTAG IDCODE register. The device ID assignments are listed in Table 4.

Figure 10. Boundary Scan Register Circuit for I/O Pins
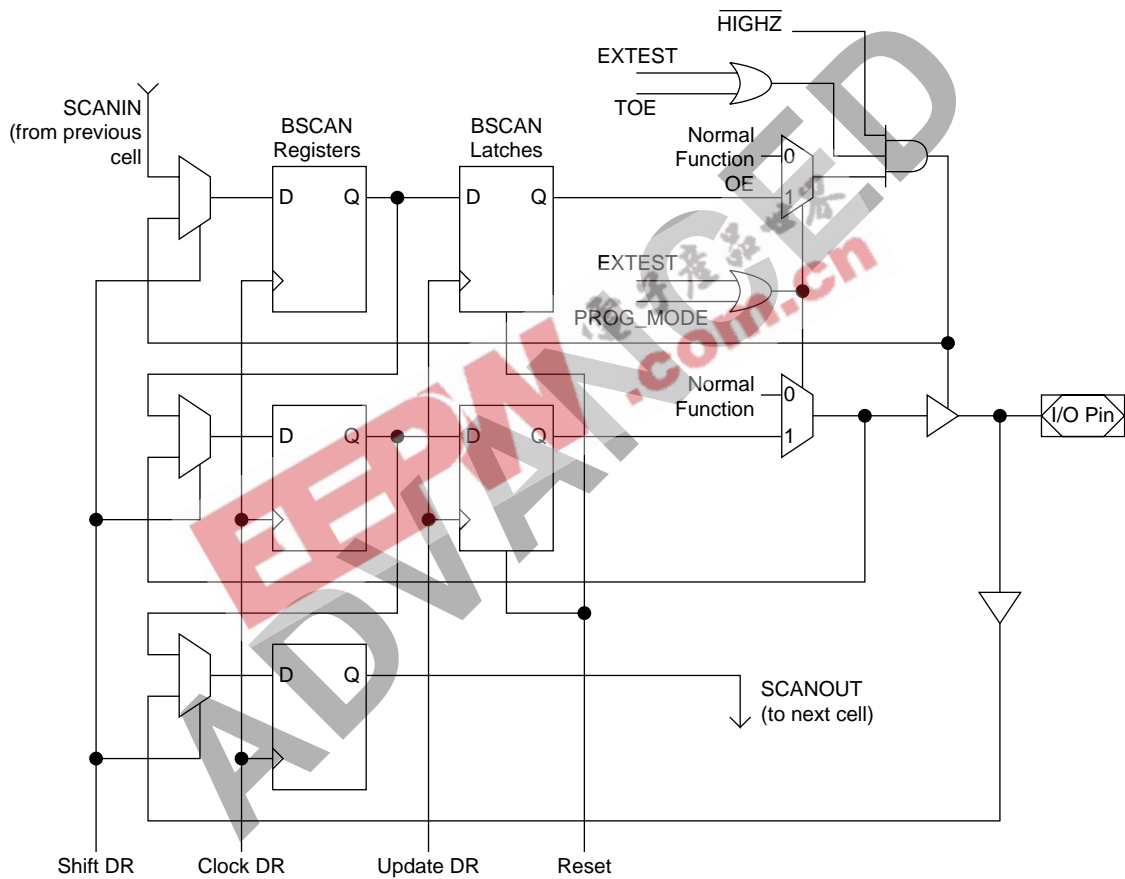
Table 3. I/O Shift Register Order

DEVICE	I/O SHIFT REGISTER ORDER
ispGDX240VA	TDI, TOE, Y2, Y3, $\overline{RESET}$, Y1, Y0, I/O B20 .. B39, I/O C0 .. C39, I/O D0 .. D19, I/O B19 .. B0, I/O A39.. A0, I/O D39 .. D20, TDO

I/O Shift Reg Order/ispGDXVA

Table 4. ispGDX240VA Device ID Codes

DEVICE	32-BIT BOUNDARY SCAN ID CODE
ispGDX240VA	0001, 0000, 0011, 0101, 0100, 0000, 0100, 0011

ID Code/GDX240VA

Boundary Scan (Continued)

The ispJTAG programming is accomplished by executing Lattice private instructions under the Boundary Scan State Machine.

Details of the programming sequence are transparent to the user and are handled by Lattice ISP Daisy Chain Downlowad (ispDCD™), ispCODE 'C' routines or any third-party programmers. Contact Lattice Technical Support to obtain more detailed programming information.

Figure 11. Boundary Scan Register Circuit for Input-Only Pins
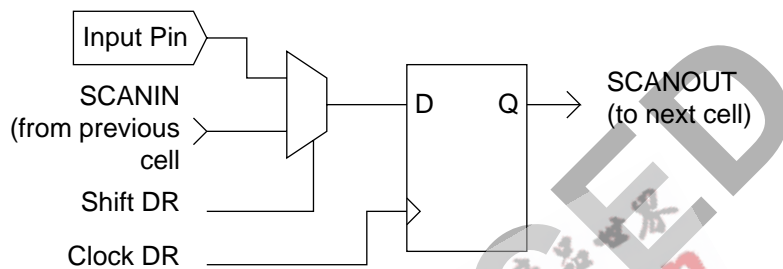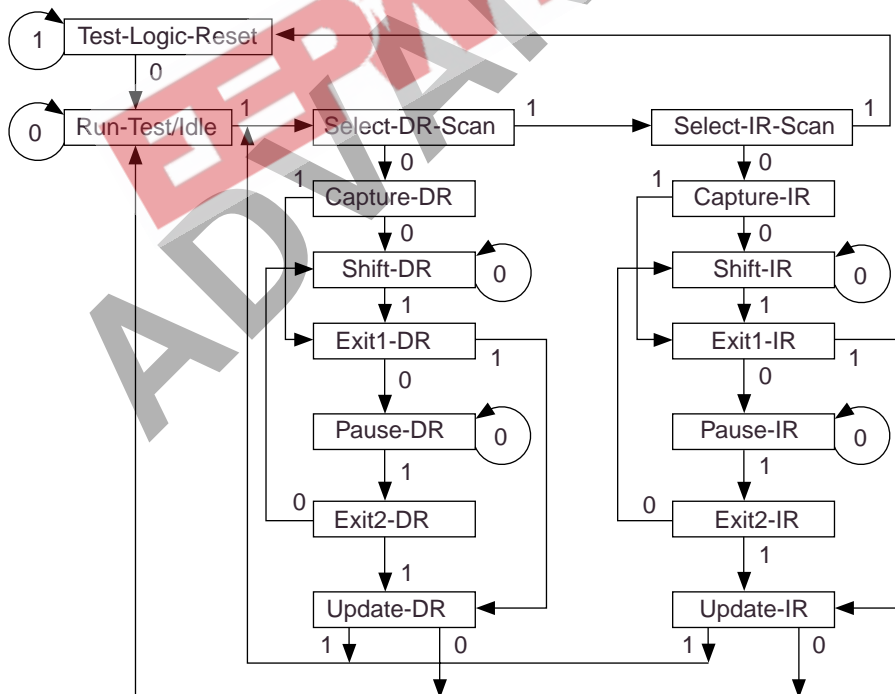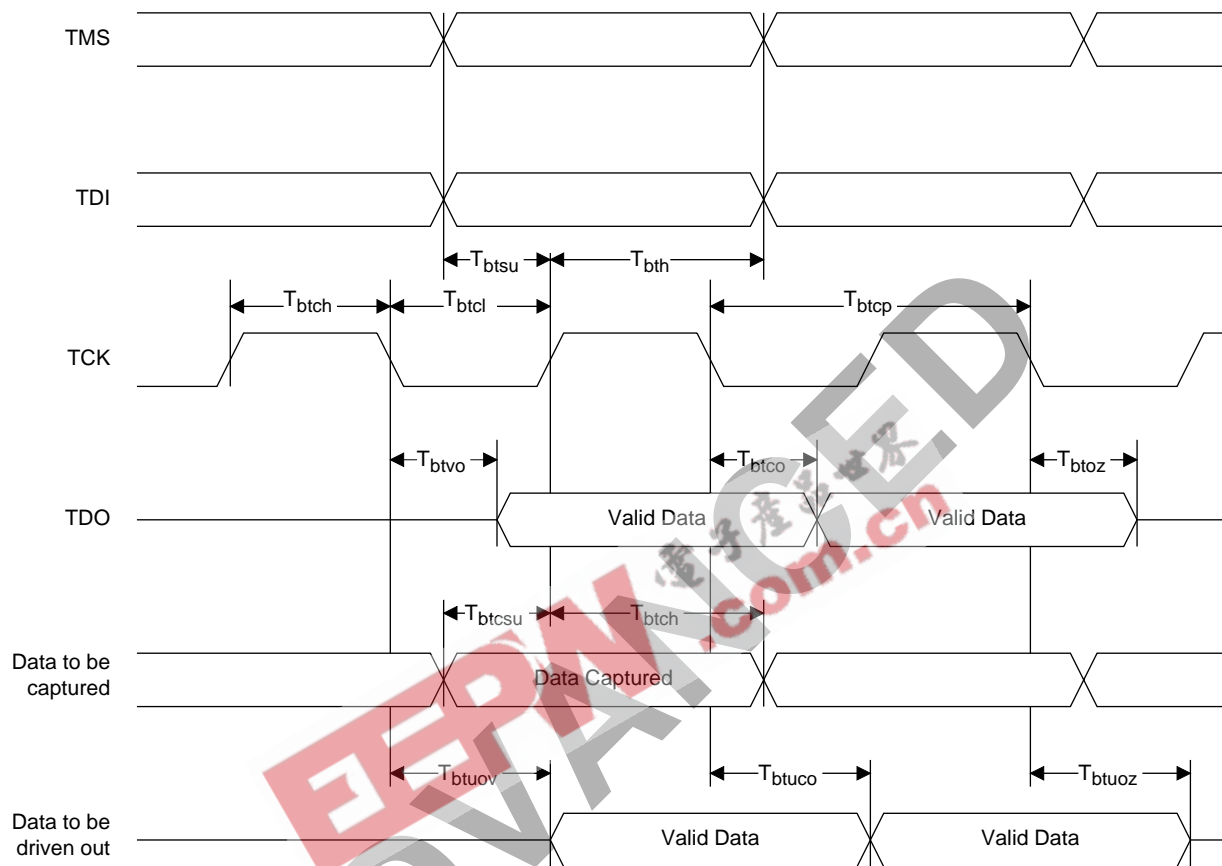

Figure 12. Boundary Scan State Machine

Boundary Scan (Continued)

Figure 13. Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min	Max	Units
t_{btcp}	TCK [BSCAN test] clock pulse width	100	–	ns
t_{btch}	TCK [BSCAN test] pulse width high	50	–	ns
t_{btcl}	TCK [BSCAN test] pulse width low	50	–	ns
t_{btsu}	TCK [BSCAN test] setup time	20	–	ns
t_{bth}	TCK [BSCAN test] hold time	25	–	ns
t_{rf}	TCK [BSCAN test] rise and fall time	50	–	mV/ns
t_{btco}	TAP controller falling edge of clock to valid output	–	25	ns
t_{btoz}	TAP controller falling edge of clock to data output disable	–	25	ns
t_{btvo}	TAP controller falling edge of clock to data output enable	–	25	ns
t_{btcpsu}	BSCAN test Capture register setup time	20	–	ns
t_{btcph}	BSCAN test Capture register hold time	25	–	ns
t_{btuco}	BSCAN test Update reg, falling edge of clock to valid output	–	50	ns
t_{btuoz}	BSCAN test Update reg, falling edge of clock to output disable	–	50	ns
t_{btuov}	BSCAN test Update reg, falling edge of clock to output enable	–	50	ns

Signal Locations: ispGDX240VA

Signal	388-Ball fpBGA
TOE	L22
RESET	L21
Y0/CLKEN0	M4
Y1/CLKEN1	L3
Y2/CLKEN2	M20
Y3/CLKEN3	M21
EPEN	A11
TDI	M1
TCK	L1
TMS	L2
TDO	AB12
GND	A1, A22, B2, B21, C3, C20, D4, D19, H9, H10, H11, H12, H13, H14, J8, J9, J10, J11, J12, J13, J14, J15, K8, K9, K10, K11, K12, K13, K14, K15, L8, L9, L10, L11, L12, L13, L14, L15, M8, M9, M10, M11, M12, M13, M14, M15, N8, N9, N10, N11, N12, N13, N14, N15, P8, P9, P10, P11, P12, P13, P14, P15, R9, R10, R11, R12, R13, R14, W4, W19, Y3, Y20, AA2, AA21, AB1, AB22
VCC	D6, D9, D12, D14, D17, F4, F19, G7, G8, G15, G16, H7, H16, J4, J19, L4, M19, P4, P19, R7, R16, T7, T8, T15, T16, U4, U19, W6, W9, W11, W14, W17
VCCIO	M22
NC	G9, G10, G11, G12, G13, G14, G15, H8, H15, J7, J16, K7, K16, L7, L16, M7. M16, N7, N16, P7, P16, R8, R15, T9, T10, T11, T12, T13, T14

I/O Locations: ispGDX240VA (Ordered by 388-Ball BGA Location)

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Signal Configuration: ispGDX240VA

ispGDX240VA 388-Ball fpBGA Signal Diagram

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	
1	GND	I/O A1	I/O A4	I/O A6	I/O A10	I/O A13	I/O A17	I/O A21	I/O A24	I/O A28	TCK	TDI	I/O A31	I/O A35	I/O A38	I/O A42	I/O A46	I/O A49	I/O A53	I/O A55	I/O A58	GND	1
2	I/O A0	GND	I/O A2	I/O A5	I/O A9	I/O A12	I/O A16	I/O A20	I/O A23	I/O A26	TMS	I/O A29	I/O A33	I/O A36	I/O A39	I/O A43	I/O A47	I/O A50	I/O A54	I/O A57	GND	I/O A59	2
3	I/O D57	I/O D59	GND	I/O A3	I/O A7	I/O A11	I/O A14	I/O A18	I/O A22	I/O A25	Y1	I/O A30	I/O A34	I/O A37	I/O A41	I/O A45	I/O A48	I/O A52	I/O A56	GND	I/O B0	I/O B2	3
4	I/O D55	I/O D54	I/O D56	GND	I/O A8	VCC	I/O A15	I/O A19	VCC	I/O A27	VCC	Y0	I/O A32	VCC	I/O A40	I/O A44	VCC	I/O A51	GND	I/O B3	I/O B5	I/O B4	4
5	I/O D50	I/O D53	I/O D52	I/O D58															I/O B1	I/O B7	I/O B6	I/O B9	5
6	I/O D47	I/O D48	I/O D49	VCC															VCC	I/O B10	I/O B11	I/O B12	6
7	I/O D43	I/O D44	I/O D46	I/O D51			VCC	VCC	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	VCC	VCC			I/O B8	I/O B13	I/O B15	I/O B16	7
8	I/O D40	I/O D41	I/O D42	I/O D45			VCC	NC[1]	GND	GND	GND	GND	GND	GND	NC[1]	VCC			I/O B14	I/O B17	I/O B18	I/O B19	8
9	I/O D36	I/O D37	I/O D39	VCC			NC[1]	GND	GND	GND	GND	GND	GND	GND	GND	NC[1]			VCC	I/O B20	I/O B21	I/O B22	9
10	I/O D33	I/O D34	I/O D35	I/O D38			NC[1]	GND	GND	GND	GND	GND	GND	GND	GND	NC[1]			I/O B23	I/O B24	I/O B25	I/O B26	10
11	EPEN	I/O D31	I/O D32	I/O D27			NC[1]	GND	GND	GND	GND	GND	GND	GND	GND	NC[1]			VCC	I/O B28	I/O B29	I/O B30	11
12	I/O D30	I/O D29	I/O D28	VCC			NC[1]	GND	GND	GND	GND	GND	GND	GND	GND	NC[1]			I/O B27	I/O B32	I/O B31	TDO	12
13	I/O D26	I/O D25	I/O D24	I/O D23			NC[1]	GND	GND	GND	GND	GND	GND	GND	GND	NC[1]			I/O B38	I/O B35	I/O B34	I/O B33	13
14	I/O D22	I/O D21	I/O D20	VCC			NC[1]	GND	GND	GND	GND	GND	GND	GND	GND	NC[1]			VCC	I/O B39	I/O B37	I/O B36	14
15	I/O D19	I/O D18	I/O D17	I/O D14			VCC	NC[1]	GND	GND	GND	GND	GND	GND	NC[1]	VCC			I/O B45	I/O B42	I/O B41	I/O B40	15
16	I/O D16	I/O D15	I/O D13	I/O D8			VCC	VCC	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	VCC	VCC			I/O B51	I/O B46	I/O B44	I/O B43	16
17	I/O D12	I/O D11	I/O D10	VCC															VCC	I/O B49	I/O B48	I/O B47	17
18	I/O D9	I/O D6	I/O D7	I/O D1															I/O B55	I/O B52	I/O B53	I/O B50	18
19	I/O D4	I/O D5	I/O D3	GND	I/O C51	VCC	I/O C44	I/O C40	VCC	I/O C32	I/O C28	VCC	I/O C27	VCC	I/O C19	I/O C15	VCC	I/O C8	GND	I/O B58	I/O B59	I/O B54	19
20	I/O D2	I/O D0	GND	I/O C56	I/O C52	I/O C48	I/O C45	I/O C41	I/O C37	I/O C34	I/O C30	Y2	I/O C25	I/O C22	I/O C18	I/O C14	I/O C11	I/O C7	I/O C3	GND	I/O B56	I/O B57	20
21	I/O C59	GND	I/O C57	I/O C54	I/O C50	I/O C47	I/O C43	I/O C39	I/O C36	I/O C33	RESET	Y3	I/O C26	I/O C23	I/O C20	I/O C16	I/O C12	I/O C9	I/O C5	I/O C2	GND	I/O C0	21
22	GND	I/O C58	I/O C55	I/O C53	I/O C49	I/O C46	I/O C42	I/O C38	I/O C35	I/O C31	TOE	VCCIO	I/O C29	I/O C24	I/O C21	I/O C17	I/O C13	I/O C10	I/O C6	I/O C4	I/O C1	GND	22
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	

ispGDX240VA
Bottom View

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description

ispGDX 240VA – X XXXX X

Device Family

Device Number

Speed
4 = 4.5ns Tpd
7 = 7.0ns Tpd
9 = 9.0ns Tpd

Grade
Blank = Commercial
I = Industrial

Package
B388 = 388-Ball fpBGA

0212/gdx240va
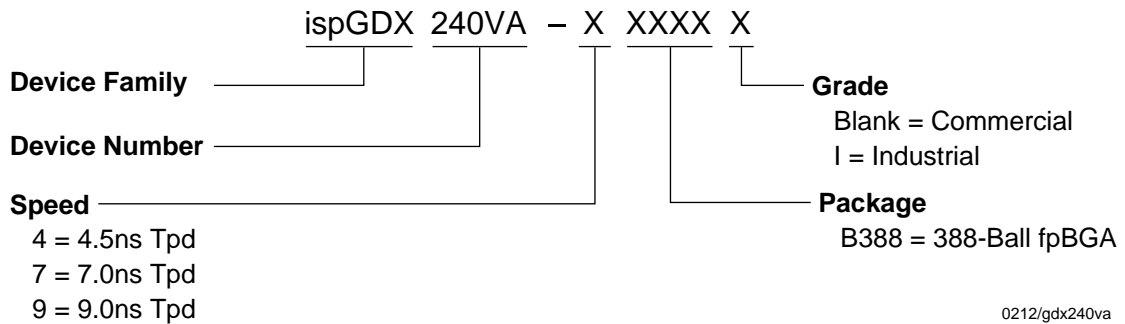
Ordering Information

COMMERCIAL

FAMILY	**t**pd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	4.5	ispGDX240VA-4B388	388-Ball fpBGA
	7	ispGDX240VA-7B388	388-Ball fpBGA

Table 2-0041A/gdx240va

INDUSTRIAL

FAMILY	**t**pd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	7	ispGDX240VA-7B388I	388-Ball fpBGA
	9	ispGDX240VA-9B388I	388-Ball fpBGA

Table 2-0041/gdx240va

Note: The ispGDX240VA devices are dual-marked with both Commercial and Industrial grades.
The Commercial speed grade is faster, e.g. ispGDX240VA-4B388-7I.