ICS421-05

DIGITAL VIDEO CAMERA CLOCK

Description

The ICS421-05 is a low-power, low-jitter clock synthesizer developed for digital camera applications. The device accepts a 27 MHz input clock to support common digital video camera interface frequencies including a 12 MHz for USB, 24.576 MHz for IEEE1394, and a 72 MHz CCD clock. Power consumption was minimized by lowering the voltage requirement to 1.8 V minimum.

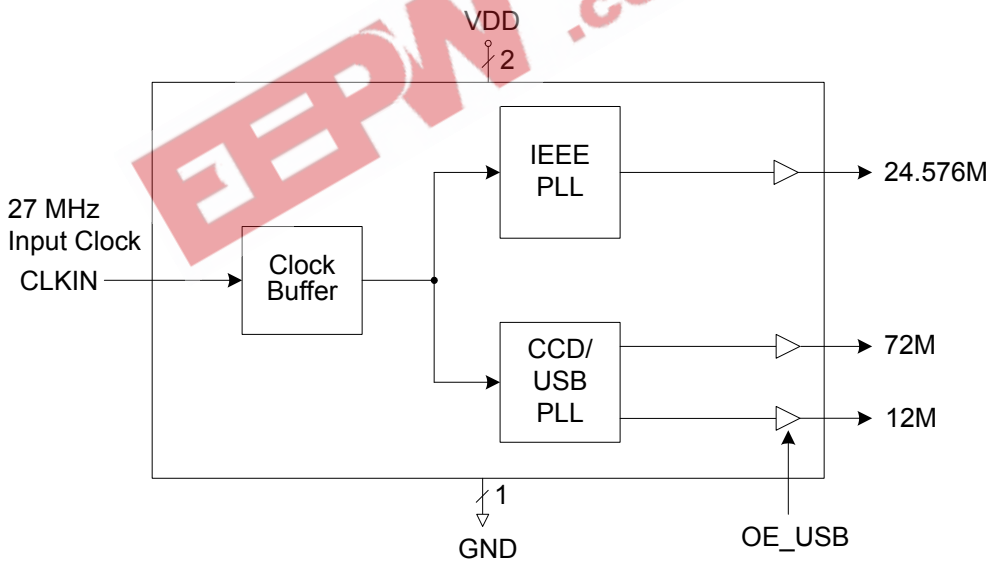
The ICS421-05 utilizes a small form factor 8-pin TSSOP package.

ICS is a leader in low power, consumer application clock sources. Devices are capable of supporting CCD, video, audio, USB, CPU, and other peripherals.

Features

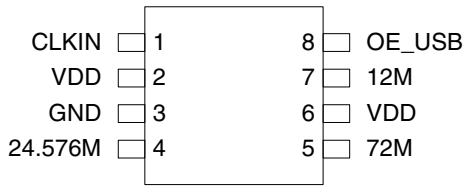
- Ultra-low operating voltage from 1.8 V to 2.4 V
- 10 mA supply current
- 27 MHz input clock frequency
- Fixed 24.576 MHz clock supports IEEE1394
- Fixed 12 MHz clock supports USB
- Fixed 72 MHz CCD clock
- Packaged in 8-pin TSSOP (Pb free)

Block Diagram



Integrated Circuit Systems ● 525 Race Street, San Jose, CA 95126 ● tel (408) 297-1201 ● www.icst.com

Pin Assignment



8 pin (173 mil) TSSOP

OE_USB Operation Table

OE_USB	Function
0	Output tri-state
1	Output running

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	27 MHz single ended clock input.
2	VDD	Power	Connect to voltage supply.
3	GND	Power	Connect to ground.
4	24.576M	Output	24.576 MHz clock output.
5	72M	Output	72 MHz clock output for CCD.
6	VDD	Power	Connect to voltage supply.
7	12M	Output	12 MHz clock output for USB.
8	OE_USB	Input	Output enable for 12M clock for USB. See table for functionality, internal pull-down.

External Components

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS421-05 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and the PCB ground plane.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the ICS421-05. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS421-05. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	-0.5 V to 7 V
All Inputs and Outputs	-0.5 V to VDD +0.5 V
Ambient Operating Temperature	0 to +70 °C
Storage Temperature	-65 to +150 °C
Junction Temperature	125 °C
Soldering Temperature	260 °C

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0	–	+70	°C
Power Supply Voltage (measured in respect to GND)	+1.8		+2.4	V

DC Electrical Characteristics

VDD = 1.8 V to 2.4 V, Ambient Temperature 0 to +70°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.80		2.40	V
Input High Voltage	V_{IH}	CLKIN	VDD/2+0.5			V
Input Low Voltage	V_{IL}	CLKIN			VDD/2-0.5	V
Input High Voltage	V_{IH}	OE_USB pin	TBD			V
Input Low Voltage	V_{IL}	OE_USB pin			TBD	V
Output High Voltage	V_{OH}	VDD = 2.4 V, I_{OH} = -4 mA	1.9			V
Output Low Voltage	V_{OL}	VDD = 2.4 V, I_{OL} = 4 mA			0.4	V
Output High Voltage	V_{OH}	VDD = 1.8 V I_{OH} = -4 mA	1.4			V
Output Low Voltage	V_{OL}	VDD = 1.8 V I_{OL} = 4 mA			0.4	V
Operating Supply Current	IDD	No load, 3 out		10		mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Short Circuit Current	I_{OS}	Each output		50		mA
Nominal Output Impedance	Z_o			20		W
On-chip Pull-down Resistor		OE_USB		150		kΩ

Notes: 1. Nominal switching threshold is VDD/2

AC Electrical Characteristics

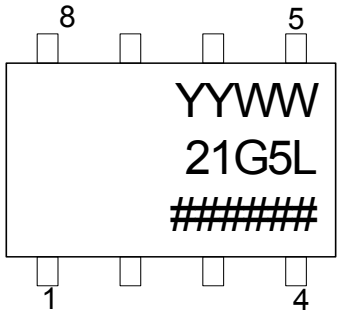
VDD = 1.8 V to 2.4 V, Ambient Temperature 0 to +70°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency		Clock Input		27		MHz
Output Rise Time	t_{OR}	VDD=2.4 V, 20% to 80%, C_L=10 pF		1.8		ns
Output Fall Time	t_{OF}	VDD=2.4 V, 80% to 20%, C_L=10 pF		1.8		ns
Output Rise Time	t_{OR}	VDD=1.8 V, 20% to 80%, C_L=10 pF		2.5		ns
Output Fall Time	t_{OF}	VDD=1.8 V, 80% to 20%, C_L=10 pF		2.5		ns
Output Clock Duty Cycle		at VDD/2		50		%
Absolute Pk-Pk Jitter		72 MHz output clock		±200		ps
PLL Lock Time within 1%		Power OFF to lock			10	ms

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		110		°C/W
	θ_{JA}	1 m/s air flow		100		°C/W
	θ_{JA}	3 m/s air flow		80		°C/W
Thermal Resistance Junction to Case	θ_{JC}			35		°C/W

Marking Diagram



Notes:

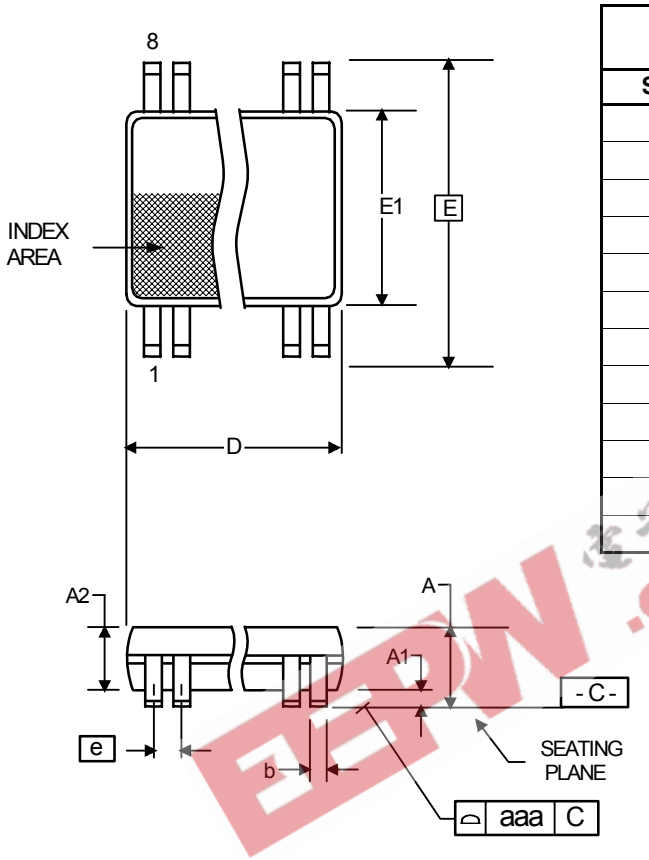
1. ###### is the lot code.

2. YYWW is the last two digits of the year, and the week number that the part was assembled.

3. “L” designates Pb (lead) free package.

Package Outline and Package Dimensions (8-pin TSSOP, 173 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	2.90	3.10	0.114	0.122
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS421G-05LF	21G5L	Tubes	8-pin TSSOP	0 to +70 °C
ICS421G-05LFT		Tape & Reel	8-pin TSSOP	0 to +70 °C

"LF" denotes Pb (lead) free package.