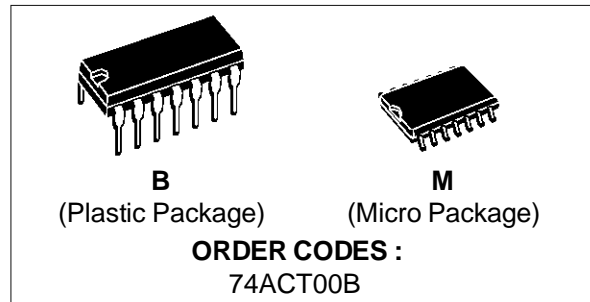


QUAD 2-INPUT NAND GATE

- HIGH SPEED: $t_{PD} = 5 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu A$ (MAX.) at $T_A = 25^\circ C$
- COMPATIBLE WITH TTL OUTPUTS
 $V_{IH} = 2V$ (MIN), $V_{IL} = 0.8V$ (MAX)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 00
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The ACT00 is an advanced high-speed CMOS QUAD 2-INPUT NAND GATE fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power applications maintaining high speed



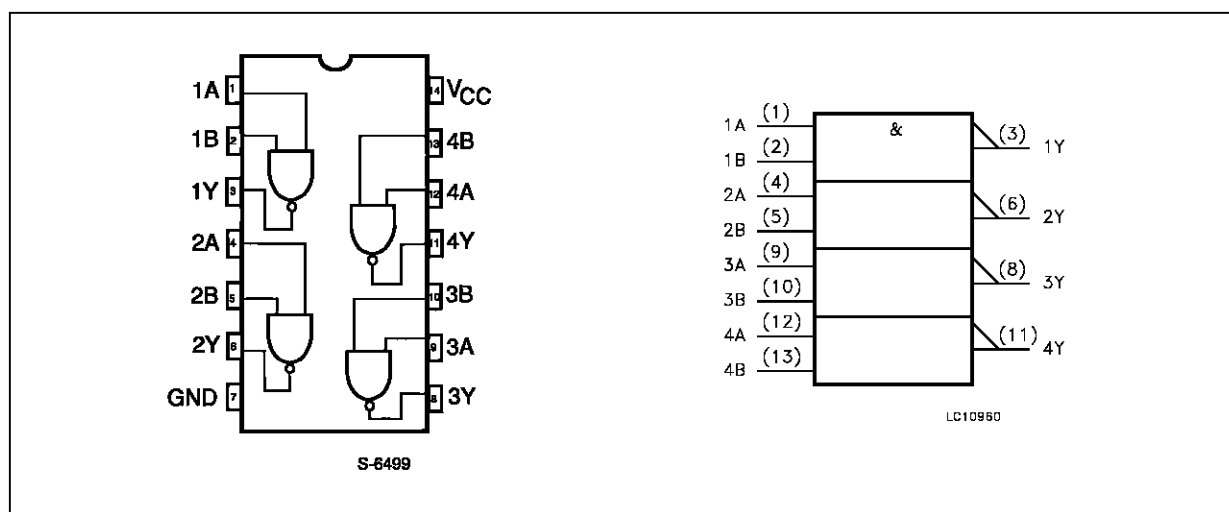
operation similar to equivalent Bipolar Schottky TTL.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

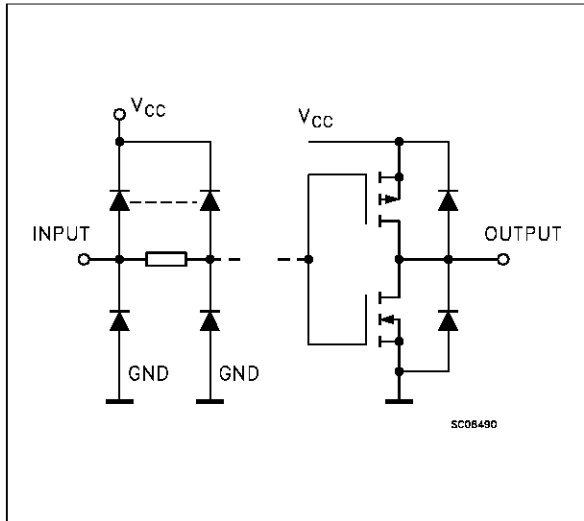
The device is designed to interface directly High Speed CMOS systems with TTL, NMOS and CMOS output voltage levels.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V _{CC}	Positive Supply Voltage

TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 50	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 200	mA
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	4.5 to 5.5	V
V _I	Input Voltage	0 to V _{CC}	V
V _O	Output Voltage	0 to V _{CC}	V
T _{op}	Operating Temperature:	-40 to +85	°C
dt/dv	Input Rise and Fall Time V _{CC} = 4.5 to 5.5V (note 1)	8	ns/V

1) V_{IN} from 0.8 V to 2.0 V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	4.5	V _O = 0.1 V or V _{CC} - 0.1 V	2.0	1.5		2.0		V
		5.5		2.0	1.5		2.0		
V _{IL}	Low Level Input Voltage	4.5	V _O = 0.1 V or V _{CC} - 0.1 V		1.5	0.8		0.8	V
		5.5			1.5	0.8		0.8	
V _{OH}	High Level Output Voltage	4.5	V _I ^(*) = V _{IH} or V _{IL}	I _O = -50 μA	4.4	4.49		4.4	V
		5.5			5.4	5.49		5.4	
		4.5		I _O = -24 mA	3.86			3.76	
		5.5			4.86			4.76	
V _{OL}	Low Level Output Voltage	4.5	V _I ^(*) = V _{IH} or V _{IL}	I _O = 50 μA	0.001	0.1		0.1	V
		5.5			0.001	0.1		0.1	
		4.5		I _O = 24 mA			0.36		0.44
		5.5					0.36		0.44
I _I	Input Leakage Current	5.5	V _I = V _{CC} or GND			±0.1		±1	μA
I _{CC1}	Max I _{CC} /Input	5.5	V _I = V _{CC} - 2.1 V		0.6			1.5	mA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40	μA
I _{OLD}	Dynamic Output Current (note 1, 2)	5.5	V _{OLD} = 1.65 V max					75	mA
I _{OHD}			V _{OHD} = 3.85 V min					-75	mA

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50 Ω.

(*) All outputs loaded.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input t_r = t_f = 3 ns)

Symbol	Parameter	Test Condition		Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time	5.0 ^(*)		1.5	5.0	9.0	1.0	9.5	ns

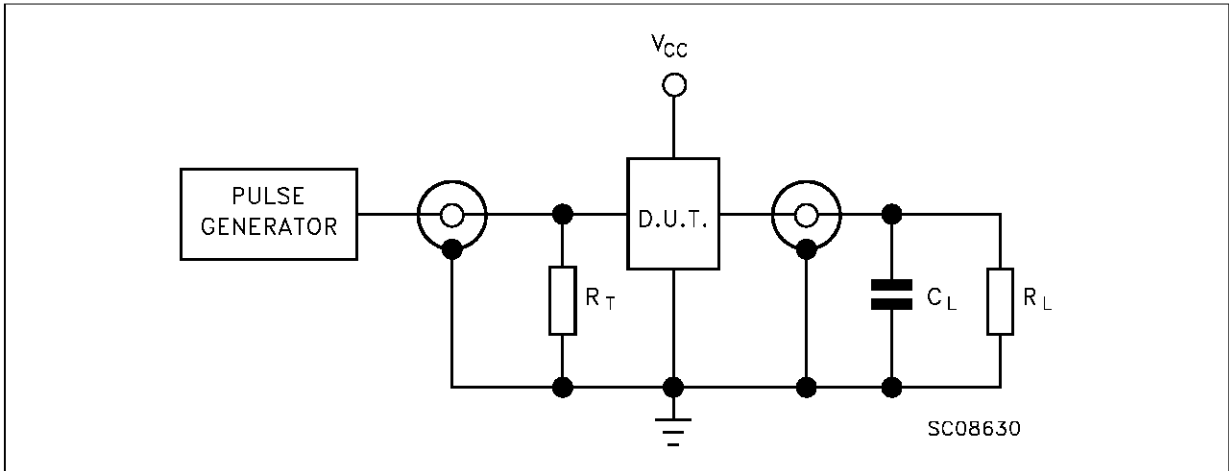
(*) Voltage range is 5V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
C _{IN}	Input Capacitance	5.0			4				pF
C _{PD}	Power Dissipation Capacitance (note 1)	5.0			31				pF

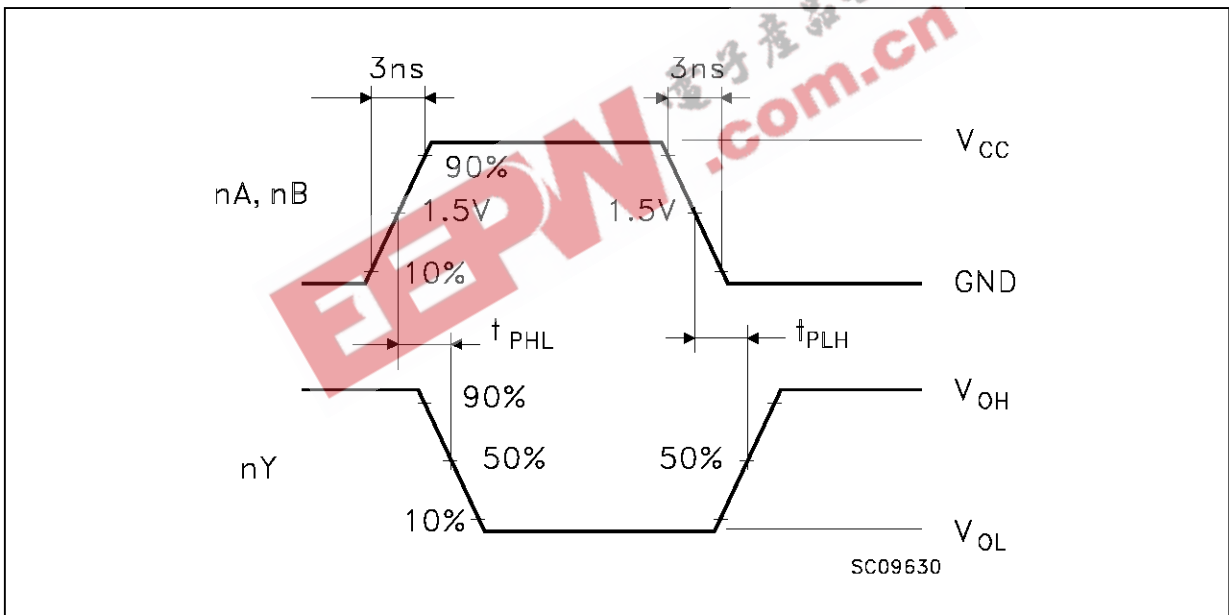
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} • V_{CC} • f_{IN} + I_{CC/n} (per circuit)

TEST CIRCUIT



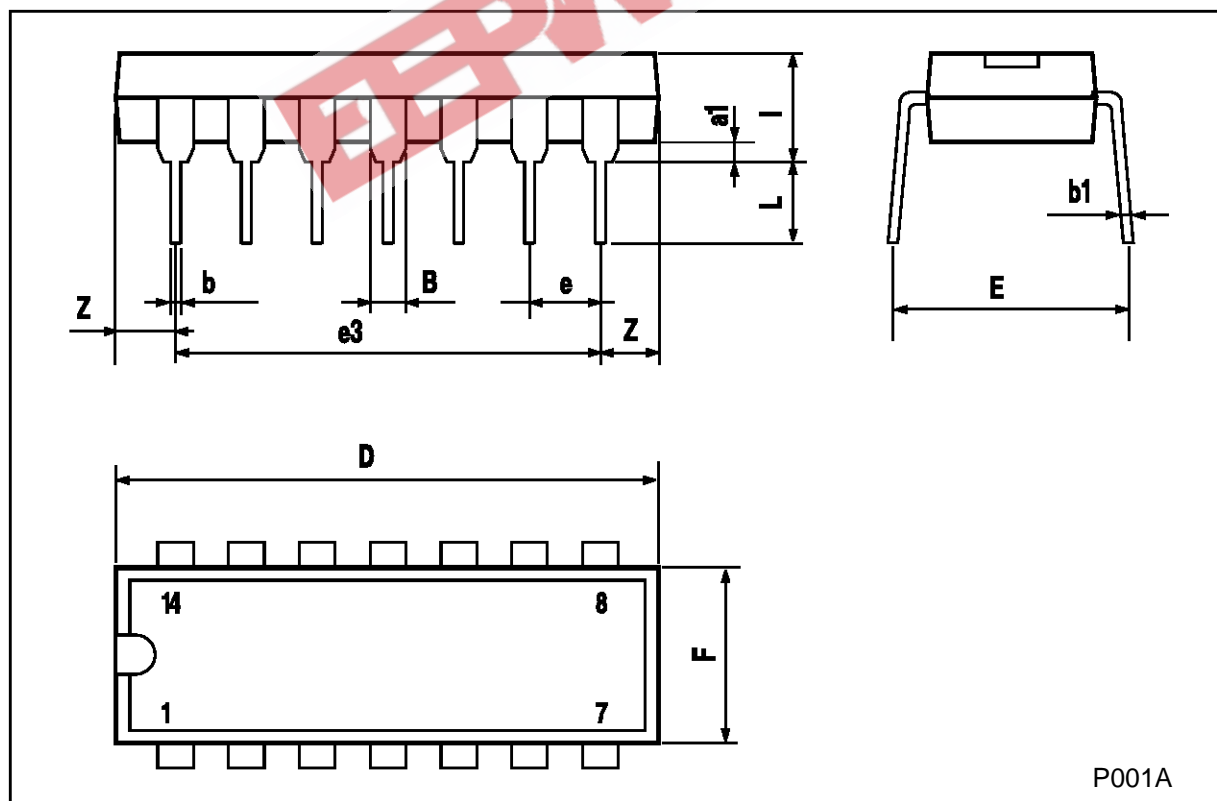
$C_L = 50 \text{ pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = R_T = 500\Omega$ or equivalent
 $R_T = Z_{out}$ of pulse generator (typically 50Ω)

WAVEFORM: PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)



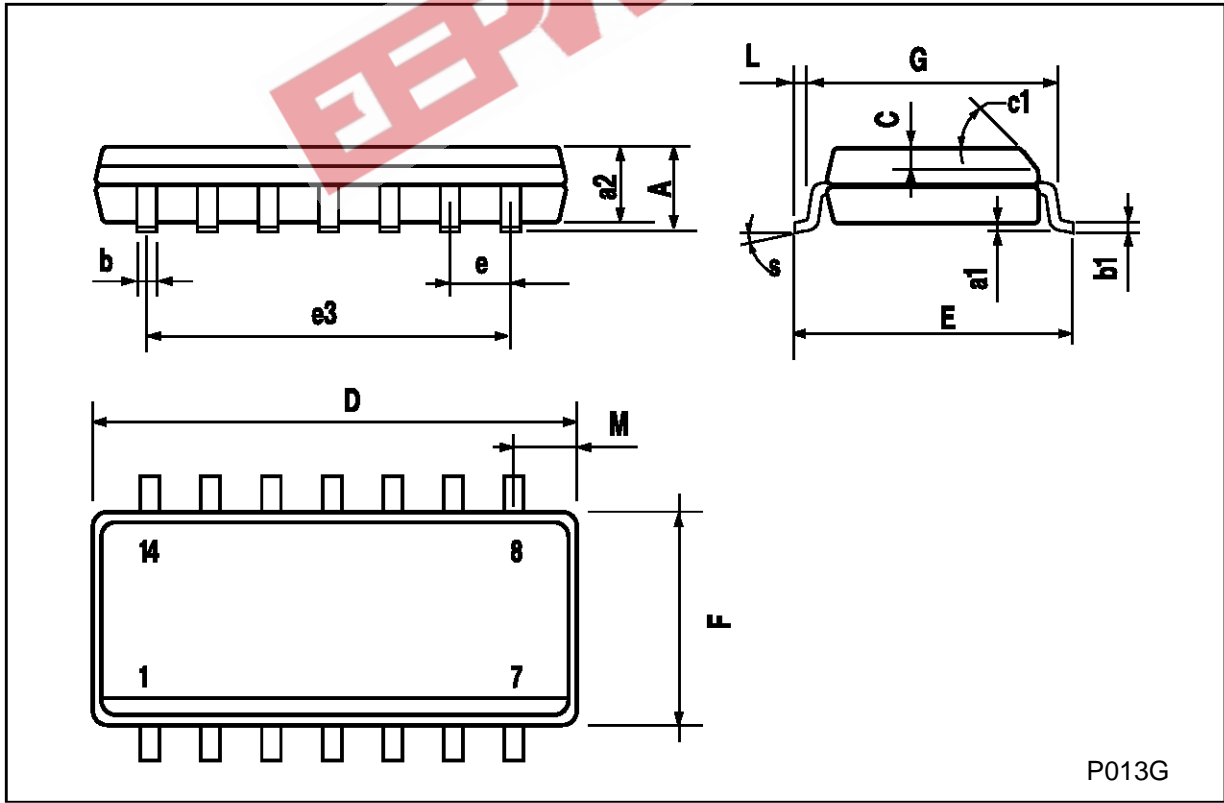
Plastic DIP14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



SO14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8 (max.)					



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