

## 74VCX38

### Low Voltage Quad 2-Input NAND Gate with Open Drain Outputs and 3.6V Tolerant Inputs and Outputs

#### General Description

The VCX38 contains four 2-input NAND gates with open drain outputs. This product is designed for low voltage (1.2V to 3.6V)  $V_{CC}$  applications with I/O compatibility up to 3.6V.

The VCX38 is fabricated with advanced CMOS technology to achieve high-speed operation while maintaining CMOS low power dissipation.

#### Features

- 1.2V to 3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- $t_{PD}$ 
  - 2.8 ns max for 3.0V to 3.6V  $V_{CC}$
- Power-Off high impedance inputs and outputs
- Static Drive ( $I_{OL}$ )
  - +24 mA @ 3.0V  $V_{CC}$
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Latchup performance exceeds JEDEC 78 conditions
- ESD performance:
  - Human body model > 2000V
  - Machine model > 250V
- Leadless Pb-Free DQFN package

#### Ordering Code:

Order Number	Package Number	Package Description
74VCX38M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VCX38BQX (Note 1)	MLP014A	Pb-Free 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
74VCX38MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VCX38MTCX_NL	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

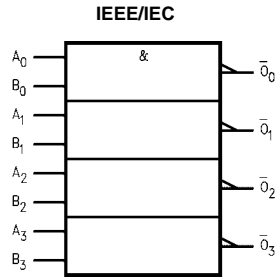
Pb-Free package per JEDEC J-STD-020B.

**Note 1:** DQFN package available in Tape and Reel.

Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

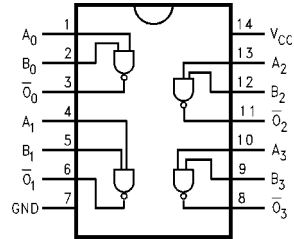
74VCX38 Low Voltage Quad 2-Input NAND Gate with Open Drain Outputs and 3.6V Tolerant Inputs and Outputs

**Logic Symbol**



**Connection Diagrams**

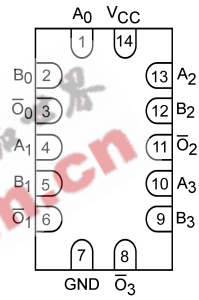
Pin Assignments for SOIC and TSSOP



**Pin Descriptions**

Pin Names	Description
$A_n, B_n$	Inputs
$\bar{O}_n$	Outputs

Pad Assignments for DQFN



(Top View)

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Absolute Maximum Ratings (Note 2)		Recommended Operating Conditions (Note 4)				
Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V	Power Supply				
DC Input Voltage ( $V_I$ )	-0.5V to +4.6V	Operating	1.2V to 3.6V			
Output Voltage ( $V_O$ ) (Note 3)	-0.5V to +4.6V	Input Voltage	-0.3V to 3.6V			
DC Input Diode Current ( $I_{IK}$ )		Output Voltage ( $V_O$ )	0V to 3.6V			
$V_I < 0V$	-50 mA	Output Current in $I_{OL}$				
DC Output Diode Current ( $I_{OK}$ )		$V_{CC} = 3.0V$ to 3.6V	+24 mA			
$V_O < 0V$	-50 mA	$V_{CC} = 2.3V$ to 2.7V	+18 mA			
DC Output Source/Sink Current ( $I_{OL}$ )	+50 mA	$V_{CC} = 1.65V$ to 2.3V	+6 mA			
DC $V_{CC}$ or Ground Current per	$\pm 100$ mA	$V_{CC} = 1.4V$ to 1.6V	+2 mA			
Supply Pin ( $I_{CC}$ or Ground)		$V_{CC} = 1.2V$	$\pm 100$ $\mu A$			
Storage Temperature Range ( $T_{stg}$ )	-65°C to +150°C	Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C			
		Minimum Input Edge Rate ( $\Delta V/\Delta V$ )				
		$V_{in} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V			
		<p><b>Note 2:</b> The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.</p> <p><b>Note 3:</b> <math>I_O</math> Absolute Maximum Rating must be observed.</p> <p><b>Note 4:</b> Floating or unused inputs must be held HIGH or LOW</p>				
DC Electrical Characteristics						
Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.7 - 3.6 2.3 - 2.7 1.65 - 2.3 1.4 - 1.6 1.2	2.0 1.6 $0.65 \times V_{CC}$ $0.65 \times V_{CC}$ $0.65 \times V_{CC}$		V
$V_{IL}$	LOW Level Input Voltage		2.7 - 3.6 2.3 - 2.7 1.65 - 2.3 1.4 - 1.6 1.2		0.8 0.7 $0.35 \times V_{CC}$ $0.35 \times V_{CC}$ $0.05 \times V_{CC}$	V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$ $I_{OL} = 12$ mA $I_{OL} = 18$ mA $I_{OL} = 24$ mA $I_{OL} = 100 \mu A$ $I_{OL} = 12$ mA $I_{OL} = 18$ mA $I_{OL} = 100 \mu A$ $I_{OL} = 6$ mA $I_{OL} = 100 \mu A$ $I_{OL} = 2$ mA $I_{OL} = 100 \mu A$	2.7 - 3.6 2.7 3.0 3.0 2.3 - 2.7 2.3 2.3 1.65 - 2.3 1.65 1.4 - 1.6 1.4 1.2		0.2 0.4 0.4 0.55 0.2 0.4 0.6 0.2 0.3 0.2 0.35 0.05	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	1.2 - 3.6		$\pm 5.0$	$\mu A$
$I_{OFF}$	Power-Off Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10.0	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND $V_{CC} \leq (V_I) \leq 3.6V$	1.2 - 3.6 1.2 - 3.6		20.0 $\pm 20.0$	$\mu A$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	2.7 - 3.6		750	$\mu A$
$I_{OHZ}$	Off State Current	$V_O = 3.6$	1.2 - 3.6		10.0	$\mu A$

AC Electrical Characteristics (Note 5)							
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Figure Number
				Min	Max		
t <sub>PZL</sub> t <sub>PLZ</sub>	Propagation Delay	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	0.6	2.8	ns	Figures 1, 2
			2.5 ± 0.2	0.8	3.7		
			1.8 ± 0.15	1.0	6.7		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2kΩ	1.5 ± 0.1	1.0	13.4		Figures 3, 4
		1.2		33.5			
t <sub>OSSL</sub> t <sub>OSLH</sub>	Output to Output Skew (Note 6)	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2kΩ	1.5 ± 0.1		1.5		
			1.2		1.5		

**Note 5:** For C<sub>L</sub> = 50pF, add approximately 300 ps to the 30 pF AC maximum specification.

**Note 6:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

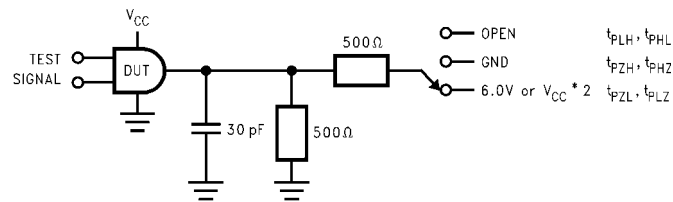
### Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C	Units
				Typical	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8 2.5 3.3	0.25 0.6 0.8	V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8 2.5 3.3	-0.25 -0.6 -0.8	V

### Capacitance

Symbol	Parameter	Conditions	T <sub>A</sub> = +25°C	Units
			Typical	
C <sub>IN</sub>	Input Capacitance	V <sub>I</sub> = 0V OR V <sub>CC</sub> , V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	6.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	7.0	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz, V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	20.0	pF

### AC Loading and Waveforms ( $V_{CC}$ $3.3V \pm 0.3V$ to $1.8V \pm 0.15V$ )



TEST	SWITCH
$t_{PZL}$ , $t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ ; $V_{CC} \times 2$ at $V_{CC} = 2.5V \pm 0.2V$ ; 1.8V

FIGURE 1. AC Test Circuit

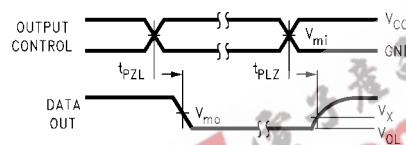
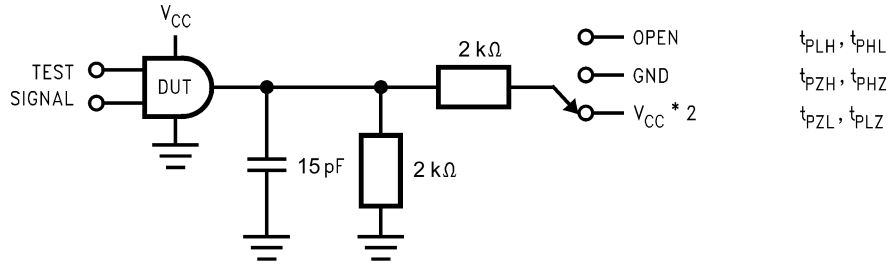


FIGURE 2. Waveform for Open Drain, Inverting and Non-inverting Functions

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
$V_{mi}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$

AC Loading and Waveforms ( $V_{CC} 1.5 \pm 0.1V$  to  $1.2V$ )



TEST	SWITCH
$t_{PZL}, t_{PLZ}$	$V_{CC} * 2$ at $V_{CC} = 1.5V \pm 0.1V$

FIGURE 3. AC Test Circuit

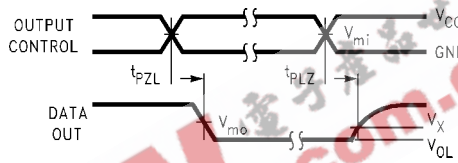


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

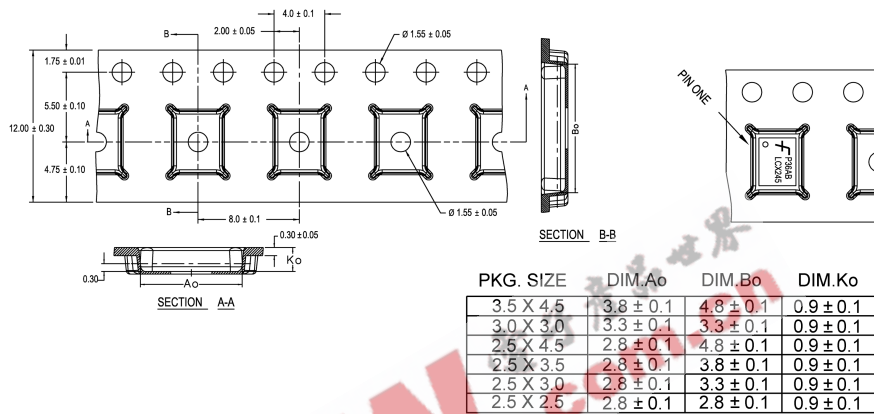
Symbol	$V_{CC}$
	$1.5V \pm 0.1V$
$V_{mi}$	$V_{CC}/2$
$V_{mo}$	$V_{CC}/2$
$V_x$	$V_{OL} + 0.1V$
$V_y$	$V_{OH} - 0.1V$

### Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

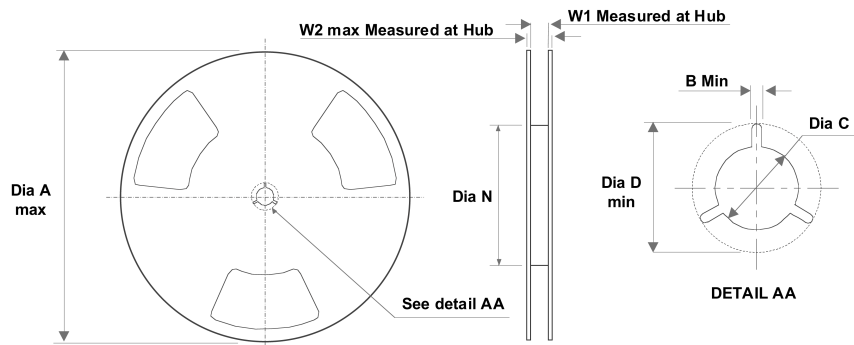
**TAPE DIMENSIONS** inches (millimeters)



NOTES: unless otherwise specified

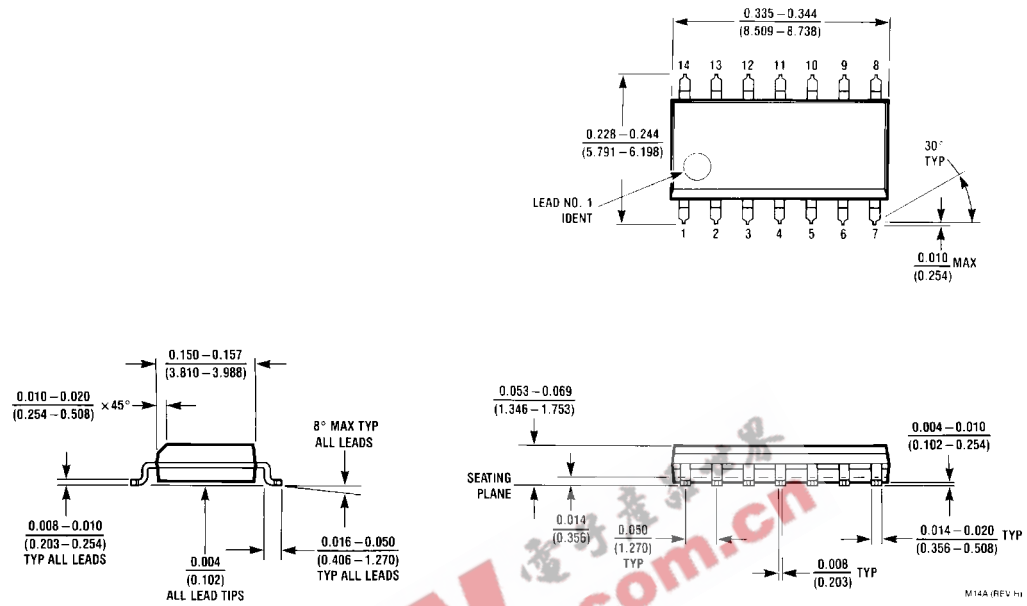
- Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
- Smallest allowable bending radius.
- Thru hole inside cavity is centered within cavity.
- Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
- Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
- Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
- Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
- Controlling dimension is millimeter. Dimension in inches rounded.

**REEL DIMENSIONS** inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

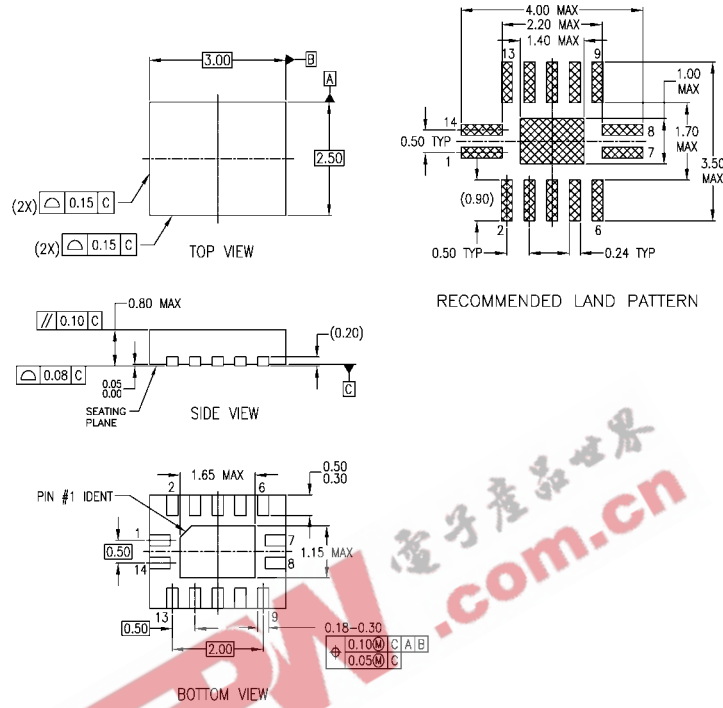
**Physical Dimensions** inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M14A



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP014ArevA

**Pb-Free 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm Package Number MLP014A**

### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

**LAND PATTERN RECOMMENDATION**

**DETAIL A**

**NOTES:**

- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
- DIMENSIONS ARE IN MILLIMETERS
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1992

MTC14revD

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

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