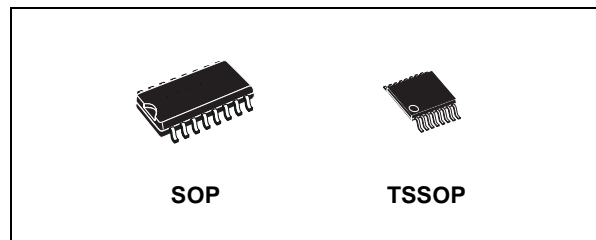




# 74LVX257

## LOW VOLTAGE CMOS QUAD 2 CHANNEL MULTIPLEXER (3-STATE) WITH 5V TOLERANT INPUTS

- HIGH SPEED:  
 $t_{PD}=5.8ns$  (TYP.) at  $V_{CC} = 3.3V$
- 5V TOLERANT INPUTS
- POWER-DOWN PROTECTION ON INPUTS
- INPUT VOLTAGE LEVEL:  
 $V_{IL} = 0.8V, V_{IH} = 2V$  at  $V_{CC} = 3V$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4 \mu A$  (MAX.) at  $T_A=25^\circ C$
- LOW NOISE:  
 $V_{OLP} = 0.3V$  (TYP.) at  $V_{CC} = 3.3V$
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 4 mA$  (MIN) at  $V_{CC} = 3V$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}(OPR) = 2V$  to  $3.6V$  (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 257
- IMPROVED LATCH-UP IMMUNITY



### ORDER CODES

PACKAGE	TUBE	T & R
SOP	74LVX257M	74LVX257MTR
TSSOP		74LVX257TTR

### DESCRIPTION

The 74LVX257 is a low voltage CMOS QUAD 2 CHANNEL MULTIPLEXER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. It is ideal for low power, battery operated and low noise 3.3V applications.

It is composed of four independent 2-channel multiplexers with common SELECT and ENABLE (OE) INPUT. The 74LVX257 is a non-inverting

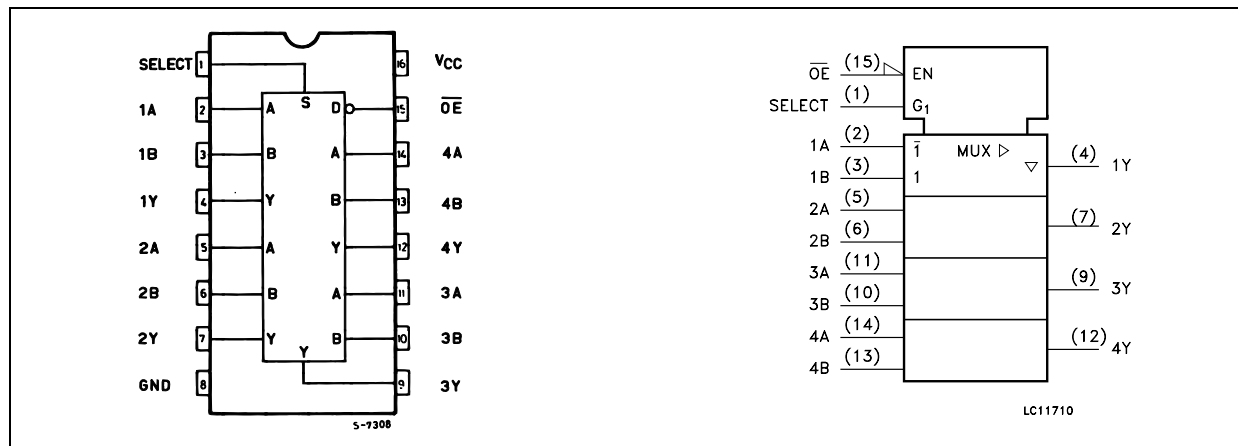
multiplexer. When the ENABLE INPUT is held "High", all outputs become in high impedance state. If SELECT INPUT is held "Low", "A" data is selected, when SELECT INPUT is "High", "B" data is chosen.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage.

This device can be used to interface 5V to 3V. It combines high speed performance with the true CMOS low power consumption.

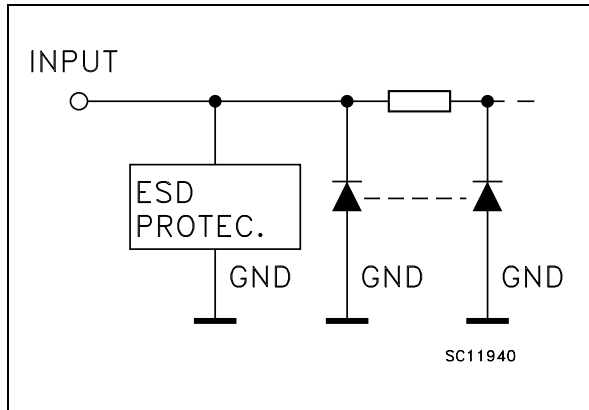
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



# 74LVX257

## INPUT EQUIVALENT CIRCUIT



## PIN DESCRIPTION

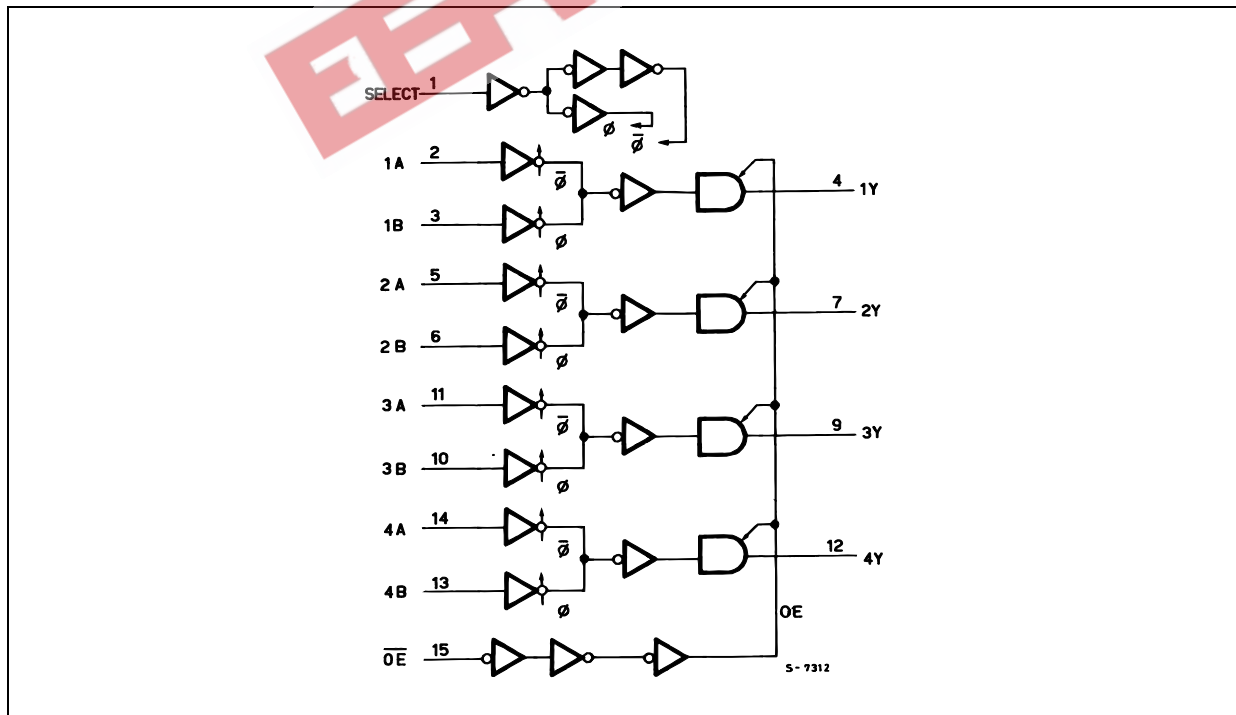
PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Inputs
2, 5, 11, 14	1A to 4A	Data Inputs From Source A
3, 6, 10, 13	1B to 4B	Data Inputs From Source B
4, 7, 9, 12	1Y to 4Y	3 State Multiplexer Outputs
15	OE	3 State Output Enable Inputs (Active LOW)
8	GND	Ground (0V)
16	V <sub>CC</sub>	Positive Supply Voltage

## TRUTH TABLE

INPUTS				OUTPUT
OE	SELECT	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X : Don't Care  
Z : High Impedance

## LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7.0	V
$V_I$	DC Input Voltage	-0.5 to +7.0	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	- 20	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage (note 1)	2 to 3.6	V
$V_I$	Input Voltage	0 to 5.5	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	$^{\circ}C$
dt/dv	Input Rise and Fall Time (note 2) ( $V_{CC} = 3V$ )	0 to 100	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V

2)  $V_{IN}$  from 0.8V to 2.0V

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^{\circ}C$			-40 to 85 $^{\circ}C$		-55 to 125 $^{\circ}C$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$V_{IH}$	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0		2.0			2.0		2.0		
		3.6		2.4			2.4		2.4		
$V_{IL}$	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0				0.8		0.8		0.8	
		3.6				0.8		0.8		0.8	
$V_{OH}$	High Level Output Voltage	2.0	$I_O = -50 \mu A$	1.9	2.0		1.9		1.9		V
		3.0	$I_O = -50 \mu A$	2.9	3.0		2.9		2.9		
		3.0	$I_O = -4 mA$	2.58			2.48		2.4		
$V_{OL}$	Low Level Output Voltage	2.0	$I_O = 50 \mu A$		0.0	0.1		0.1		0.1	V
		3.0	$I_O = 50 \mu A$		0.0	0.1		0.1		0.1	
		3.0	$I_O = 4 mA$			0.36		0.44		0.55	
$I_{OZ}$	High Impedance Output Leakage Current	3.6	$V_I = V_{IH}$ or $V_{IL}$ $V_O = V_{CC}$ or GND			$\pm 0.25$		$\pm 2.5$		$\pm 5$	$\mu A$
$I_I$	Input Leakage Current	3.6	$V_I = 5.5V$ or GND			$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu A$
$I_{CC}$	Quiescent Supply Current	3.6	$V_I = V_{CC}$ or GND			4		40		40	$\mu A$

## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>OLP</sub>	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C <sub>L</sub> = 50 pF		0.3	0.5					V
V <sub>OLV</sub>				-0.5	-0.3						
V <sub>IHD</sub>	Dynamic High Voltage Input (note 1, 3)	3.3		2.0							
V <sub>ILD</sub>	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f=1MHz.

AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time A, B, to Y	2.7	15		7.0	13.0	1.0	15.4	1.0	16.4	ns
		2.7	50		9.5	18.0	1.0	20.3	1.0	21.3	
		3.3(*)	15		5.8	9.3	1.0	11.0	1.0	12.0	
		3.3(*)	50		8.3	12.8	1.0	14.5	1.0	15.5	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time SELECT to Y	2.7	15		8.5	15.4	1.0	18.2	1.0	20.0	ns
		2.7	50		10.5	20.3	1.0	23.1	1.0	24.5	
		3.3(*)	15		7.0	11.0	1.0	13.0	1.0	14.0	
		3.3(*)	50		9.5	14.5	1.0	16.5	1.0	18.0	
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	2.7	15		8.0	14.7	1.0	17.5	1.0	18.5	ns
		2.7	50		10.5	19.6	1.0	22.4	1.0	24.0	
		3.3(*)	15		6.7	10.5	1.0	12.5	1.0	13.5	
		3.3(*)	50		9.2	14.0	1.0	16.0	1.0	17.0	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time	2.7	50		9.5	16.8	1.0	18.9	1.0	20.0	ns
		3.3(*)	50		8.6	12.0	1.0	13.5	1.0	15.0	
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew Time (note 1,2)	2.7	50		0.5	1.0		1.5		1.5	ns
		3.3(*)	50		0.5	1.0		1.5		1.5	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW

2) Parameter guaranteed by design

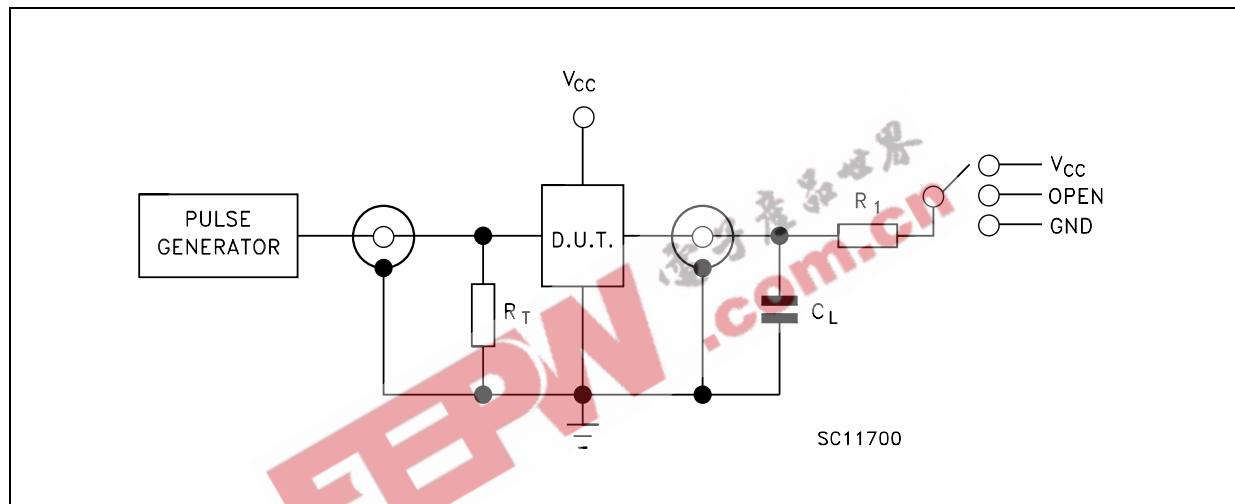
(\*) Voltage range is 3.3V ± 0.3V

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance	3.3			4	10		10		10	pF
C <sub>OUT</sub>	Output Capacitance	3.3			6						pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	3.3			23						pF

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$  (per channel)

## TEST CIRCUIT



TEST	SWITCH
t <sub>PLH</sub> , t <sub>PHL</sub>	Open
t <sub>PZL</sub> , t <sub>PLZ</sub>	V <sub>CC</sub>
t <sub>PZH</sub> , t <sub>PHZ</sub>	GND

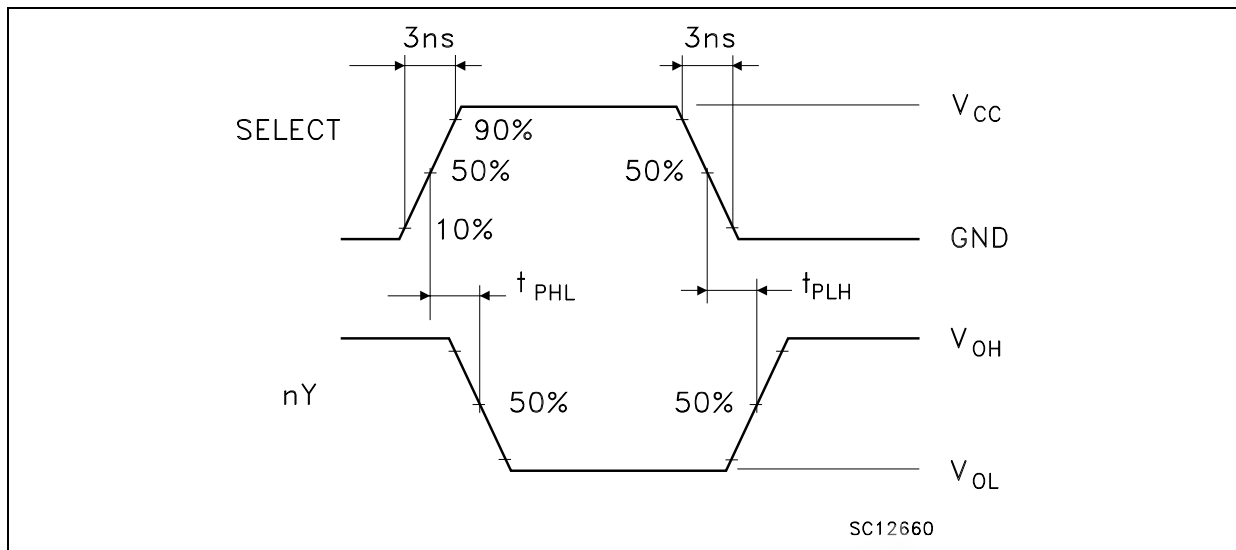
C<sub>L</sub> = 15/50pF or equivalent (includes jig and probe capacitance)

R<sub>L</sub> = R<sub>1</sub> = 1KΩ or equivalent

R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50Ω)

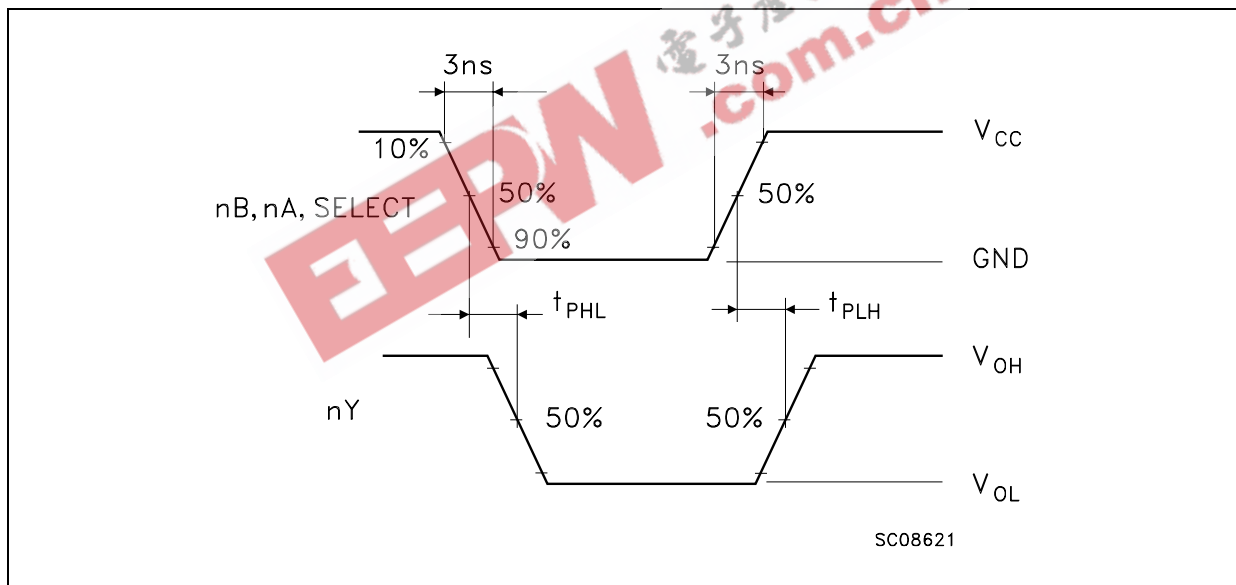
**WAVEFORM 1 : PROPAGATION DELAYS FOR INVERTING CONDITIONS**

(f=1MHz; 50% duty cycle)

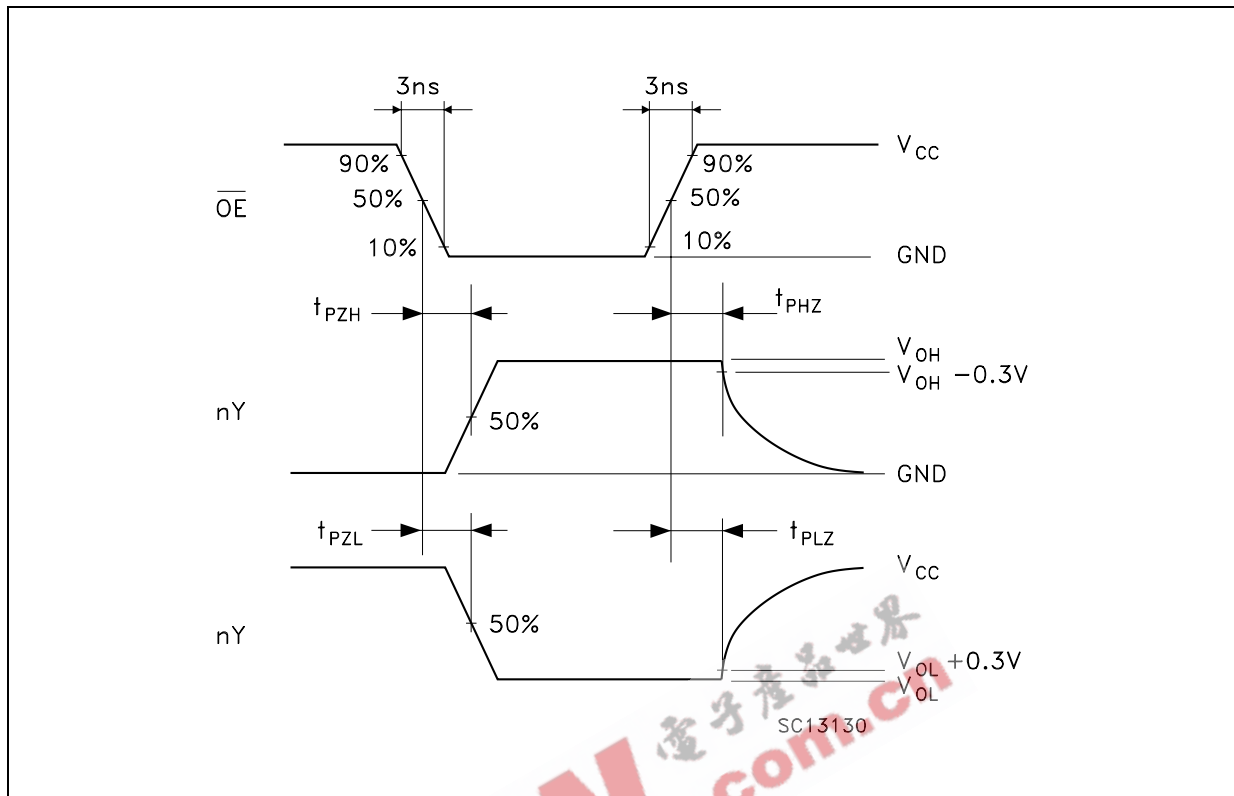


**WAVEFORM 2 : PROPAGATION DELAYS FOR NON-INVERTING CONDITIONS**

(f=1MHz; 50% duty cycle)

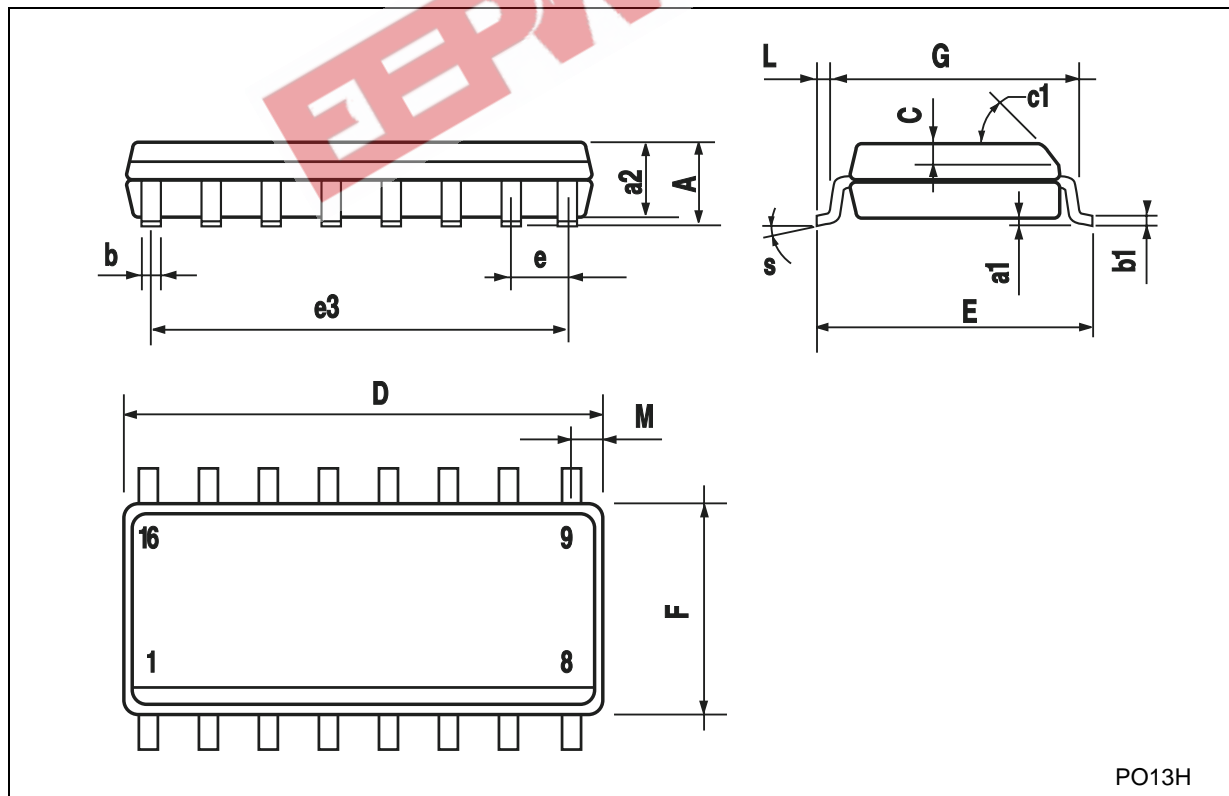


WAVEFORM 3 : OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



## SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					

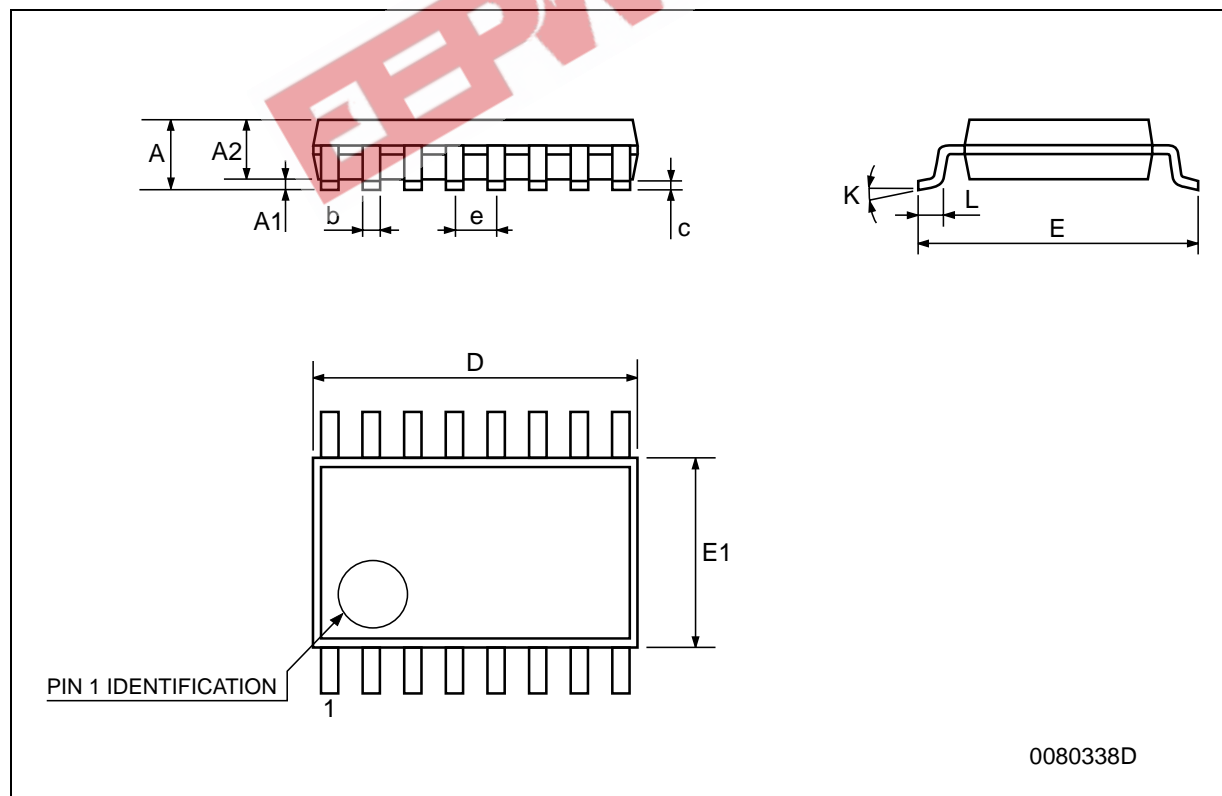


PO13H



## TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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