- **State-of-the-Art Advanced BiCMOS Technology (ABT) *Widebus*™ Design for 2.5-V and 3.3-V Operation and Low Static Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **High Drive (–24/24 mA at 2.5-V and –32/64 mA at 3.3-V V_{CC})**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **High-Impedance State During Power Up and Power Down Prevents Driver Conflict**
- **Uses Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating**
- **Auto3-State Eliminates Bus Current Loading When Output Exceeds V_{CC} + 0.5 V**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model; and Exceeds 1000 V Using Charged-Device Model, Robotic Method**
- **Flow-Through Architecture Facilitates Printed Circuit Board Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package**

SN54ALVTH16373 . . . WD PACKAGE
SN74ALVTH16373 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	48	1LE
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
V_{CC}	7	42	V_{CC}
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
V_{CC}	18	31	V_{CC}
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
2$\overline{OE}$	24	25	2LE

description

The ’ALVTH16373 devices are 16-bit transparent D-type latches with 3-state outputs designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

description (continued)

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

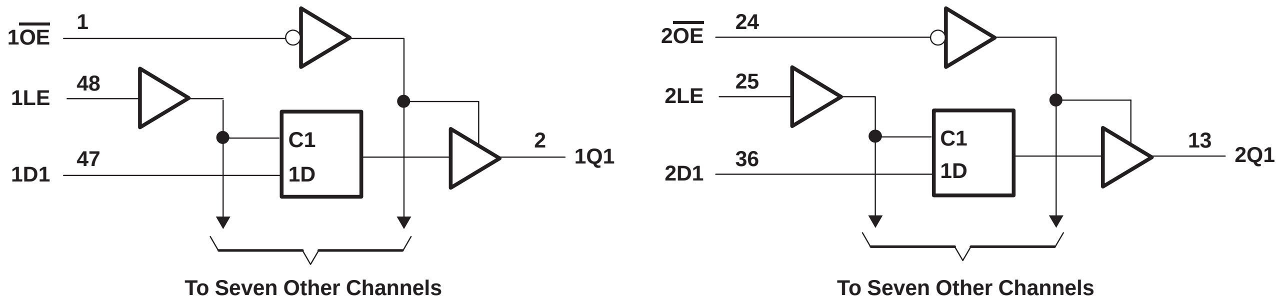
When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ALVTH16373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALVTH16373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to 7 V
Voltage range applied to any output in the high-impedance
or power-off state, V_O (see Note 1) . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1) . . . . –0.5 V to 7 V
Output current in the low state, I_O: SN54ALVTH16373 . . . . 96 mA
SN74ALVTH16373 . . . . 128 mA
Output current in the high state, I_O: SN54ALVTH16373 . . . . –48 mA
SN74ALVTH16373 . . . . –64 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . 89°C/W
DGV package . . . . 93°C/W
DL package . . . . 94°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions, V_{CC} = 2.5 V ± 0.2 V (see Note 3)

			SN54ALVTH16373			SN74ALVTH16373			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		2.3		2.7	2.3		2.7	V
V_{IH}	High-level input voltage		1.7			1.7			V
V_{IL}	Low-level input voltage				0.7			0.7	V
V_I	Input voltage		0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current				–6			–8	mA
I_{OL}	Low-level output current				6			8	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 kHz				18			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			200			µs/V
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions, V_{CC} = 3.3 V ± 0.3 V (see Note 3)

			SN54ALVTH16373			SN74ALVTH16373			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		3		3.6	3		3.6	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input voltage		0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current				–24			–32	mA
I_{OL}	Low-level output current				24			32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 kHz				48			64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			200			µs/V
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALVTH16373 MIN	SN54ALVTH16373 TYP†	SN54ALVTH16373 MAX	SN74ALVTH16373 MIN	SN74ALVTH16373 TYP†	SN74ALVTH16373 MAX	UNIT
V_{IK}	V_{CC} = 2.3 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = 2.3 V to 2.7 V,	I_{OH} = –100 µA	V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.3 V	I_{OH} = –6 mA	1.8						
		I_{OH} = –8 mA				1.8			
V_{OL}	V_{CC} = 2.3 V to 2.7 V,	I_{OL} = 100 µA			0.2			0.2	V
	V_{CC} = 2.3 V	I_{OL} = 6 mA			0.4				
		I_{OL} = 8 mA						0.4	
		I_{OL} = 18 mA			0.5				
		I_{OL} = 24 mA						0.5	
I_I Control inputs	V_{CC} = 2.7 V,	$V_I = V_{CC}$ or GND			±1			±1	µA
	V_{CC} = 0 or 2.7 V,	V_I = 5.5 V			10			10	
I_I Data inputs	V_{CC} = 2.7 V	V_I = 5.5 V			10			10	
		$V_I = V_{CC}$			1			1	
		V_I = 0			–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
I_{BHL}‡	V_{CC} = 2.3 V,	V_I = 0.7 V		115			115		µA
I_{BHH}§	V_{CC} = 2.3 V,	V_I = 1.7 V		–10			–10		µA
I_{BHLO}¶	V_{CC} = 2.7 V,	V_I = 0 to V_{CC}	300			300			µA
I_{BHHO}#	V_{CC} = 2.7 V,	V_I = 0 to V_{CC}	–300			–300			µA
I_{EX}‖	V_{CC} = 2.3 V,	V_O = 5.5 V			125			125	µA
$I_{OZ(PU/PD)}$☆	V_{CC} ≤ 1.2 V, V_O = 0.5 V to V_{CC}, V_I = GND or V_{CC}, $\overline{OE}$ = don't care				±100			±100	µA
I_{OZH}	V_{CC} = 2.7 V	V_O = 2.3 V, V_I = 0.7 V or 1.7 V			5			5	µA
I_{OZL}	V_{CC} = 2.7 V	V_O = 0.5 V, V_I = 0.7 V or 1.7 V			–5			–5	µA
I_{CC}	V_{CC} = 2.7 V, I_O = 0, $V_I = V_{CC}$ or GND	Outputs high		0.04	0.1		0.04	0.1	mA
		Outputs low		2.3	4.5		2.3	4.5	
		Outputs disabled		0.04	0.1		0.04	0.1	
C_i	V_{CC} = 2.5 V,	V_I = 2.5 V or 0		3.5			3.5		pF
C_o	V_{CC} = 2.5 V,	V_O = 2.5 V or 0		6			6		pF

† All typical values are at V_{CC} = 2.5 V, T_A = 25°C.
‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
¶ An external driver must source at least I_{BHLO} to switch this node from low to high.
# An external driver must sink at least I_{BHHO} to switch this node from high to low.
‖ Current into an output in the high state when $V_O > V_{CC}$
☆ High-impedance state during power up or power down

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH16373			SN74ALVTH16373			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 3 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 3 V to 3.6 V,	I_{OH} = –100 µA	V_{CC}–0.2			V_{CC}–0.2			V
		V_{CC} = 3 V	I_{OH} = –24 mA	2						
			I_{OH} = –32 mA				2			
V_{OL}		V_{CC} = 3 V to 3.6 V,	I_{OL} = 100 µA			0.2			0.2	V
		V_{CC} = 3 V	I_{OL} = 16 mA						0.4	
			I_{OL} = 24 mA			0.5				
			I_{OL} = 32 mA						0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	
	Data inputs	V_{CC} = 3.6 V	V_I = 5.5 V			10			10	
			V_I = V_{CC}			1			1	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
I_{BHL}‡		V_{CC} = 3 V,	V_I = 0.8 V	75			75			µA
I_{BHH}§		V_{CC} = 3 V,	V_I = 2 V	–75			–75			µA
I_{BHLO}¶		V_{CC} = 3.6 V,	V_I = 0 to V_{CC}	500			500			µA
I_{BHHO}#		V_{CC} = 3.6 V,	V_I = 0 to V_{CC}	–500			–500			µA
I_{EX}‖		V_{CC} = 3 V,	V_O = 5.5 V			125			125	µA
$I_{OZ(PU/PD)}$☆		V_{CC} ≤ 1.2 V, V_O = 0.5 V to V_{CC}, V_I = GND or V_{CC}, $\overline{OE}$ = don't care				±100			±100	µA
I_{OZH}		V_{CC} = 3.6 V	V_O = 3 V, V_I = 0.8 V or 2 V			5			5	µA
I_{OZL}		V_{CC} = 3.6 V	V_O = 0.5 V, V_I = 0.8 V or 2 V			–5			–5	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		0.07	0.1		0.07	0.1	mA
			Outputs low		3.2	5.5		3.2	5	
			Outputs disabled		0.07	0.1		0.07	0.1	
ΔI_{CC}□		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.4			0.4	mA
C_i		V_{CC} = 3.3 V,	V_I = 3.3 V or 0		3.5			3.5		pF
C_o		V_{CC} = 3.3 V,	V_O = 3.3 V or 0		6			6		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
¶ An external driver must source at least I_{BHLO} to switch this node from low to high.
# An external driver must sink at least I_{BHHO} to switch this node from high to low.
‖ Current into an output in the high state when V_O > V_{CC}
☆ High-impedance state during power up or power down
□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			SN54ALVTH16373		SN74ALVTH16373		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		1.5		1.5		ns
t_{su}	Setup time, data before LE↓	Data high	1.1		1		ns
		Data low	1.6		1.5		
t_h	Hold time, data after LE↓	Data high	1		0.9		ns
		Data low	1.6		1.5		

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

			SN54ALVTH16373		SN74ALVTH16373		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		1.5		1.5		ns
t_{su}	Setup time, data before LE↓	Data high	1.5		1.4		ns
		Data low	1		0.9		
t_h	Hold time, data after LE↓	Data high	1		0.9		ns
		Data low	1.5		1.4		

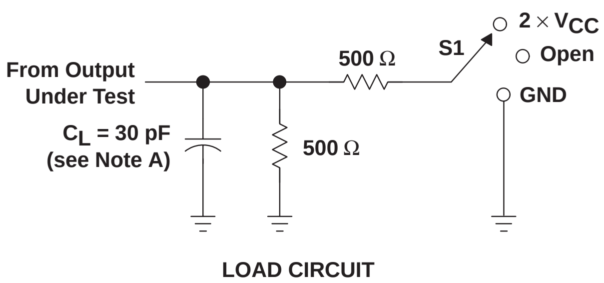
switching characteristics over recommended operating free-air temperature range, C_L = 30 pF, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16373		SN74ALVTH16373		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	3.4	1	3.3	ns
t_{PHL}			1	4.3	1	4.2	
t_{PLH}	LE	Q	1.4	3.9	1.5	3.8	ns
t_{PHL}			1.4	4.6	1.5	4.5	
t_{PZH}	$\overline{OE}$	Q	1.7	4.4	1.8	4.3	ns
t_{PZL}			1.4	4.1	1.5	4	
t_{PHZ}	$\overline{OE}$	Q	1.4	4.7	1.5	4.6	ns
t_{PLZ}			1	3.7	1	3.6	

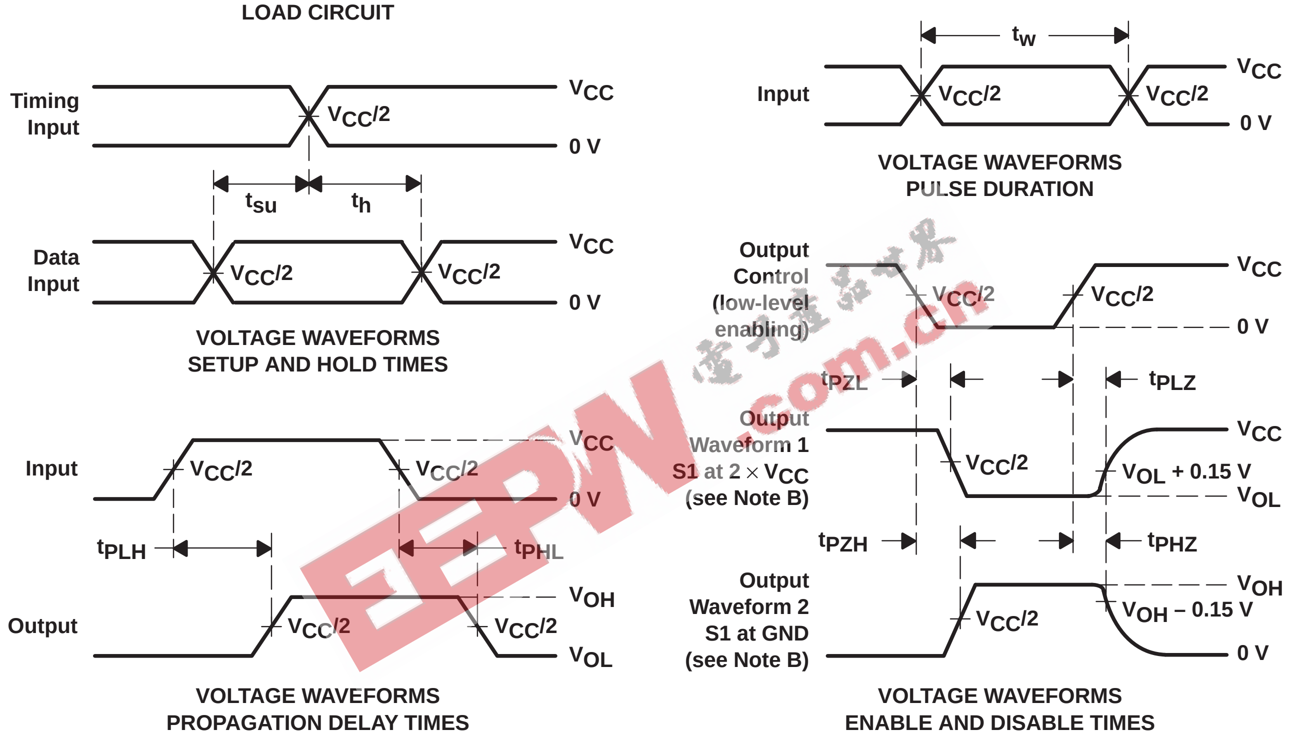
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16373		SN74ALVTH16373		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	3.2	1	3.1	ns
t_{PHL}			1	3.4	1	3.3	
t_{PLH}	LE	Q	1	3.4	1	3.3	ns
t_{PHL}			1	3.6	1	3.5	
t_{PZH}	$\overline{OE}$	Q	1.3	4.1	1.4	4	ns
t_{PZL}			1	3.5	1	3.4	
t_{PHZ}	$\overline{OE}$	Q	1.4	5	1.5	4.9	ns
t_{PLZ}			1.4	4.6	1.5	4.5	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V



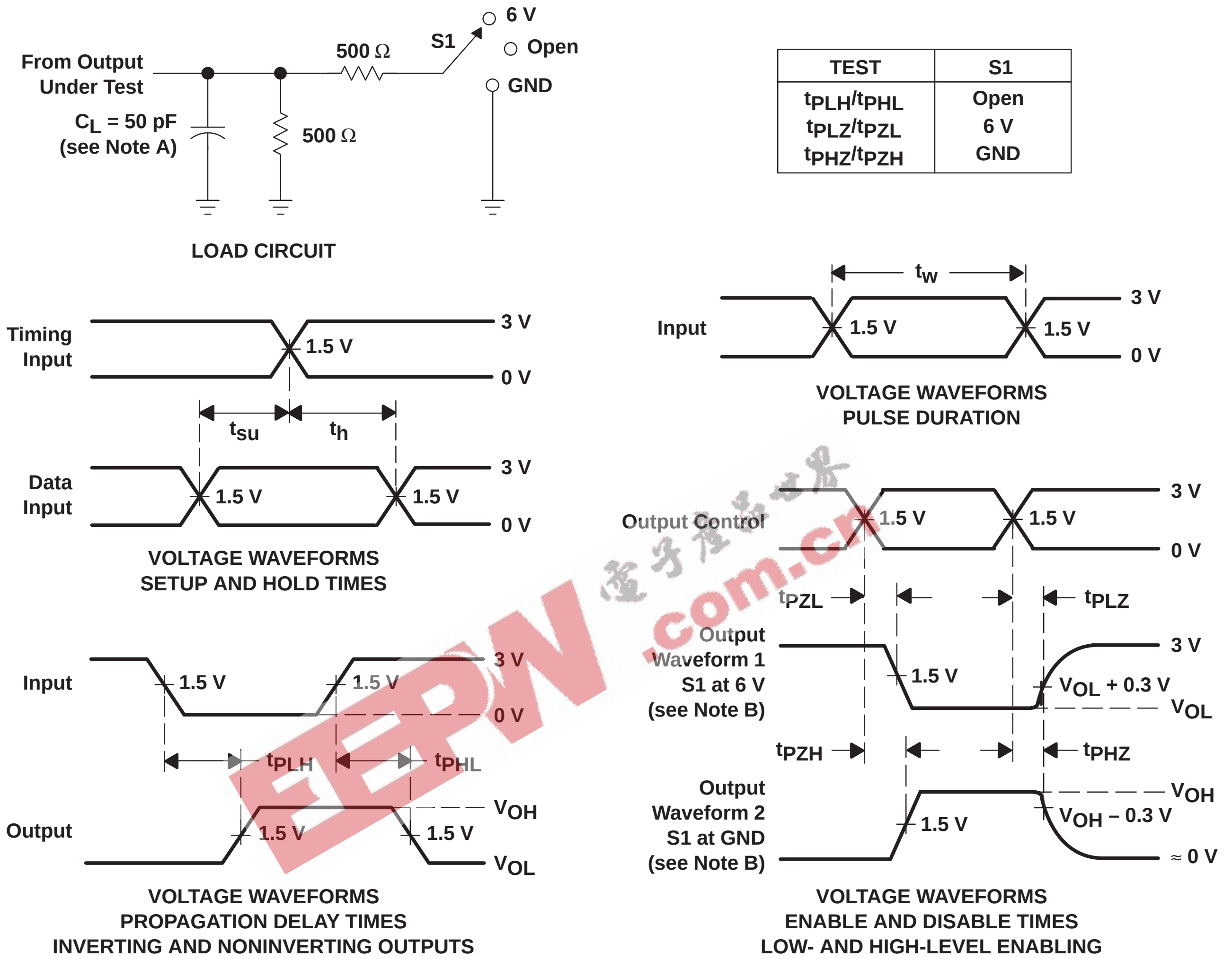
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3 V ± 0.3 V



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform22 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74ALVTH16373DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16373DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16373GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16373GRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16373VRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16373VRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16373ZQLR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74ALVTH16373DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16373DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16373GR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16373KR	NRND	BGA MI CROSTA R JUNI OR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74ALVTH16373VR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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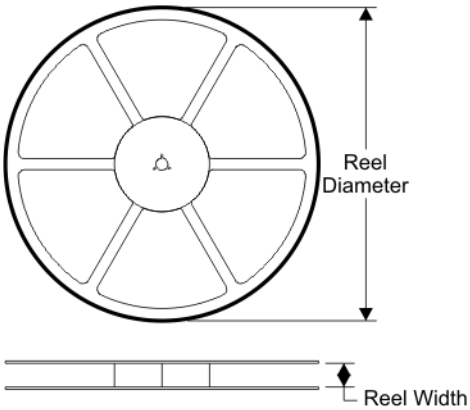
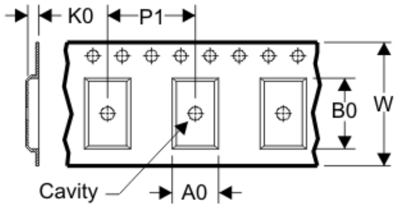
TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

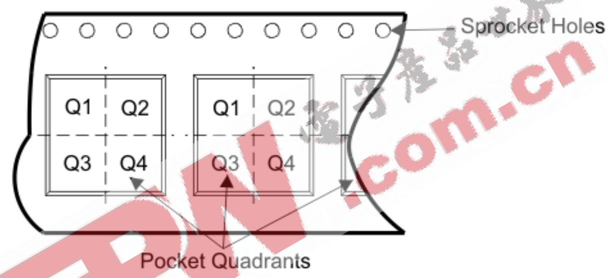


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

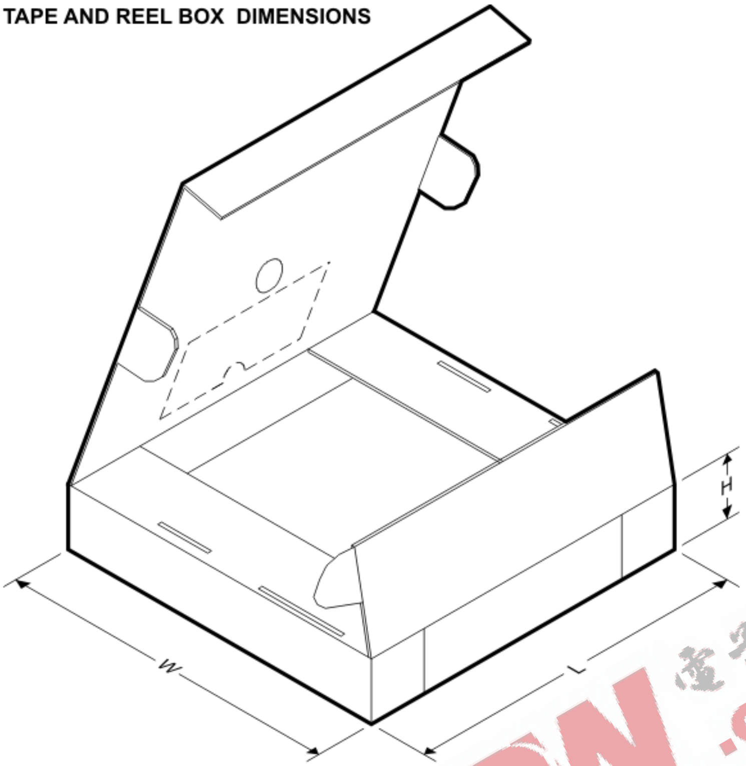
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ALVTH16373ZQLR	ZQL	56	SITE 32	330	16	4.8	7.3	1.45	8	16	Q1
SN74ALVTH16373DLR	DL	48	SITE 41	330	32	11.35	16.2	3.1	16	32	Q1
SN74ALVTH16373GR	DGG	48	SITE 41	330	24	8.6	15.8	1.8	12	24	Q1
SN74ALVTH16373KR	GQL	56	SITE 32	330	16	4.8	7.3	1.45	8	16	Q1
SN74ALVTH16373VR	DGV	48	SITE 41	330	24	6.8	10.1	1.6	12	24	Q1

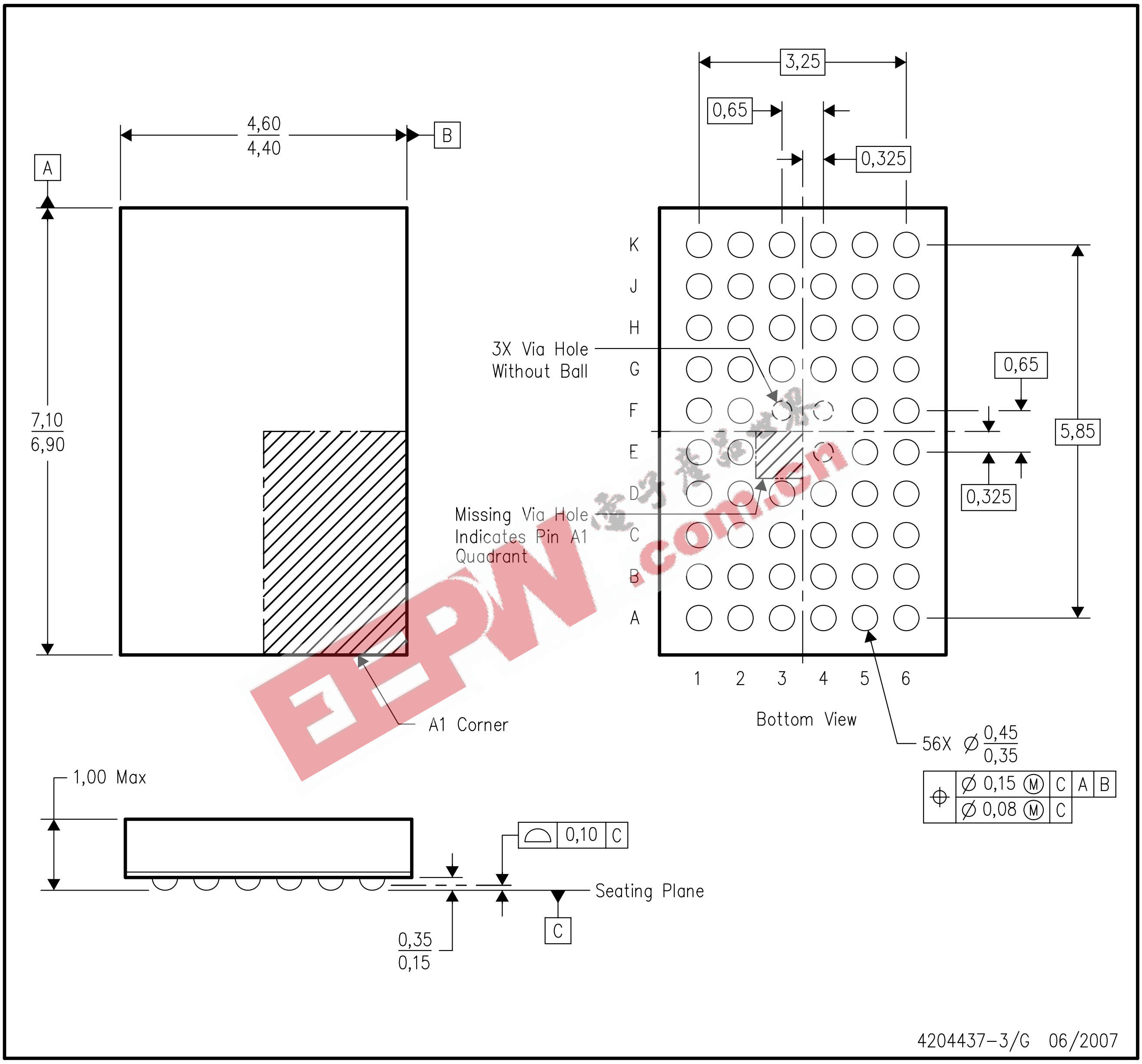
PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
74ALVTH16373ZQLR	ZQL	56	SITE 32	346.0	346.0	0.0
SN74ALVTH16373DLR	DL	48	SITE 41	346.0	346.0	0.0
SN74ALVTH16373GR	DGG	48	SITE 41	346.0	346.0	0.0
SN74ALVTH16373KR	GQL	56	SITE 32	346.0	346.0	0.0
SN74ALVTH16373VR	DGV	48	SITE 41	346.0	346.0	0.0

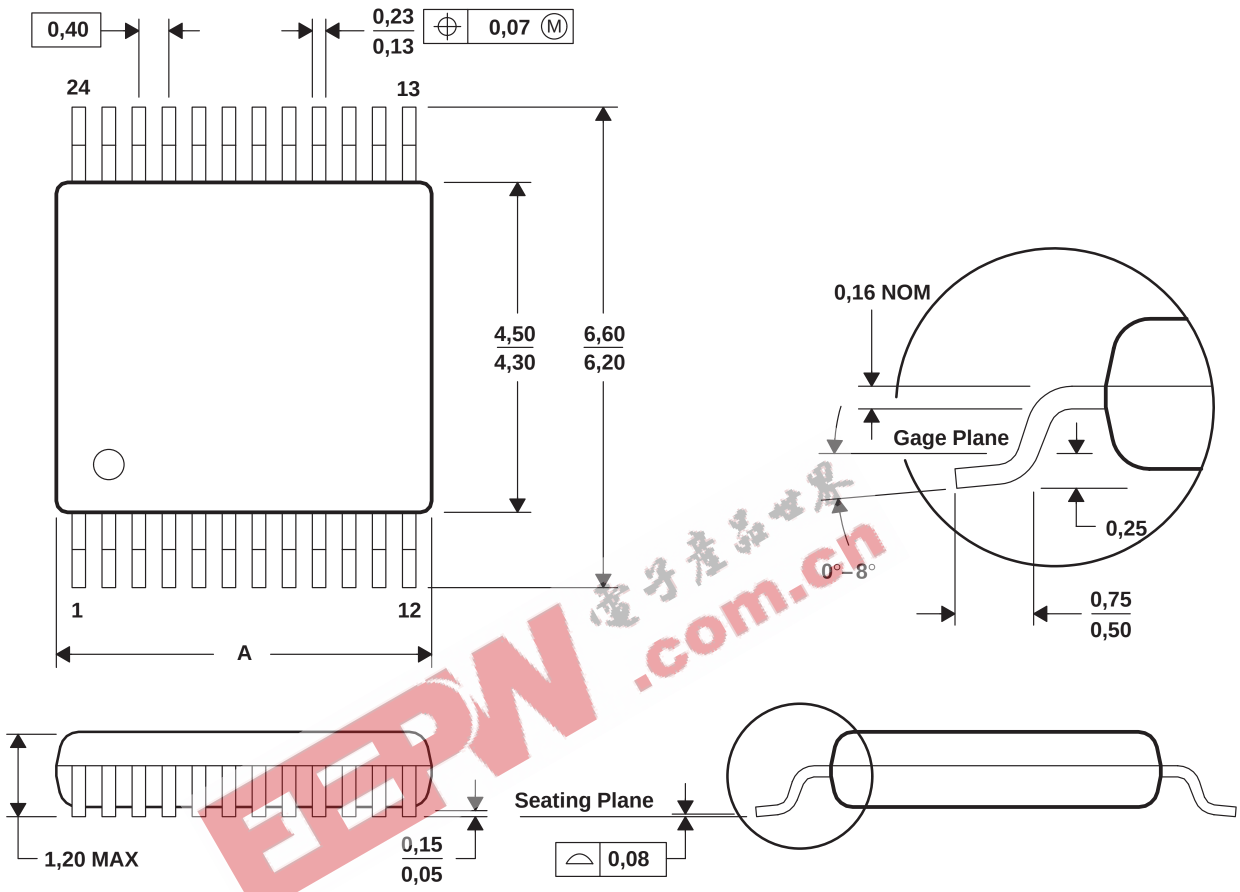
ZQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO–285 variation BA–2.
- D. This package is lead–free. Refer to the 56 GQL package (drawing 4200583) for tin–lead (SnPb).

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

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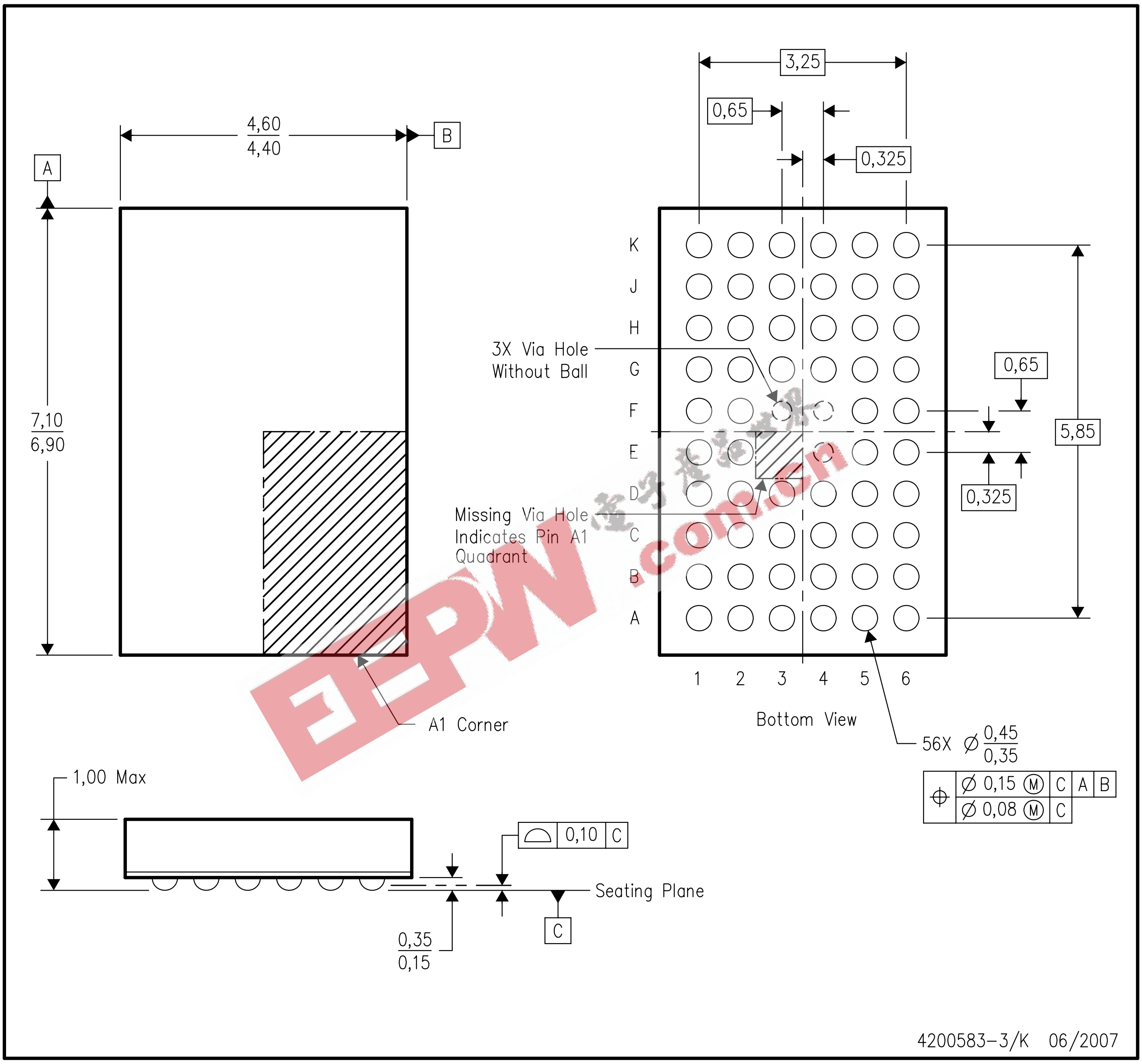
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

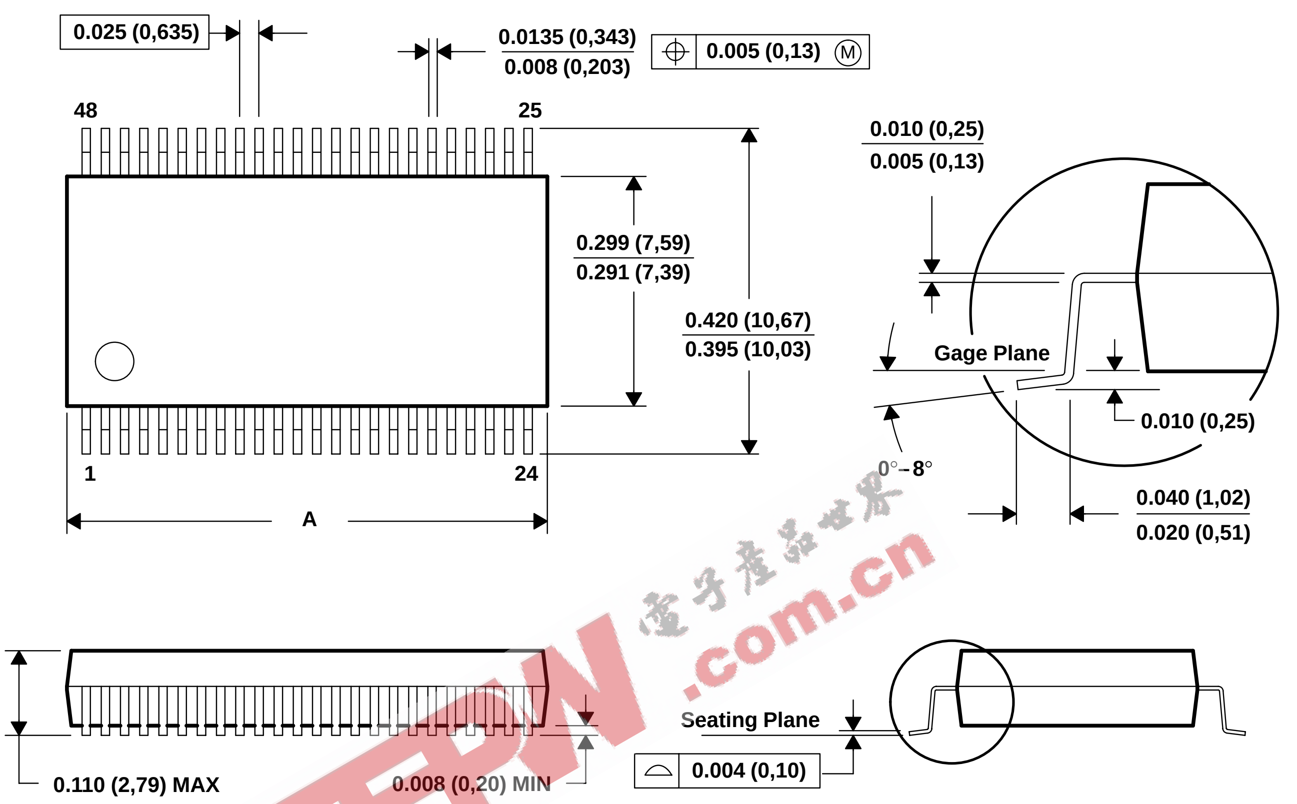
GQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–285 variation BA–2.
D. This package is tin–lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead–free.

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

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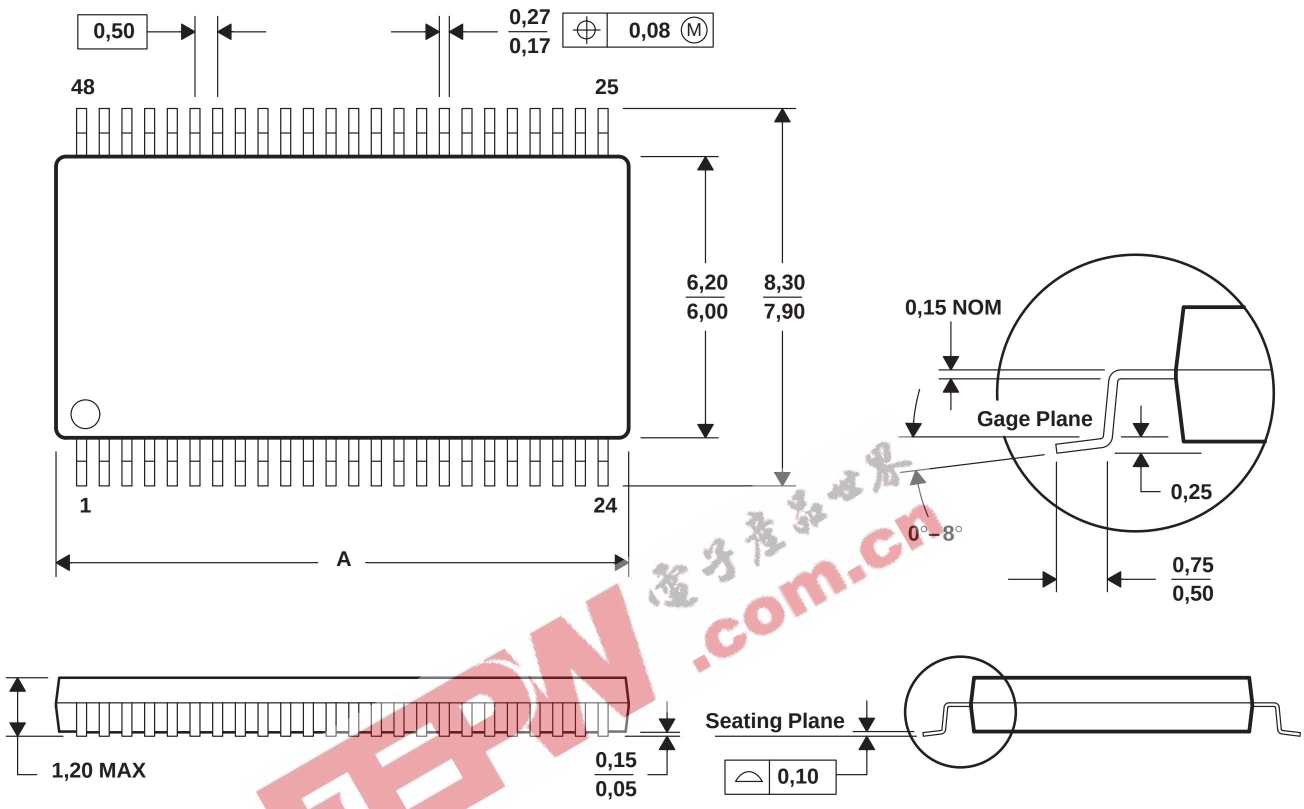
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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