

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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74HC/HCT158

Quad 2-input multiplexer; inverting

Product specification
File under Integrated Circuits, IC06

December 1990

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74HC/HCT158

FEATURES

- Inverting data path
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT158 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT158 are quad 2-input multiplexers which select 4 bits of data from two sources and are controlled by a common data select input (S). The four outputs present the selected data in the inverted form. The enable input (\bar{E}) is active LOW.

When \bar{E} is HIGH, all the outputs ($1\bar{Y}$ to $4\bar{Y}$) are forced HIGH regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the "158". The state of S determines the particular register from which the data comes. It can also be used as a function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "158" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations for the output are:

$$1\bar{Y} = \bar{E} \cdot (1I_1 \cdot S + 1I_0 \cdot \bar{S})$$

$$2\bar{Y} = \bar{E} \cdot (2I_1 \cdot S + 2I_0 \cdot \bar{S})$$

$$3\bar{Y} = \bar{E} \cdot (3I_1 \cdot S + 3I_0 \cdot \bar{S})$$

$$4\bar{Y} = \bar{E} \cdot (4I_1 \cdot S + 4I_0 \cdot \bar{S})$$

The "158" is identical to the "157" but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------------------------|--|---|----------------|----------------|----------------|
| | | | HC | HCT | |
| t _{PHL} / t _{PLH} | propagation delay nI ₀ , nI ₁ to nY \bar{E} to nY S to nY | C _L = 15 pF; V _{CC} = 5 V | 12 14 14 | 13 16 16 | ns ns ns |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| C _{PD} | power dissipation capacitance per multiplexer | notes 1 and 2 | 40 | 40 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

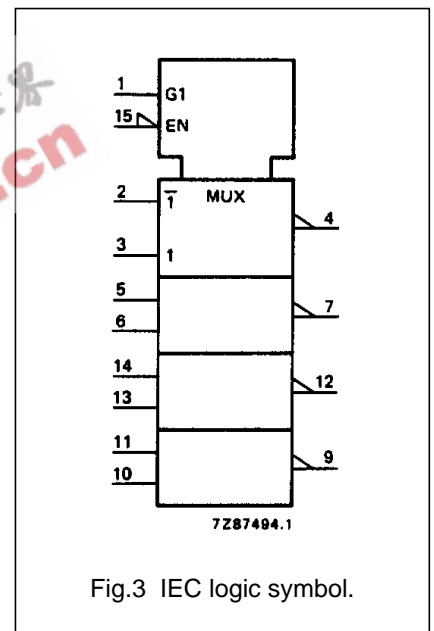
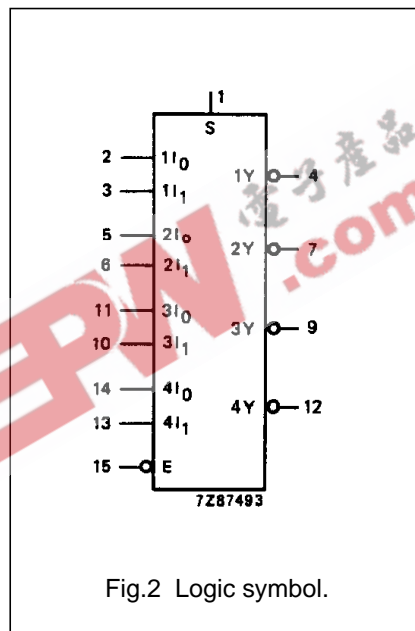
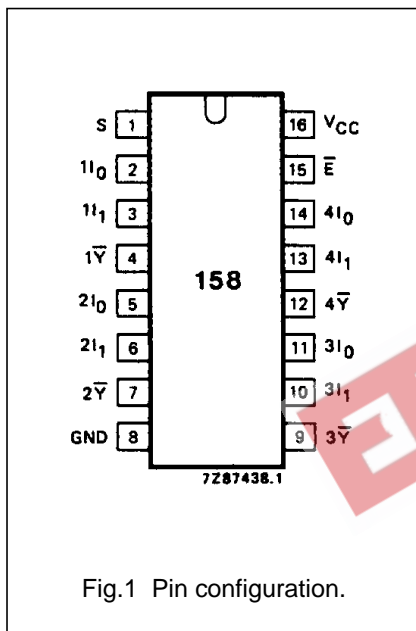
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|--------------|------------------------------------|---------------------------|
| 1 | S | common data select input |
| 2, 5, 11, 14 | 1I ₀ to 4I ₀ | data inputs from source 0 |
| 3, 6, 10, 13 | 1I ₁ to 4I ₁ | data inputs from source 1 |
| 4, 7, 9, 12 | 1Ȳ to 4Ȳ | multiplexer outputs |
| 8 | GND | ground (0 V) |
| 15 | \bar{E} | enable input (active LOW) |
| 16 | V _{CC} | positive supply voltage |



Quad 2-input multiplexer; inverting

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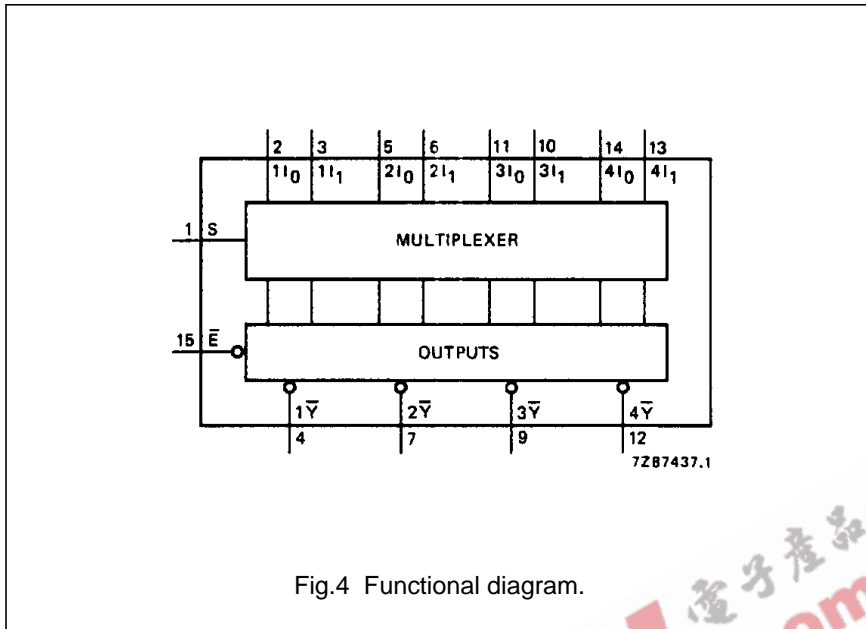


Fig.4 Functional diagram.

FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|-----------|---|--------|--------|------------|
| \bar{E} | S | nI_0 | nI_1 | $n\bar{Y}$ |
| H | X | X | X | H |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

Notes

- 1. H = HIGH voltage level
- L = LOW voltage level
- X = don't care

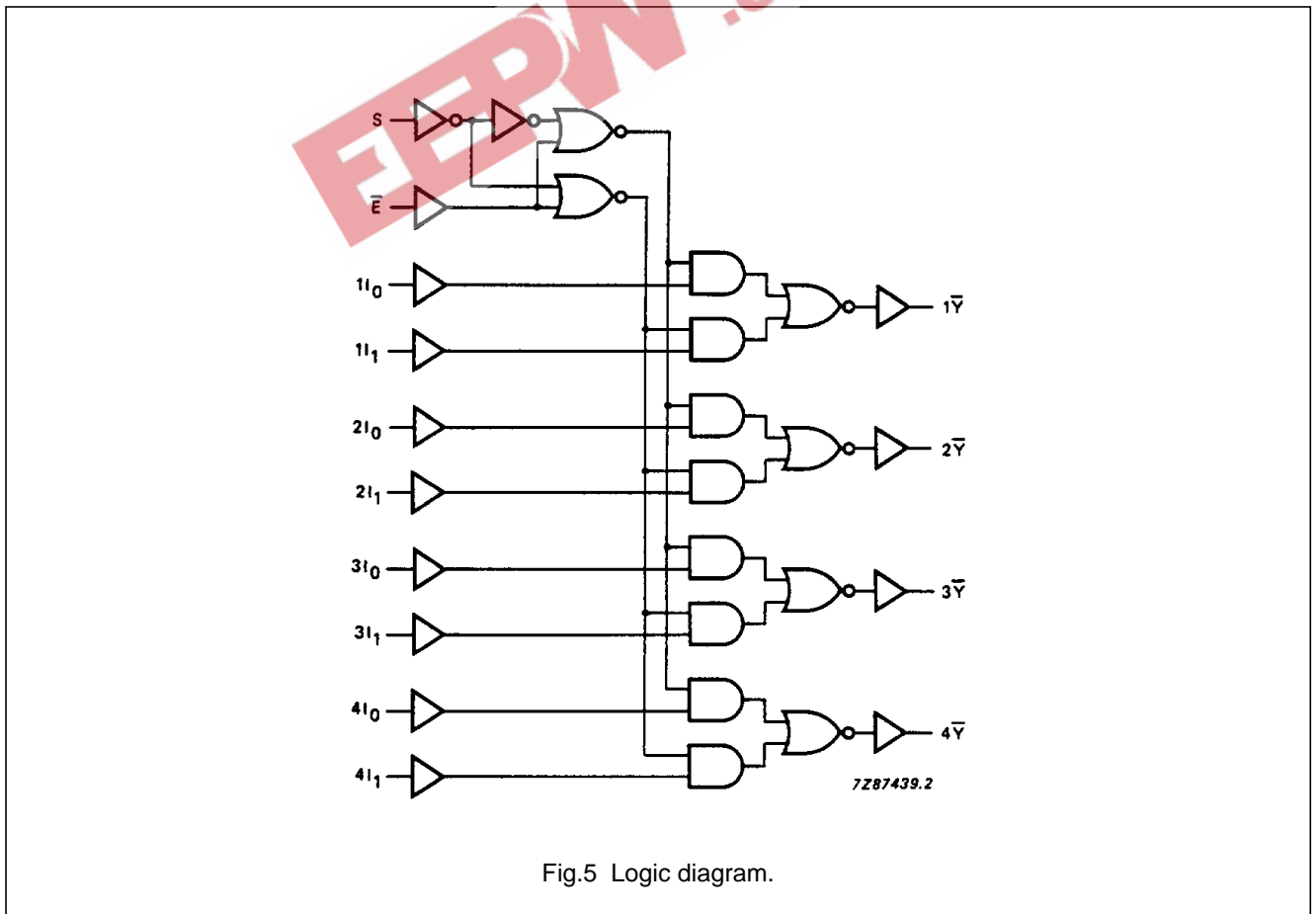


Fig.5 Logic diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|---|-----------------------|----------------|-----------------|------------|-----------------|-------------|-----------------|------------------------|-------------------|--------------|
| | | 74HC | | | | | | | V _{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay nI ₀ , nI ₁ to n \bar{Y} | | 41 15 12 | 125 25 21 | | 155 31 26 | | 190 38 32 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{PHL} / t _{PLH} | propagation delay \bar{E} to n \bar{Y} | | 47 17 14 | 145 29 25 | | 180 36 31 | | 220 44 38 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{PHL} / t _{PLH} | propagation delay S to n \bar{Y} | | 47 17 14 | 145 29 25 | | 180 36 31 | | 220 44 38 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{THL} / t _{TLH} | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | | 110 22 19 | ns | 2.0 4.5 6.0 | Figs 6 and 7 |

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|-----------------|-----------------------|
| nI ₀ | 0.40 |
| nI ₁ | 0.40 |
| S | 2.80 |
| \bar{E} | 0.60 |

AC CHARACTERISTICS FOR 74HCT

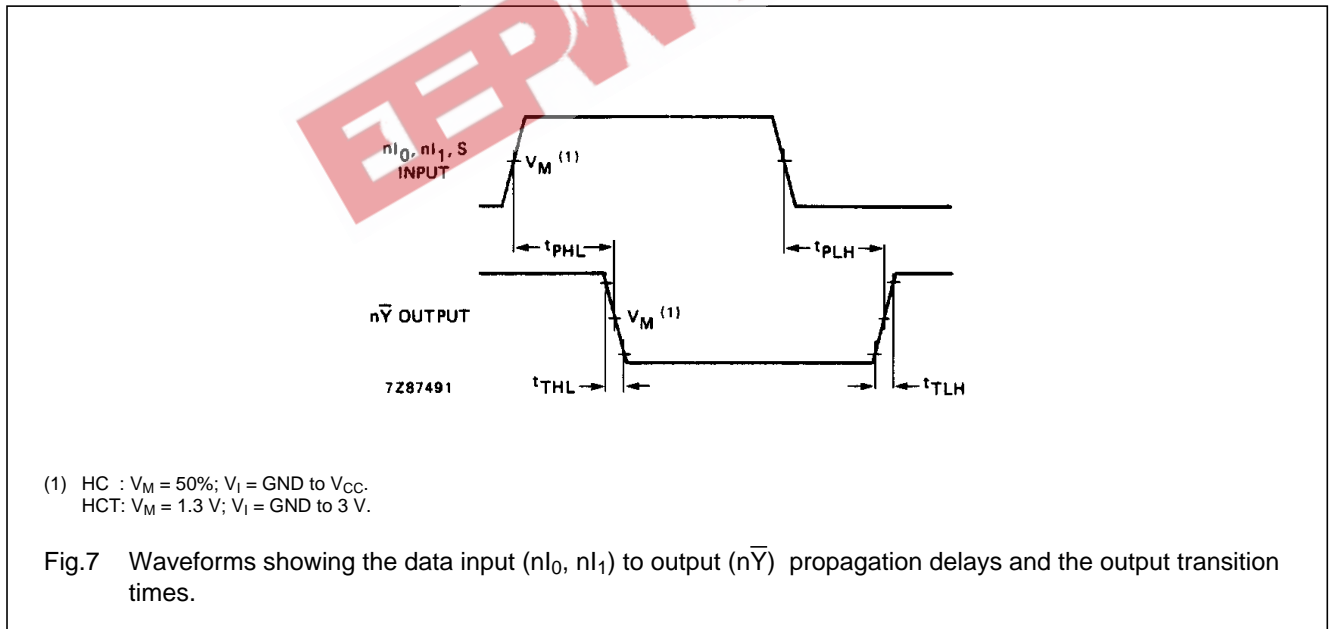
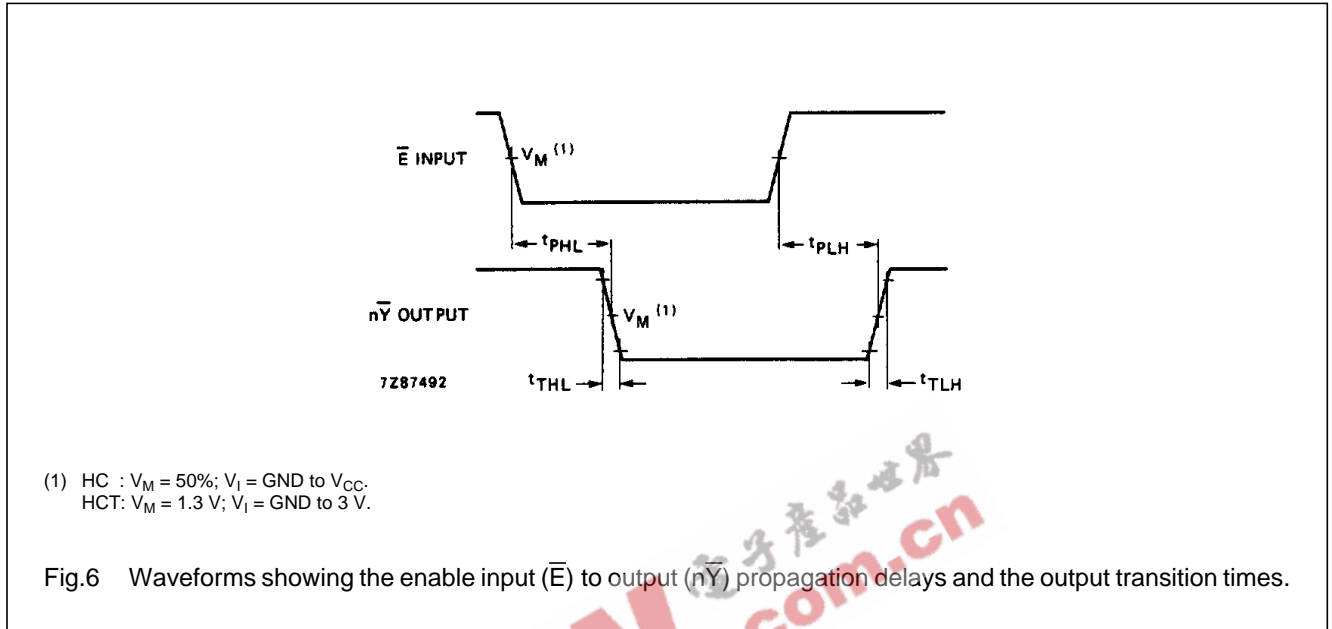
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|---|-----------------------|------|------|------------|------|-------------|------|------|------------------------|--------------|--|
| | | 74HCT | | | | | | | | V _{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| t _{PHL} / t _{PLH} | propagation delay nI ₀ , nI ₁ to n \bar{Y} | | 16 | 30 | | 38 | | 45 | ns | 4.5 | Fig.7 | |
| t _{PHL} / t _{PLH} | propagation delay \bar{E} to n \bar{Y} | | 19 | 35 | | 44 | | 53 | ns | 4.5 | Fig.6 | |
| t _{PHL} / t _{PLH} | propagation delay S to n \bar{Y} | | 19 | 35 | | 44 | | 53 | ns | 4.5 | Fig.7 | |
| t _{THL} / t _{TLH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Figs 6 and 7 | |

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".