

74LVC2G38

Dual 2-input NAND gate; open drain

Rev. 05 — 4 September 2007

Product data sheet

1. General description

The 74LVC2G38 provides a 2-input NAND function.

The outputs of the 74LVC2G38 devices are open drain and can be connected to other open-drain outputs to implement active-LOW, wired-OR or active-HIGH wired-AND functions.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM EIA/JESD22-A114E exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Open-drain outputs
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC2G38DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G38DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G38GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC2G38GM	-40 °C to +125 °C	XQFN8	plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-1

4. Marking

Table 2. Marking code

Type number	Marking code
74LVC2G38DP	Y38
74LVC2G38DC	Y38
74LVC2G38GT	Y38
74LVC2G38GM	Y38

5. Functional diagram

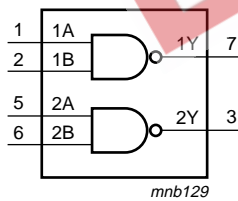


Fig 1. Logic symbol

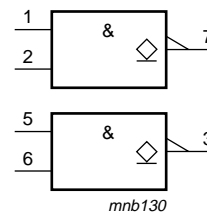


Fig 2. IEC logic symbol

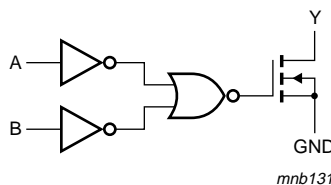
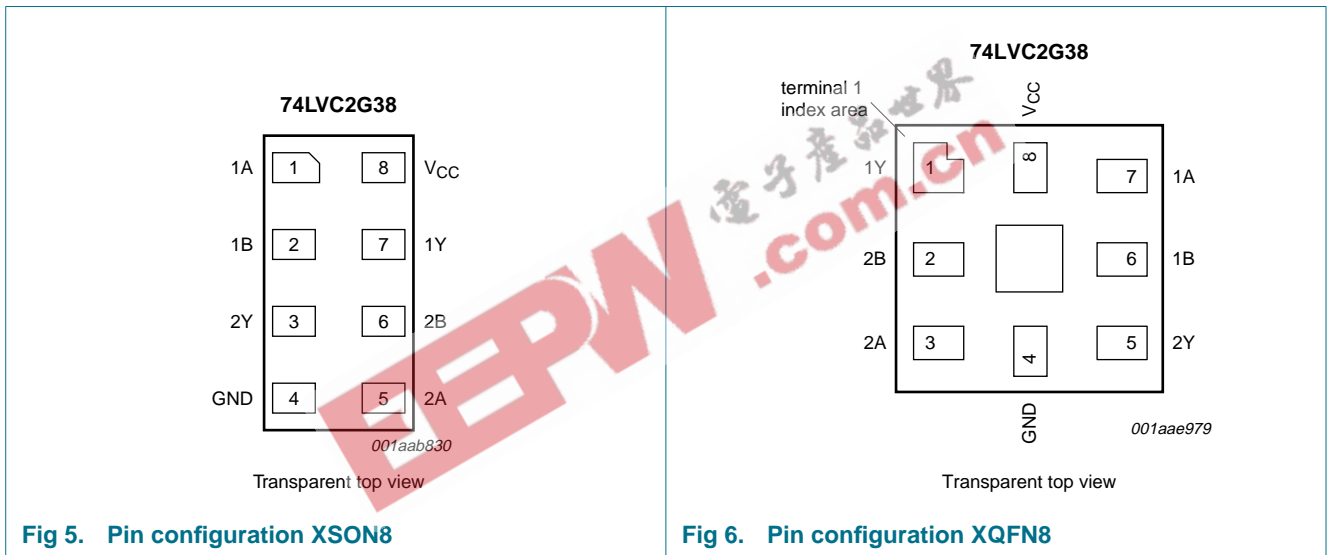
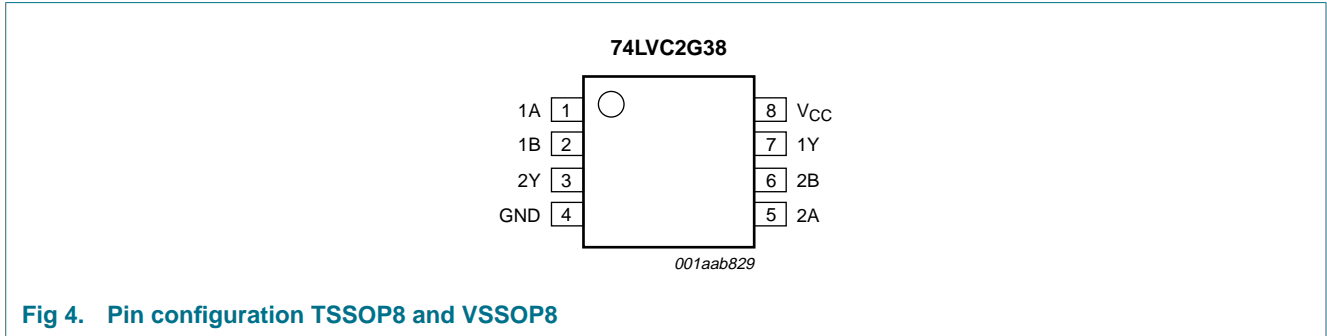


Fig 3. Functional diagram (one gate)

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin			Description
	TSSOP8, VSSOP8	XSON8	XQFN8	
1A	1	1	7	data input
1B	2	2	6	data input
2Y	3	3	5	data output
GND	4	4	4	ground (0 V)
2A	5	5	3	data input
2B	6	6	2	data input
1Y	7	7	1	data output
V _{CC}	8	8	8	supply voltage

7. Functional description

Table 4. Function table^[1]

Input		Output
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage		^[1] -0.5	+6.5	V
V_O	output voltage	Active mode	^{[1][2]} -0.5	+6.5	V
		Power-down mode	^{[1][2]} -0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	^[3] -	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

For XSON8 and XQFN8 packages: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	5.5	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	Active mode	0	-	V _{CC}	V
		disable mode	0	-	5.5	V
		Power-down mode	0	-	5.5	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V _{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C [1]						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	0.08	0.45	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	0.14	0.3	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	0.19	0.4	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	0.37	0.55	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	0.43	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±5	μA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	±0.1	±10	μA
I _{CC}	supply current	V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A	-	0.1	10	μA
ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	-	5	500	μA
C _i	input capacitance		-	2.5	-	pF

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.70	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.80	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	±20	μA
		V _I or V _O = 5.5 V; V _{CC} = 0 V	-	-	±20	μA
I _{CC}	supply current	V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A	-	-	40	μA
ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	-	-	5000	μA

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{PZL}	OFF-state to LOW propagation delay	nA, nB to nY; see Figure 7						
		V _{CC} = 1.65 V to 1.95 V	1.2	3.0	8.6	1.2	10.8	ns
		V _{CC} = 2.3 V to 2.7 V	0.7	1.8	4.8	0.7	6.0	ns
		V _{CC} = 2.7 V	0.7	2.5	4.4	0.7	5.5	ns
		V _{CC} = 3.0 V to 3.6 V	0.7	2.1	4.1	0.7	5.2	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.5	3.3	0.5	4.2	ns
t _{PLZ}	LOW to OFF-state propagation delay	nA, nB to nY; see Figure 7						
		V _{CC} = 1.65 V to 1.95 V	1.2	3.0	8.6	1.2	10.8	ns
		V _{CC} = 2.3 V to 2.7 V	0.7	1.8	4.8	0.7	6.0	ns
		V _{CC} = 2.7 V	0.7	2.5	4.4	0.7	5.5	ns
		V _{CC} = 3.0 V to 3.6 V	0.7	2.1	4.1	0.7	5.2	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.5	3.3	0.5	4.2	ns
C _{PD}	power dissipation capacitance	per gate; V _I = GND to V _{CC}	5	-	-	-	-	pF

[1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

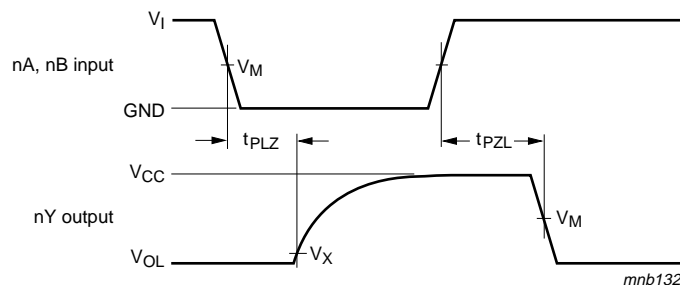
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms

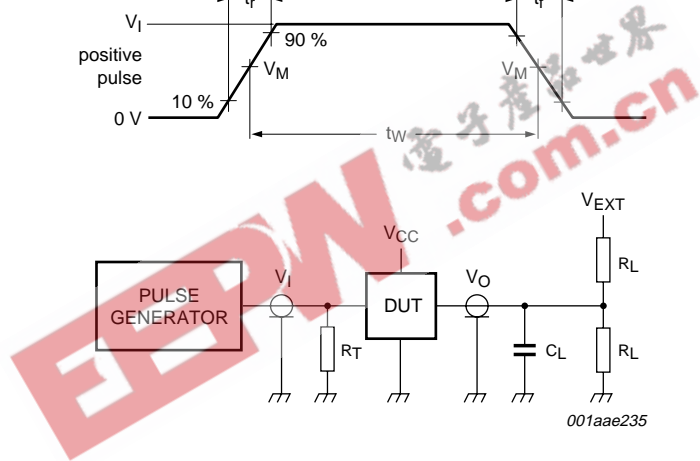
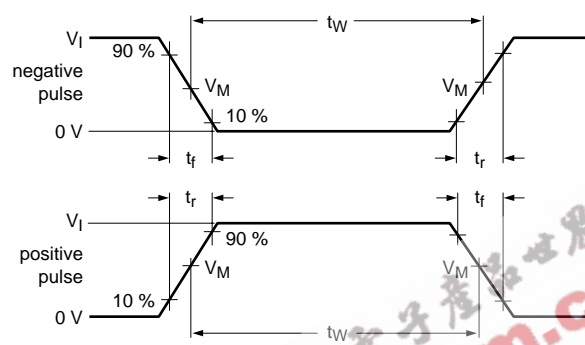


Measurement points are given in [Table 9](#)

Fig 7. Inputs nA and nB to output nY propagation delay times

Table 9. Measurement points

Supply voltage	Input	Output	
V_{CC}	V_M	V_X	V_M
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	1.5 V
3.0 V to 3.6 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$0.5 \times V_{CC}$



Test data is given in [Table 10](#)

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig 8. Load circuitry for switching times

Table 10. Test data

Supply voltage	Input	Load	V_{EXT}
V_{CC}	V_I , t_r, t_f	C_L , R_L	t_{PLZ}, t_{PZL}
1.65 V to 1.95 V	V_{CC} , $\leq 2.0 \text{ ns}$	30 pF, 1 k Ω	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC} , $\leq 2.0 \text{ ns}$	30 pF, 500 Ω	$2 \times V_{CC}$
2.7 V	2.7 V, $\leq 2.5 \text{ ns}$	50 pF, 500 Ω	6 V
3.0 V to 3.6 V	2.7 V, $\leq 2.5 \text{ ns}$	50 pF, 500 Ω	6 V
4.5 V to 5.5 V	V_{CC} , $\leq 2.5 \text{ ns}$	50 pF, 500 Ω	$2 \times V_{CC}$

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

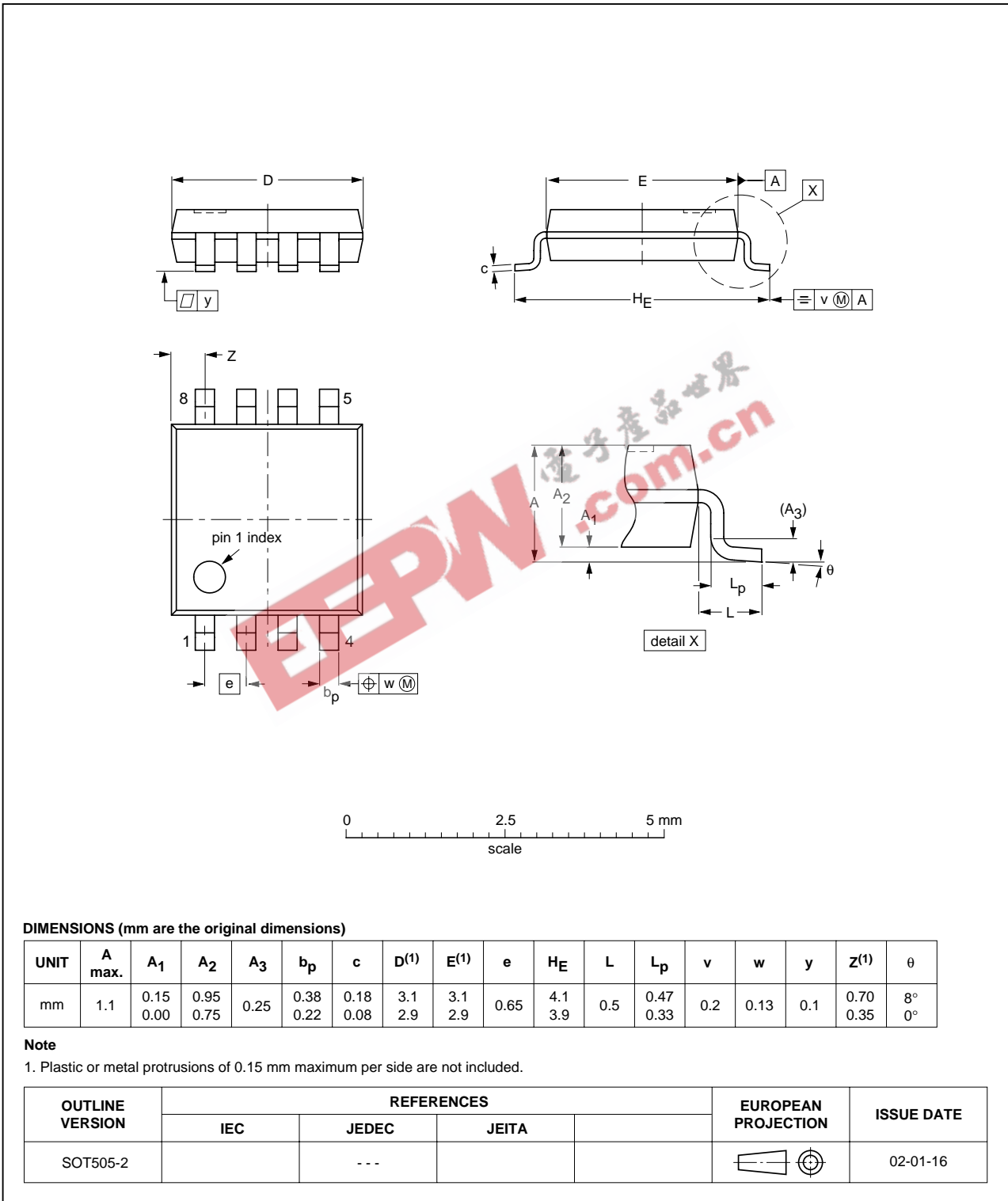


Fig 9. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

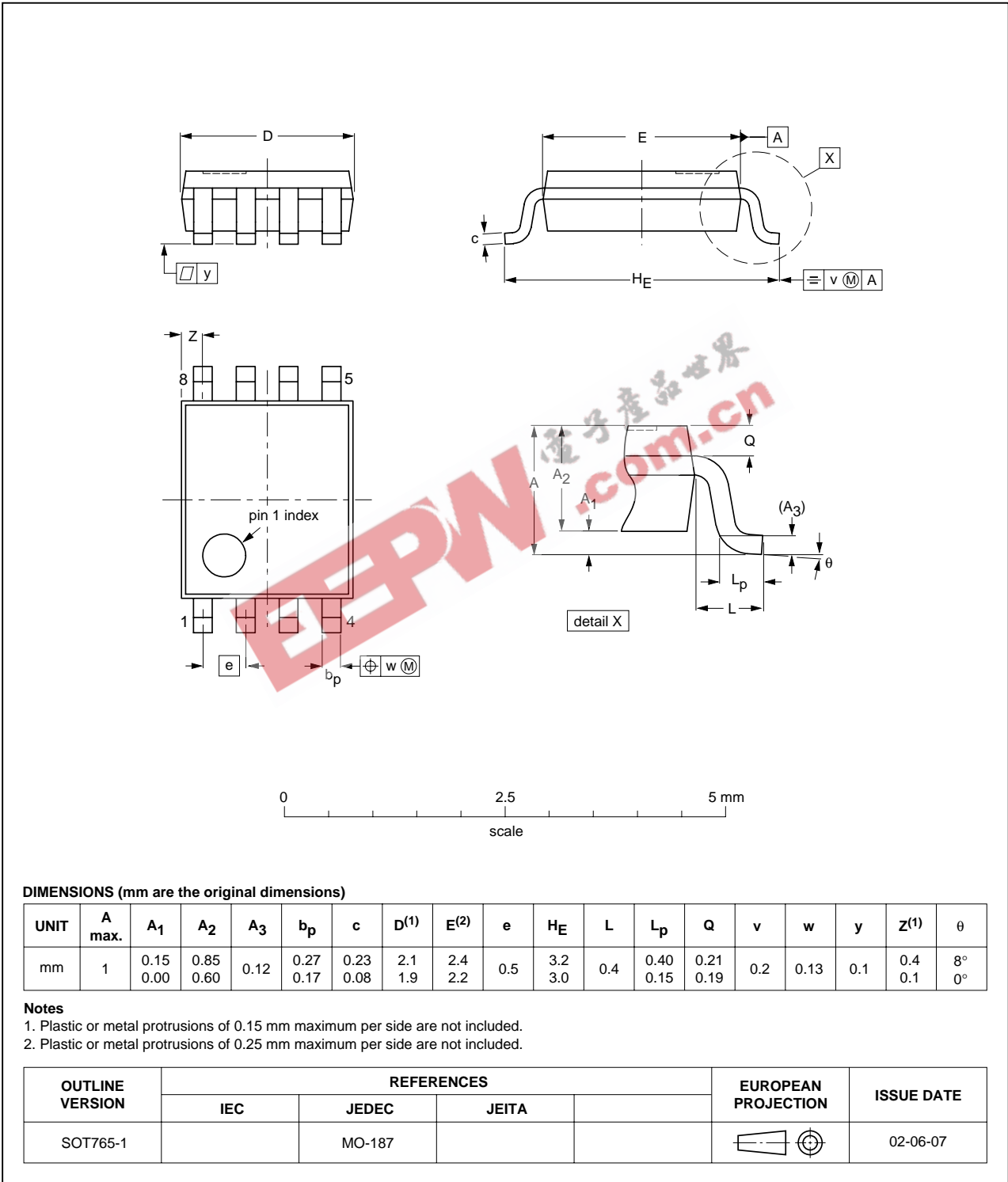


Fig 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

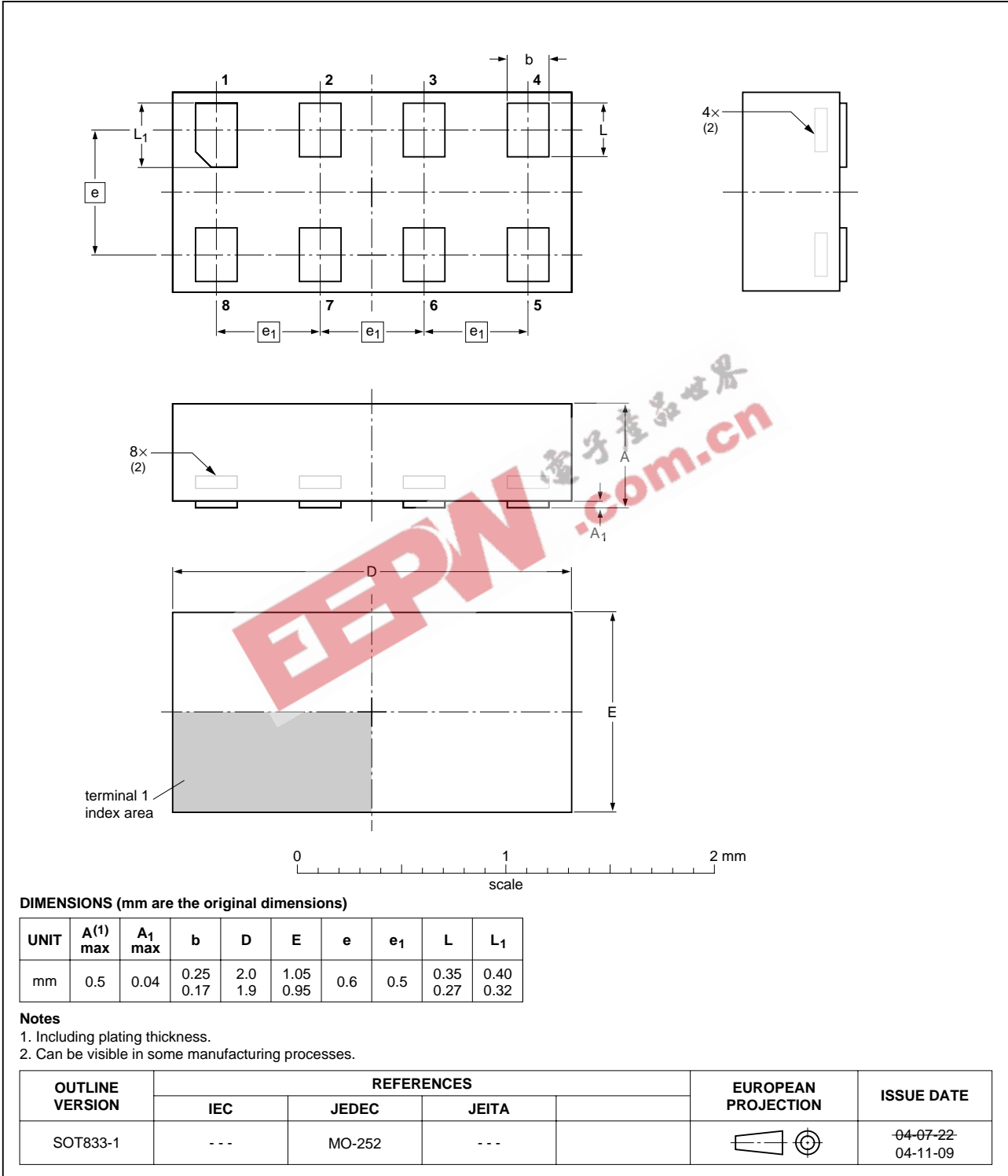


Fig 11. Package outline SOT833-1 (XSON8)

XQFN8: plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm

SOT902-1

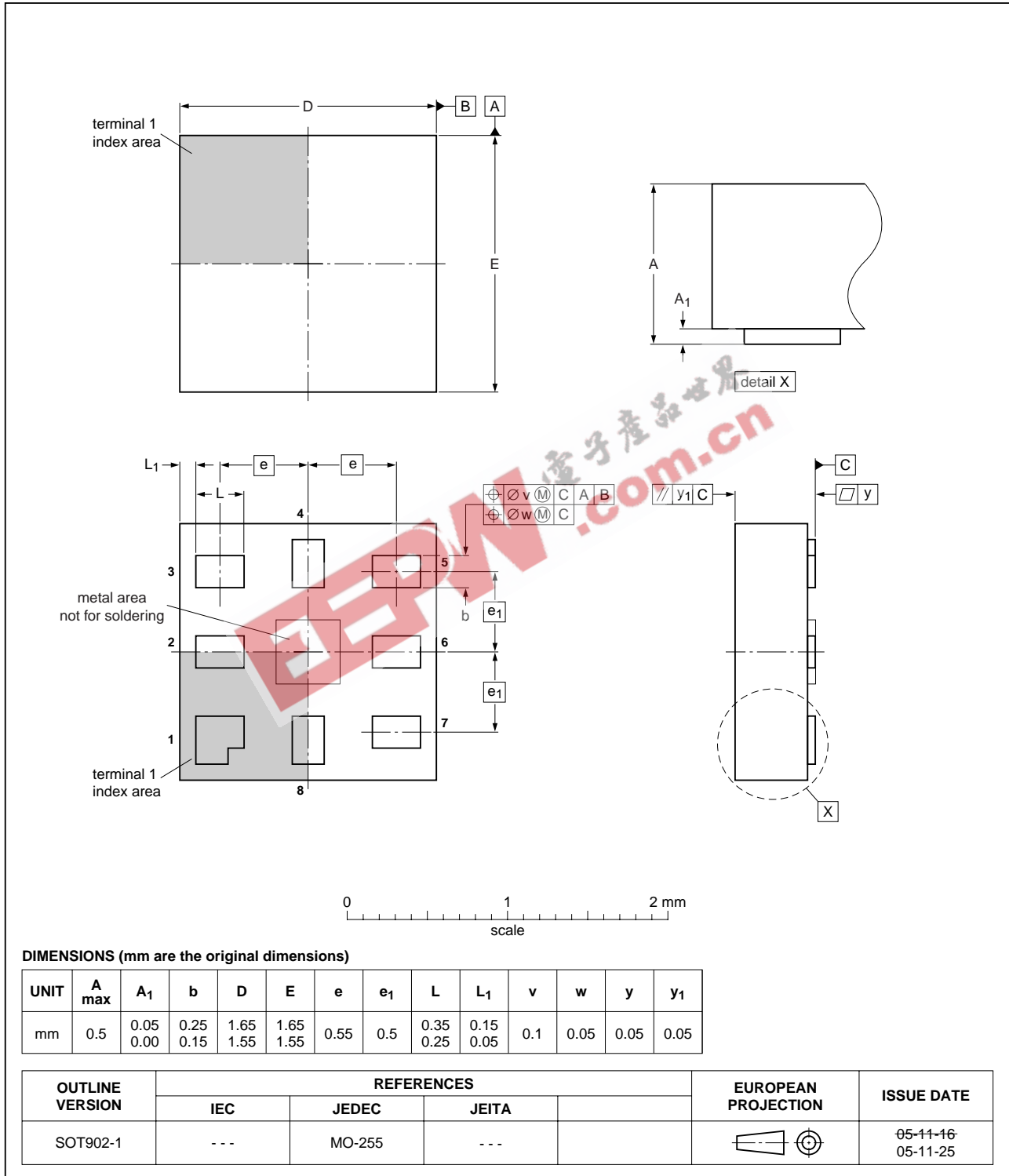


Fig 12. Package outline SOT902-1 (XQFN8)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G38_5	20070904	Product data sheet	-	74LVC2G38_4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. In Section 10 "Static characteristics", changed conditions for input leakage and supply current. 			
74LVC2G38_4	20060516	Product data sheet	-	74LVC2G38_3
74LVC2G38_3	20050201	Product specification	-	74LVC2G38_2
74LVC2G38_2	20041018	Product specification	-	74LVC2G38_1
74LVC2G38_1	20031027	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: salesaddresses@nxp.com

18. Contents

1 General description 1

2 Features 1

3 Ordering information 2

4 Marking 2

5 Functional diagram 2

6 Pinning information 3

6.1 Pinning 3

6.2 Pin description 3

7 Functional description 4

8 Limiting values 4

9 Recommended operating conditions 5

10 Static characteristics 5

11 Dynamic characteristics 7

12 Waveforms 7

13 Package outline 9

14 Abbreviations 13

15 Revision history 13

16 Legal information 14

16.1 Data sheet status 14

16.2 Definitions 14

16.3 Disclaimers 14

16.4 Trademarks 14

17 Contact information 14

18 Contents 15



Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2007. All rights reserved.

For more information, please visit: <http://www.nxp.com>
 For sales office addresses, please send an email to: salesaddresses@nxp.com
 Date of release: 4 September 2007
 Document identifier: 74LVC2G38_5