

74VHC00 Quad 2-Input NAND Gate

General Description

The VHC00 is an advanced high-speed CMOS 2-Input NAND Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages, including buffer output, which provide high noise immunity and stable output. An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: $t_{PD} = 3.7\text{ns}$ (typ) at $T_A = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Power down protection is provided on all inputs
- Low noise: $V_{OLP} = 0.8\text{V}$ (max)
- Low power dissipation: $I_{CC} = 2\ \mu\text{A}$ (max) at $T_A = 25^\circ\text{C}$
- Pin and function compatible with 74HC00

Ordering Code:

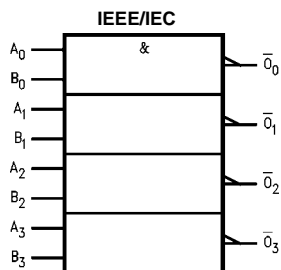
| Order Number | Package Number | Package Description |
|----------------------------|----------------|--|
| 74VHC00M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74VHC00MX_NL | M14A | Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74VHC00SJ | M14D | Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74VHC00MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74VHC00MTCX_NL (Note 1) | MTC14 | Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74VHC00N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

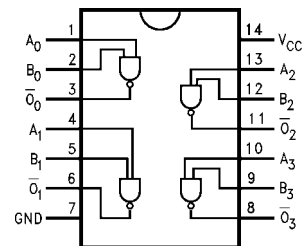
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Logic Symbol



Connection Diagram



Truth Table

| A | B | \bar{O} |
|---|---|-----------|
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

Pin Descriptions

| Pin Names | Description |
|-------------|-------------|
| A_n, B_n | Inputs |
| \bar{O}_n | Outputs |

| Absolute Maximum Ratings (Note 2) | | Recommended Operating Conditions (Note 3) | |
|---|--------------------------|---|---|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V | Supply Voltage (V_{CC}) | 2.0V to +5.5V |
| DC Input Voltage (V_{IN}) | -0.5V to +7.0V | Input Voltage (V_{IN}) | 0V to +5.5V |
| DC Output Voltage (V_{OUT}) | -0.5V to $V_{CC} + 0.5V$ | Output Voltage (V_{OUT}) | 0V to V_{CC} |
| Input Diode Current (I_{IK}) | -20 mA | Operating Temperature (T_{OPR}) | -40°C to +85°C |
| Output Diode Current (I_{OK}) | ±20 mA | Input Rise and Fall Time (t_r, t_f) | $V_{CC} = 3.3V \pm 0.3V$ 0 ns/V ~ 100 ns/V $V_{CC} = 5.0V \pm 0.5V$ 0 ns/V ~ 20 ns/V |
| DC Output Current (I_{OUT}) | ±25 mA | | |
| DC V_{CC} /GND Current (I_{CC}) | ±50 mA | | |
| Storage Temperature (T_{STG}) | -65°C to +150°C | | |
| Lead Temperature (T_L) (Soldering, 10 seconds) | 260°C | | |

Note 2: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ\text{C}$ | | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | Units | Conditions | |
|----------|------------------------------|------------------|--------------------------|-----|----------------------|---|------|-------|--|---|
| | | | Min | Typ | Max | Min | Max | | | |
| V_{IH} | HIGH Level Input Voltage | 2.0 3.0 – 5.5 | 1.50 | | | 1.50 $0.7 V_{CC}$ | | V | | |
| V_{IL} | LOW Level Input Voltage | 2.0 3.0 – 5.5 | | | 0.50 $0.3 V_{CC}$ | 0.50 $0.3 V_{CC}$ | | V | | |
| V_{OH} | HIGH Level Output Voltage | 2.0 | 1.9 | 2.0 | 1.9 | | | V | $V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50 \mu\text{A}$ | |
| | | 3.0 | 2.9 | 3.0 | 2.9 | | | | | |
| | | 4.5 | 4.4 | 4.5 | 4.4 | | | | | |
| | | 3.0 | 2.53 | | 2.48 | | | V | $I_{OH} = -4\text{mA}$ $I_{OH} = -8\text{mA}$ | |
| V_{OL} | LOW Level Output Voltage | 2.0 | | 0.0 | 0.1 | | 0.1 | | V | $V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50 \mu\text{A}$ |
| | | 3.0 | | 0.0 | 0.1 | | 0.1 | | | |
| | | 4.5 | | 0.0 | 0.1 | | 0.1 | | | |
| | | 3.0 | | | 0.36 | | 0.44 | | V | $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$ |
| | | 4.5 | | | 0.36 | | 0.44 | | | |
| I_{IN} | Input Leakage Current | 0 – 5.5 | | | ±0.1 | | ±1.0 | μA | $V_{IN} = 5.5V$ or GND | |
| I_{CC} | Quiescent Supply Current | 5.5 | | | 2.0 | | 20.0 | μA | $V_{IN} = V_{CC}$ or GND | |

Noise Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ\text{C}$ | | Units | Conditions |
|-----------------------|---|-----------------|--------------------------|-------|-------|-----------------------|
| | | | Typ | Limit | | |
| V_{OLP} (Note 4) | Quiet Output Maximum Dynamic V_{OL} | 5.0 | 0.3 | 0.8 | V | $C_L = 50 \text{ pF}$ |
| V_{OLV} (Note 4) | Quiet Output Minimum Dynamic V_{OL} | 5.0 | -0.3 | -0.8 | V | $C_L = 50 \text{ pF}$ |
| V_{IHD} (Note 4) | Minimum HIGH Level Dynamic Input Voltage | 5.0 | | 3.5 | V | $C_L = 50 \text{ pF}$ |
| V_{ILD} (Note 4) | Maximum LOW Level Dynamic Input Voltage | 5.0 | | 1.5 | V | $C_L = 50 \text{ pF}$ |

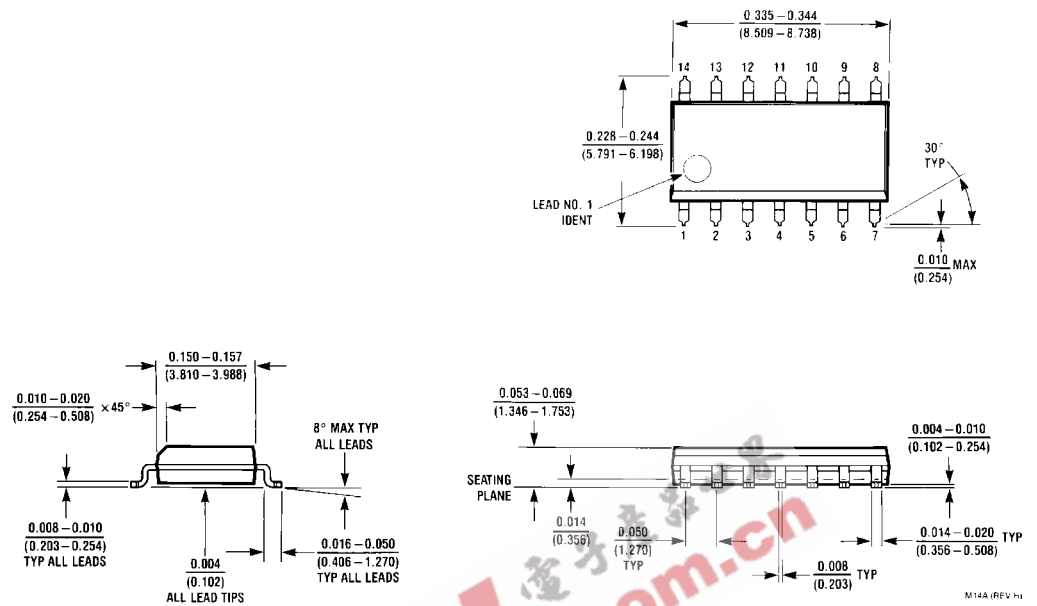
Note 4: Parameter guaranteed by design

| AC Electrical Characteristics | | | | | | | | | |
|-------------------------------|----------------------------------|------------------------|-----------------------|------|-----|---------------------------------|-----|------------------------|------------|
| Symbol | Parameter | V _{CC} (V) | T _A = 25°C | | | T _A = -40°C to +85°C | | Units | Conditions |
| | | | Min | Typ | Max | Min | Max | | |
| t _{PLH} | Propagation Delay | 3.3 ± 0.3 | 5.5 | 7.9 | 1.0 | 9.5 | ns | C _L = 15 pF | |
| t _{PHL} | | | 8.0 | 11.4 | 1.0 | 13.0 | | C _L = 50 pF | |
| | | 5.0 ± 0.5 | 3.7 | 5.5 | 1.0 | 6.5 | ns | C _L = 15 pF | |
| | | | 5.2 | 7.5 | 1.0 | 8.5 | | C _L = 50 pF | |
| C _{IN} | Input Capacitance | | 4 | 10 | | 10 | pF | V _{CC} = Open | |
| C _{PD} | Power Dissipation Capacitance | | 19 | | | | pF | (Note 5) | |

Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/4 (per gate).

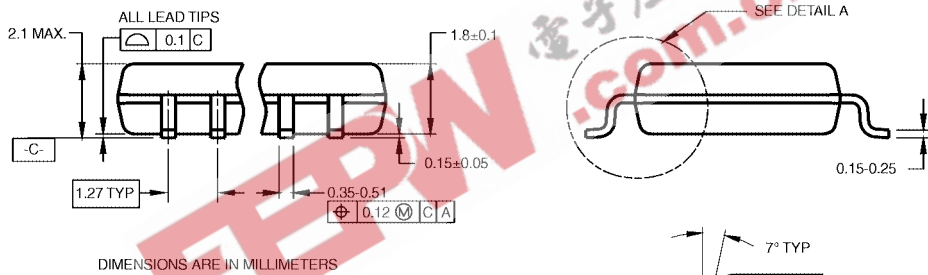
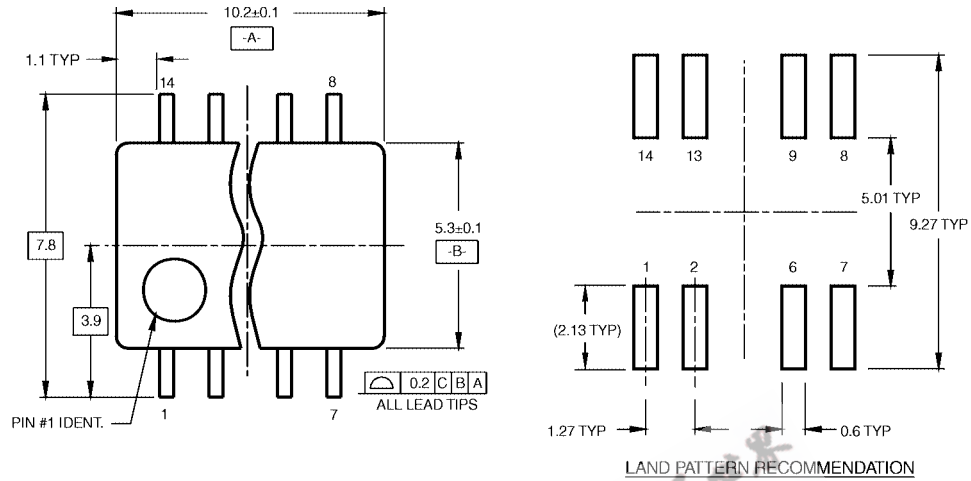
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Physical Dimensions inches (millimeters) unless otherwise noted



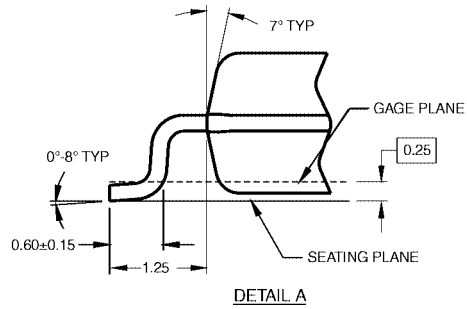
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



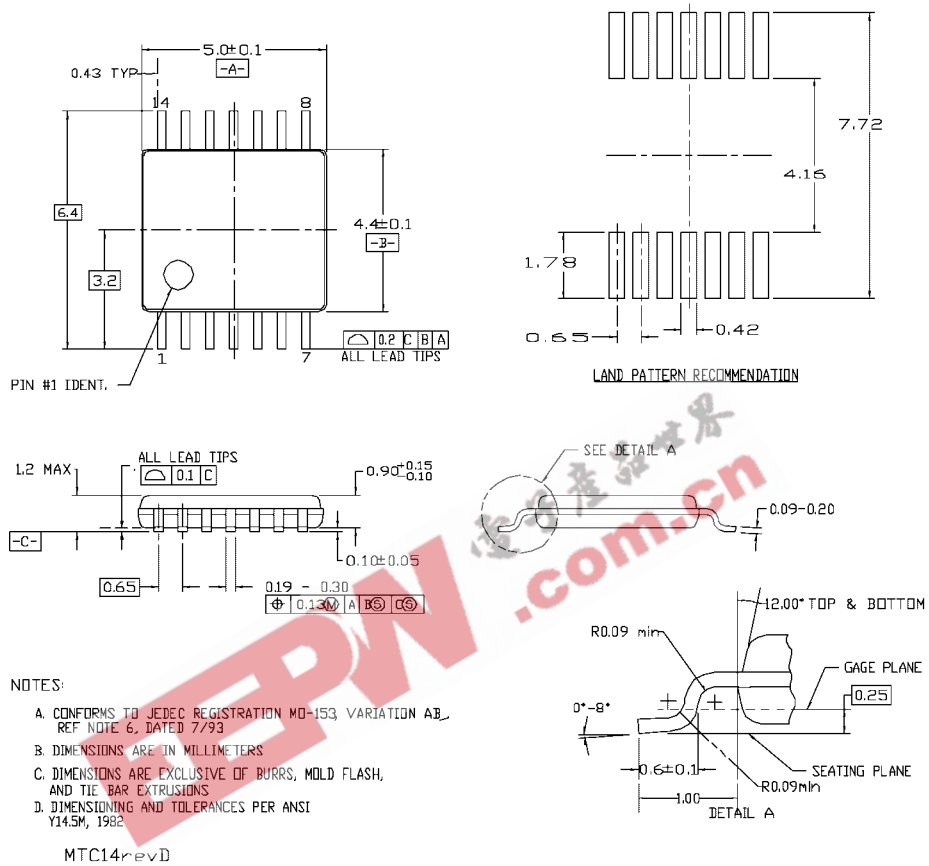
- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



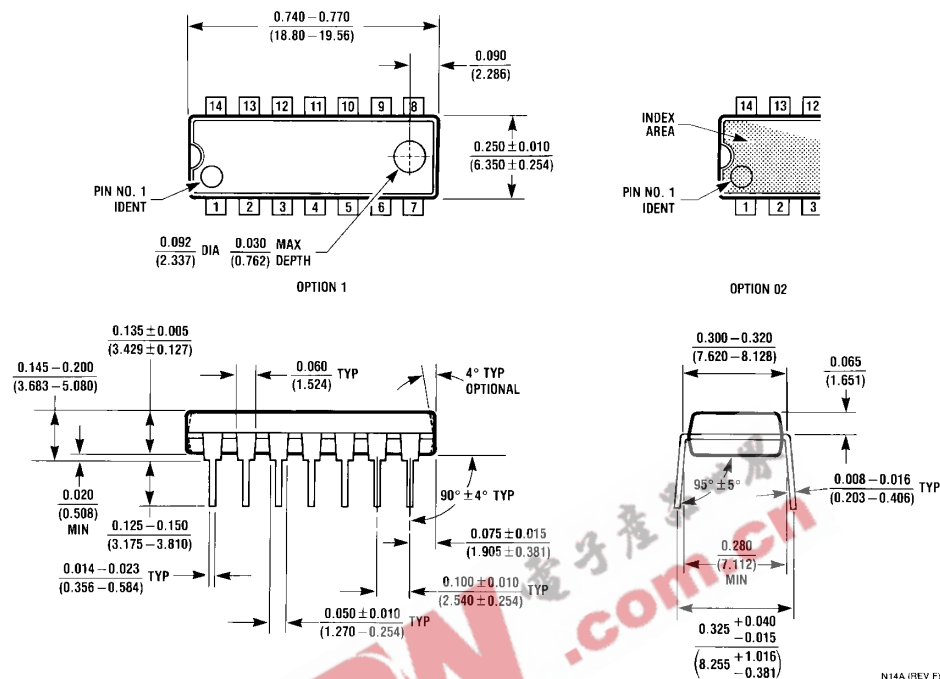
**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A**

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