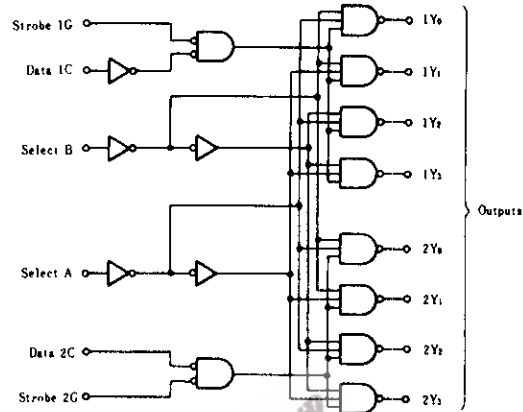


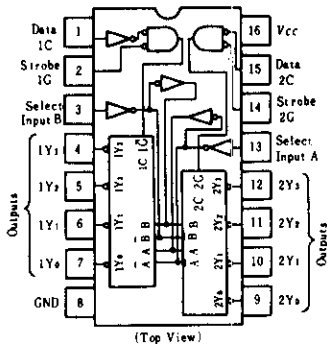
HD74LS156 • Dual 2-line-to-4-line Decoders/Demultiplexers (with open collector outputs)

This circuit features dual 1-line-to-4-line demultiplexer with individual strobes and common binary-address inputs. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating.

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
High level output voltage	V_{OH}	—	—	5.5	V
Low level output current	I_{OL}	—	—	8	mA

■ FUNCTION TABLE

● 2-to-4-line Decoder/1-to-4-line Demultiplexer

Inputs				Outputs				Inputs				Outputs			
SELECT	STROBE	DATA		1Y0	1Y1	1Y2	1Y3	SELECT	STROBE	DATA		2Y0	2Y1	2Y2	2Y3
B	A	1G	1C					B	A	2G	2C				
X	X	H	X	H	H	H	H	X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H	L	L	L	L	L	H	H	H
L	H	L	H	H	L	H	H	L	H	L	L	H	L	H	H
H	L	L	H	H	H	L	H	H	L	L	L	H	H	L	H
H	H	L	H	H	H	H	L	H	H	L	L	H	H	H	L
X	X	X	L	H	H	H	H	X	X	X	H	H	H	H	H

● 3-to-8-line Decoder/1-to-8-line Demultiplexer

Inputs				Outputs							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C ⁽¹⁾	B	A	G ⁽²⁾	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

- Notes) 1. C; input 1C and 2C connected together
 2. G; inputs 1G and 2G connected together
 3. H; high level, L; low level, X; irrelevant

HD74LS156

■ ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	V_{IH}		2.0	—	—	V	
	V_{IL}		—	—	0.8	V	
Output current	I_{OH}	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}, V_{OH}=5.5\text{V}$	—	—	100	μA	
Output voltage	V_{OL}	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$	$I_{OL}=4\text{mA}$	—	—	0.4	V
			$I_{OL}=8\text{mA}$	—	—	0.5	
Input current	I_{IH}	$V_{CC}=5.25\text{V}, V_I=2.7\text{V}$	—	—	20	μA	
	I_{IL}	$V_{CC}=5.25\text{V}, V_I=0.4\text{V}$	—	—	-0.4	mA	
	I_I	$V_{CC}=5.25\text{V}, V_I=7\text{V}$	—	—	0.1	mA	
Supply current**	I_{CC}	$V_{CC}=5.25\text{V}$	—	6.1	10	mA	
Input clamp voltage	V_{IK}	$V_{CC}=4.75\text{V}, I_{IK}=-18\text{mA}$	—	—	-1.5	V	

* $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

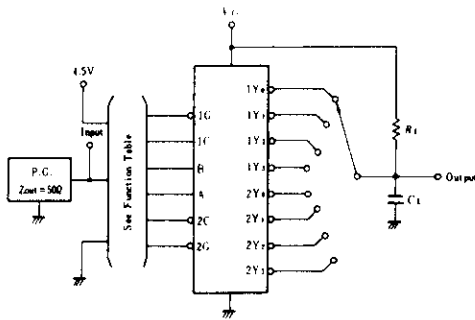
** I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5V, and 2C, 1G, and 2G inputs grounded.

■ SWITCHING CHARACTERISTICS ($V_{CC}=5\text{V}, T_a=25^\circ\text{C}$)

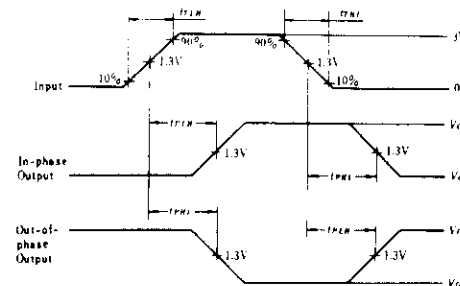
Item	Symbol	Inputs	Output	Level of logic	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	A, B, 2C, 1G or 2G	Y	2	$C_L=15\text{pF}, R_l=2\text{k}\Omega$	—	25	40	ns
	t_{PHL}	A, B, 2C, 1G or 2G	Y	2		—	34	51	
	t_{PLH}	A or B	Y	3		—	31	46	
	t_{PHL}	A or B	Y	3		—	34	51	
	t_{PLH}	1C	Y	3		—	32	48	
	t_{PHL}	1C	Y	3		—	32	48	

■ TESTING METHOD

1) Test Circuit



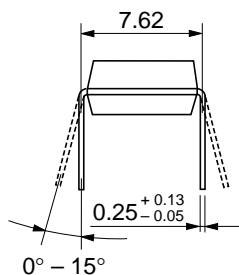
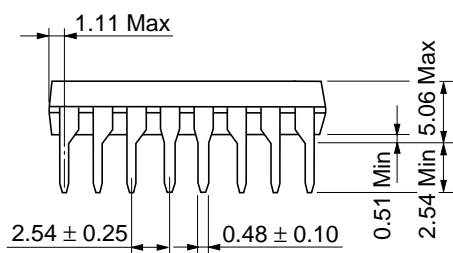
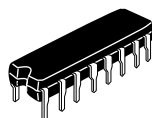
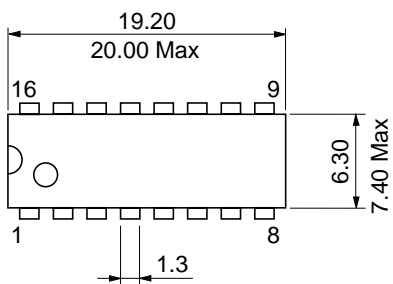
Waveform



- Notes) 1. Input pulse: $t_{TLH} \leq 15\text{ns}, t_{THL} \leq 6\text{ns}, \text{PRR}=1\text{MHz}, \text{duty cycle}=50\%$
 2. C_L includes probe and jig capacitance.

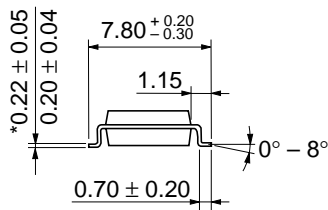
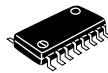
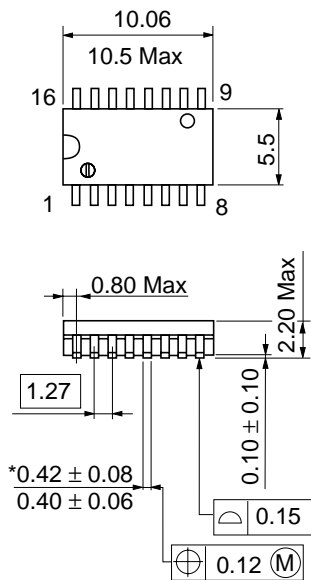
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Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

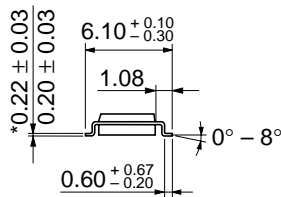
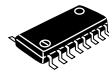
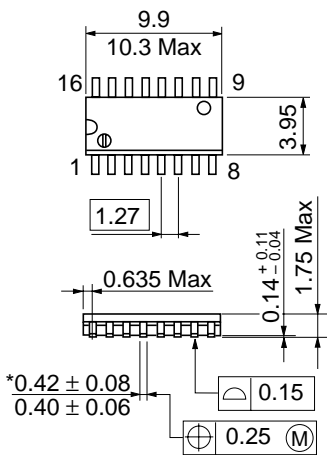
Unit: mm



Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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