

## 74AC08 • 74ACT08 Quad 2-Input AND Gate

### General Description

The AC/ACT08 contains four, 2-input AND gates.

### Features

- $I_{CC}$  reduced by 50% on 74AC only
- Outputs source/sink 24 mA

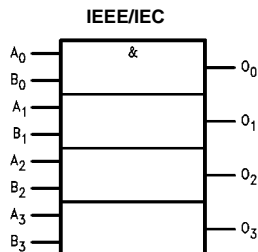
### Ordering Code:

Order Number	Package Number	Package Description
74AC08SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC08SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC08MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC08MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC08PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74AC08PC_NL (Note 1)	N14A	Pb-Free 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT08SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT08SCX_NL (Note 1)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT08MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT08MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT08PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT08PC_NL (Note 1)	N14A	Pb-Free 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

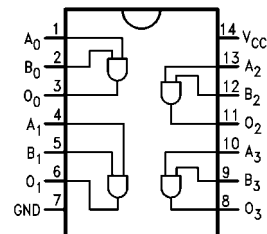
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code. (PC not available in Tape and Reel.)  
Pb-Free package per JEDEC J-STD-020B.

**Note 1:** ".NL" indicates Pb-Free package (per JEDEC J-STD-020B). Use this number to order device.

### Logic Symbol



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$A_n, B_n$	Inputs
$O_n$	Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Absolute Maximum Ratings (Note 2)		Recommended Operating Conditions	
Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V	Supply Voltage ( $V_{CC}$ )	AC 2.0V to 6.0V
DC Input Diode Current ( $I_{IK}$ )		ACT 4.5V to 5.5V	
$V_I = -0.5V$	-20 mA		
$V_I = V_{CC} + 0.5V$	+20 mA		
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$	Input Voltage ( $V_I$ )	0V to $V_{CC}$
DC Output Diode Current ( $I_{OK}$ )		Output Voltage ( $V_O$ )	0V to $V_{CC}$
$V_O = -0.5V$	-20 mA	Operating Temperature ( $T_A$ )	-40°C to +85°C
$V_O = V_{CC} + 0.5V$	+20 mA	Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$	AC Devices	
DC Output Source		$V_{IN}$ from 30% to 70% of $V_{CC}$	
or Sink Current ( $I_O$ )	$\pm 50$ mA	$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
DC $V_{CC}$ or Ground Current		Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA	ACT Devices	
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C	$V_{IN}$ from 0.8V to 2.0V	
Junction Temperature ( $T_J$ )		$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns
PDIP	140°C		

**Note 2:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

### DC Electrical Characteristics for AC

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits	Typ	Guaranteed Limits		
$V_{IH}$	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
$V_{IL}$	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
$V_{OH}$	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
			3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12$ mA $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 3)
			4.5		3.86	3.76		
			5.5		4.86	4.76		
$V_{OL}$	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
			3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 3)
			4.5		0.36	0.44		
			5.5		0.36	0.44		
$I_{IN}$ (Note 5)	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu A$	$V_I = V_{CC}, GND$	
$I_{OLD}$	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max	
$I_{OHD}$	Output Current (Note 4)	5.5			-75	mA	$V_{OHD} = 3.85V$ Min	
$I_{CC}$ (Note 5)	Maximum Quiescent Supply Current	5.5		2.0	20.0	$\mu A$	$V_{IN} = V_{CC}$ or GND	

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:**  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

DC Electrical Characteristics for ACT								
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	1.5	2.0	2.0			
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	1.5	0.8	0.8			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I <sub>OUT</sub> = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA (Note 6)	
		5.5		4.86	4.76			
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA (Note 6)	
		5.5		0.36	0.44			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	
I <sub>OLD</sub>	Minimum Dynamic Output Current (Note 7)	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>		5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

**Note 6:** All outputs loaded; thresholds on input associated with output under test.  
**Note 7:** Maximum test duration 2.0 ms, one output loaded at a time.

### AC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	7.5	9.5	1.0	10.0	ns
		5.0	1.5	5.5	7.5	1.0	8.5	
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	7.0	8.5	1.0	9.0	ns
		5.0	1.5	5.5	7.0	1.0	7.5	

**Note 8:** Voltage Range 3.3 is 3.3V ± 0.3V  
Voltage Range 5.0 is 5.0V ± 0.5V

### AC Electrical Characteristics for ACT

Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns
t <sub>PHL</sub>	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns

**Note 9:** Voltage Range 5.0 is 5.0V ± 0.5V

### Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	20.0	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M14A

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

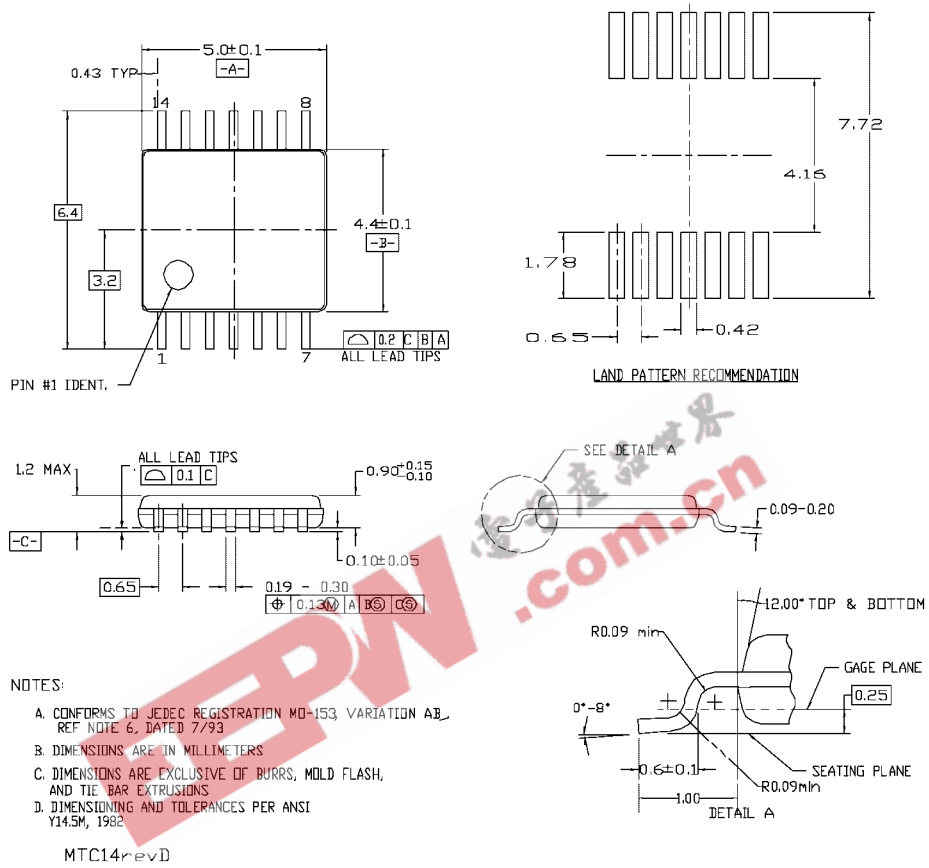
- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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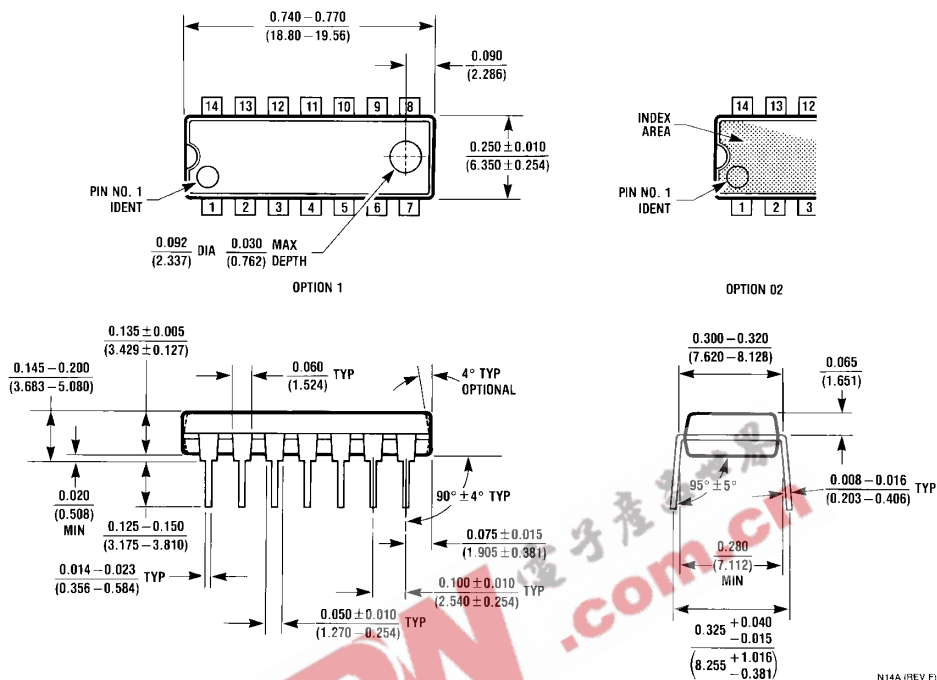
**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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