

SN54ALVTH16827, SN74ALVTH16827 2.5-V/3.3-V 20-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCES076E – JULY 1996 – REVISED DECEMBER 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) *Widebus*™ Design for 2.5-V and 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- High Drive (–24/24 mA at 2.5-V and –32/64 mA at 3.3-V V_{CC})
- Power Off Disables Outputs, Permitting Live Insertion
- High-Impedance State During Power Up and Power Down Prevents Driver Conflict
- Uses Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- Auto3-State Eliminates Bus Current Loading When Output Exceeds $V_{CC} + 0.5$ V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model; and Exceeds 1000 V Using Charged-Device Model, Robotic Method
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package

SN54ALVTH16827 . . . WD PACKAGE
SN74ALVTH16827 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1OE1	1	56	1OE2
1Y1	2	55	1A1
1Y2	3	54	1A2
GND	4	53	GND
1Y3	5	52	1A3
1Y4	6	51	1A4
V_{CC}	7	50	V_{CC}
1Y5	8	49	1A5
1Y6	9	48	1A6
1Y7	10	47	1A7
GND	11	46	GND
1Y8	12	45	1A8
1Y9	13	44	1A9
1Y10	14	43	1A10
2Y1	15	42	2A1
2Y2	16	41	2A2
2Y3	17	40	2A3
GND	18	39	GND
2Y4	19	38	2A4
2Y5	20	37	2A5
2Y6	21	36	2A6
V_{CC}	22	35	V_{CC}
2Y7	23	34	2A7
2Y8	24	33	2A8
GND	25	32	GND
2Y9	26	31	2A9
2Y10	27	30	2A10
2OE1	28	29	2OE2

description

The 'ALVTH16827 devices are 20-bit buffers/line drivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The devices are composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ($1OE1$ and $1OE2$, or $2OE1$ and $2OE2$) inputs must be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.



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 **TEXAS
INSTRUMENTS**

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SN54ALVTH16827, SN74ALVTH16827 2.5-V/3.3-V 20-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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description (continued)

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

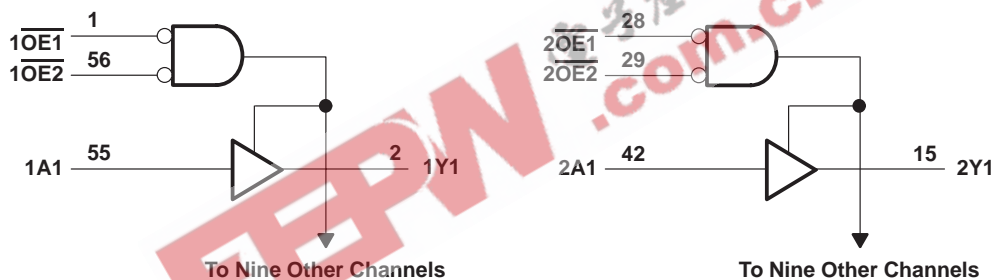
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ALVTH16827 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALVTH16827 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 10-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to 7 V
Output current in the low state, I_O : SN54ALVTH16827	96 mA
SN74ALVTH16827	128 mA
Output current in the high state, I_O : SN54ALVTH16827	-48 mA
SN74ALVTH16827	-64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DGV package	86°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (see Note 3)

		SN54ALVTH16827			SN74ALVTH16827			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	2.3		2.7	2.3		2.7	V
V_{IH}	High-level input voltage	1.7			1.7			V
V_{IL}	Low-level input voltage			0.7			0.7	V
V_I	Input voltage	0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current			-6			-8	mA
I_{OL}	Low-level output current			6			8	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$			18			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	10		ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
T_A	Operating free-air temperature	-55		125	-40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Note 3)

		SN54ALVTH16827			SN74ALVTH16827			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	3		3.6	3		3.6	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current			-24			-32	mA
I_{OL}	Low-level output current			24			32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$			48			64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	10		ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
T_A	Operating free-air temperature	-55		125	-40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH16827			SN74ALVTH16827			UNIT		
				MIN	TYP†	MAX	MIN	TYP†	MAX			
V_{IK}		$V_{CC} = 2.3\text{ V}$, $I_I = -18\text{ mA}$		-1.2			-1.2			V		
V_{OH}		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V		
		$V_{CC} = 2.3\text{ V}$, $I_{OH} = -6\text{ mA}$		1.8								
		$V_{CC} = 2.3\text{ V}$, $I_{OH} = -8\text{ mA}$					1.8					
V_{OL}		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2			V		
		$V_{CC} = 2.3\text{ V}$		$I_{OL} = 6\text{ mA}$		0.4		0.47				
				$I_{OL} = 8\text{ mA}$				0.4				
				$I_{OL} = 18\text{ mA}$		0.5						
				$I_{OL} = 24\text{ mA}$				0.5				
I_I		Control inputs $V_{CC} = 2.7\text{ V}$, $V_I = V_{CC}$ or GND		± 1			± 1			μA		
				$V_{CC} = 0$ or 2.7 V , $V_I = 5.5\text{ V}$		10			10			
		Data inputs $V_{CC} = 2.7\text{ V}$		$V_I = 5.5\text{ V}$		10			10			
				$V_I = V_{CC}$		1			1			
				$V_I = 0$		-5			-5			
I_{off}		$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V					± 100			μA		
I_{BHL}^\ddagger		$V_{CC} = 2.3\text{ V}$, $V_I = 0.7\text{ V}$		115			115			μA		
I_{BHH}^\S		$V_{CC} = 2.3\text{ V}$, $V_I = 1.7\text{ V}$		-10			-10			μA		
I_{BHLO}^\P		$V_{CC} = 2.7\text{ V}$, $V_I = 0$ to V_{CC}		300			300			μA		
$I_{BHHO}^\#$		$V_{CC} = 2.7\text{ V}$, $V_I = 0$ to V_{CC}		-300			-300			μA		
I_{EX}^\parallel		$V_{CC} = 2.3\text{ V}$, $V_O = 5.5\text{ V}$		125			125			μA		
$I_{OZ}(\text{PU/PD})^\star$		$V_{CC} \leq 1.2\text{ V}$, $V_O = 0.5\text{ V to } V_{CC}$, $V_I = \text{GND or } V_{CC}$, $OE = \text{don't care}$		± 100			± 100			μA		
I_{OZH}		$V_{CC} = 2.7\text{ V}$, $V_O = 2.3\text{ V}$, $V_I = 0.7\text{ V or } 1.7\text{ V}$		5			5			μA		
I_{OZL}		$V_{CC} = 2.7\text{ V}$, $V_O = 0.5\text{ V}$, $V_I = 0.7\text{ V or } 1.7\text{ V}$		-5			-5			μA		
I_{CC}		$V_{CC} = 2.7\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND		Outputs high		0.04	0.1	0.04	0.1	mA		
				Outputs low		2.3	5	2.3	5			
				Outputs disabled		0.04	0.1	0.04	0.1			
C_i		$V_{CC} = 2.5\text{ V}$, $V_I = 2.5\text{ V or } 0$		3			3			pF		
C_o		$V_{CC} = 2.5\text{ V}$, $V_O = 2.5\text{ V or } 0$		6			6			pF		

† All typical values are at $V_{CC} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

|| Current into an output in the high state when $V_O > V_{CC}$

* High-impedance state during power up or power down

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**electrical characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54ALVTH16827			SN74ALVTH16827			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}	V _{CC} = 3 V, I _I = -18 mA			-1.2			-1.2	V	
V _{OH}	V _{CC} = 3 V to 3.6 V, I _{OH} = -100 μA	V _{CC} -0.2			V _{CC} -0.2			V	
	V _{CC} = 3 V, I _{OH} = -24 mA	2			2				
V _{OL}	V _{CC} = 3 V to 3.6 V, I _{OL} = 100 μA	0.2			0.2			V	
	V _{CC} = 3 V	I _{OL} = 16 mA				0.4			
		I _{OL} = 24 mA	0.5						
		I _{OL} = 32 mA				0.5			
		I _{OL} = 48 mA	0.55						
I _{OL} = 64 mA				0.55					
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND	±1			±1			μA
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V	10			10			
	Data inputs	V _{CC} = 3.6 V, V _I = 5.5 V	10			10			
		V _{CC} = 3.6 V, V _I = V _{CC}	1			1			
		V _{CC} = 3.6 V, V _I = 0	-5			-5			
I _{off}	V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100			μA	
I _{BHL} ‡	V _{CC} = 3 V, V _I = 0.8 V	75			75			μA	
I _{BHH} §	V _{CC} = 3 V, V _I = 2 V	-75			-75			μA	
I _{BHLO} ¶	V _{CC} = 3.6 V, V _I = 0 to V _{CC}	500			500			μA	
I _{BHHO} #	V _{CC} = 3.6 V, V _I = 0 to V _{CC}	-500			-500			μA	
I _{EX}	V _{CC} = 3 V, V _O = 5.5 V	125			125			μA	
I _{OZ} (PU/PD)*	V _{CC} ≤ 1.2 V, V _O = 0.5 V to V _{CC} , V _I = GND or V _{CC} , OE = don't care	±100			±100			μA	
I _{OZH}	V _{CC} = 3.6 V, V _O = 3 V, V _I = 0.8 V or 2 V	5			5			μA	
I _{OZL}	V _{CC} = 3.6 V, V _O = 0.5 V, V _I = 0.8 V or 2 V	-5			-5			μA	
I _{CC}	V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	0.07	0.1	0.07	0.1	mA		
		Outputs low	3.2	6	3.2	6			
		Outputs disabled	0.07	0.1	0.07	0.1			
ΔI _{CC} □	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	0.4			0.4			mA	
C _i	V _{CC} = 3.3 V, V _I = 3.3 V or 0	3			3			pF	
C _o	V _{CC} = 3.3 V, V _O = 3.3 V or 0	6			6			pF	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

|| Current into an output in the high state when V_O > V_{CC}

* High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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2.5-V/3.3-V 20-BIT BUFFERS/DRIVERS
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switching characteristics over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16827		SN74ALVTH16827		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	3.2	1.5	3.2	ns
t_{PHL}			1.7	3.7	1.7	3.7	
t_{PZH}	OE	Y	1.9	4.3	1.9	4.3	ns
t_{PZL}			1.8	4	1.8	4	
t_{PHZ}	\overline{OE}	Y	2.5	5.6	2.5	5.6	ns
t_{PLZ}			1.7	4.6	1.7	4.6	

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 2)

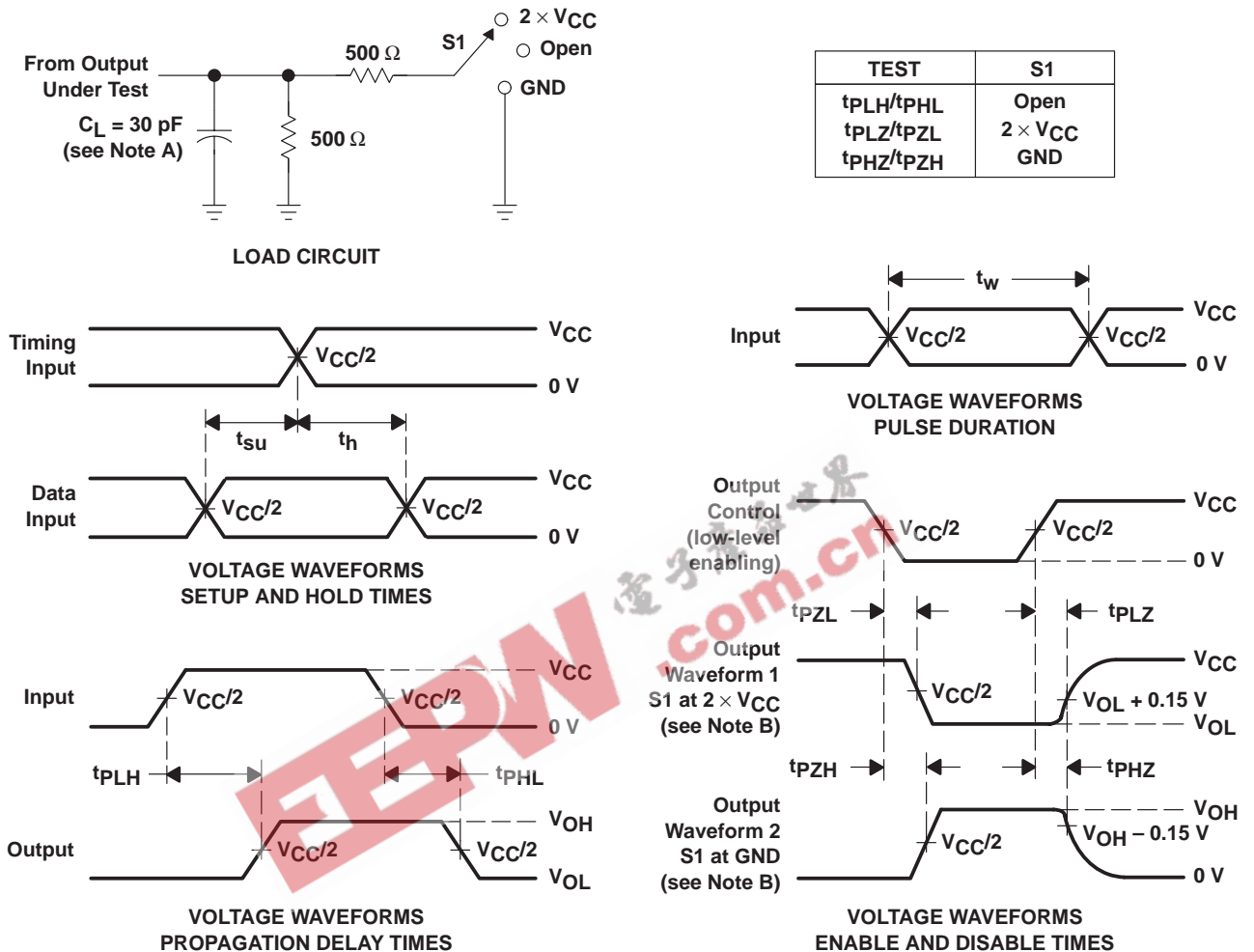
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16827		SN74ALVTH16827		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.8	3	1.8	3	ns
t_{PHL}			1.6	2.8	1.6	2.8	
t_{PZH}	\overline{OE}	Y	1.6	3.9	1.6	3.9	ns
t_{PZL}			1.5	3.4	1.5	3.4	
t_{PHZ}	\overline{OE}	Y	3.3	5.8	3.3	5.8	ns
t_{PLZ}			2.6	4.6	2.6	4.6	

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PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

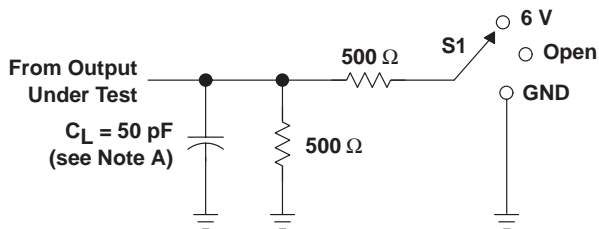
Figure 1. Load Circuit and Voltage Waveforms

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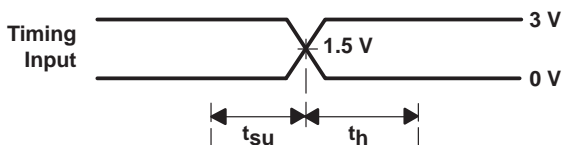
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

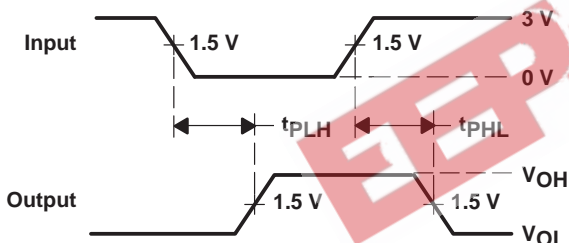


LOAD CIRCUIT

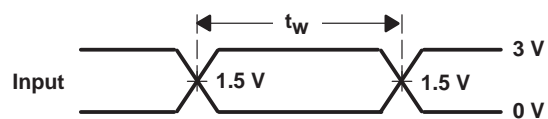
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



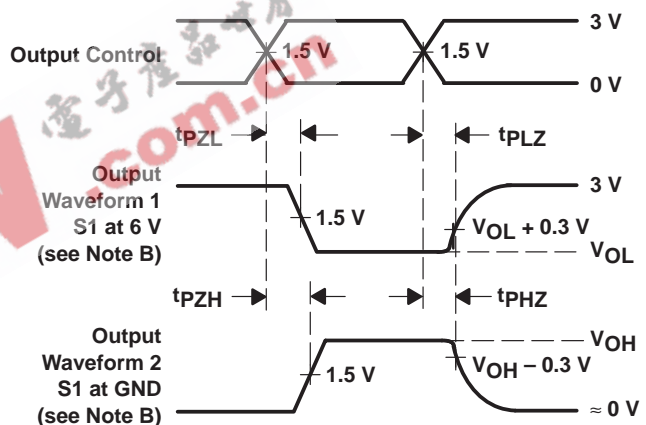
**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
 PULSE DURATION**



**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVTH16827DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16827DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16827GRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16827VRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16827VRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16827DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16827DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16827GR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16827VR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

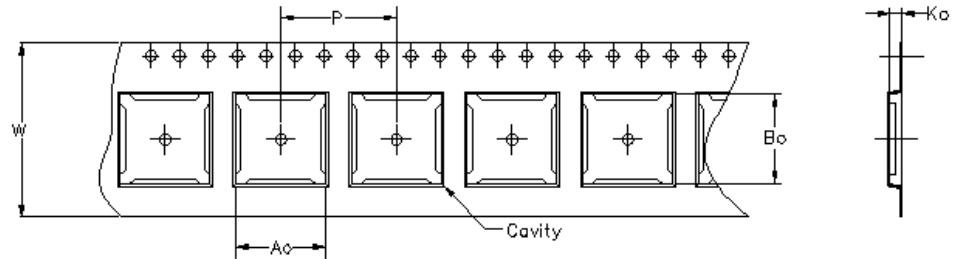
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

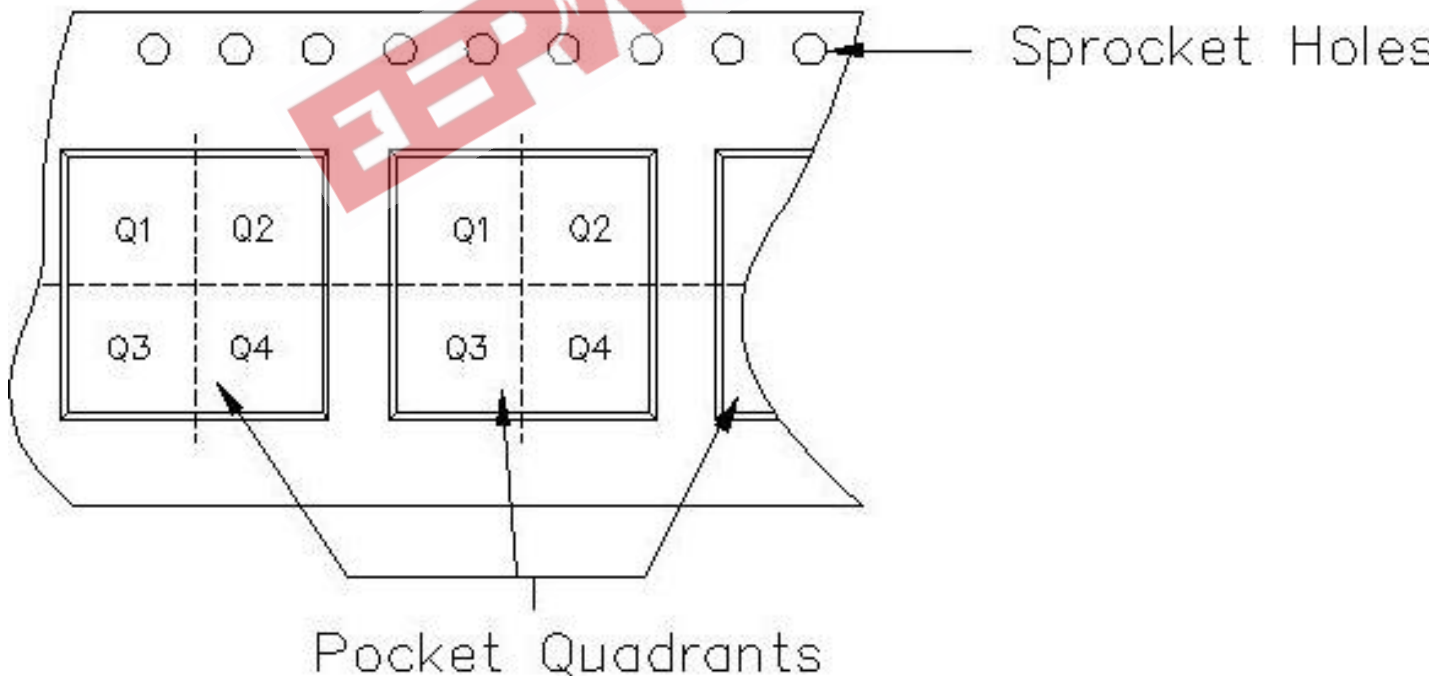
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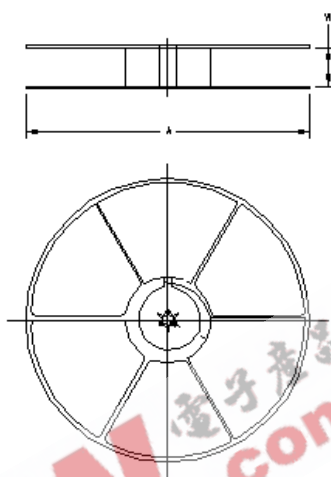
Carrier tape design is defined largely by the component length, width, and thickness.

A_o = Dimension designed to accommodate the component width.
B_o = Dimension designed to accommodate the component length.
K_o = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



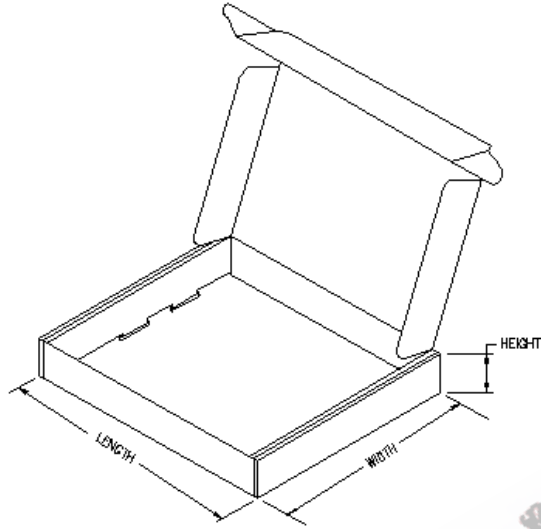
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVTH16827DLR	DL	56	MLA	330	32	11.35	18.67	3.1	16	32	Q1
SN74ALVTH16827GR	DGG	56	MLA	330	24	8.6	15.8	1.8	12	24	Q1
SN74ALVTH16827VR	DGV	56	MLA	330	24	6.8	10.1	1.6	12	24	Q1



TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74ALVTH16827DLR	DL	56	MLA	336.6	342.9	41.3
SN74ALVTH16827GR	DGG	56	MLA	333.2	333.2	31.75
SN74ALVTH16827VR	DGV	56	MLA	333.2	333.2	31.75



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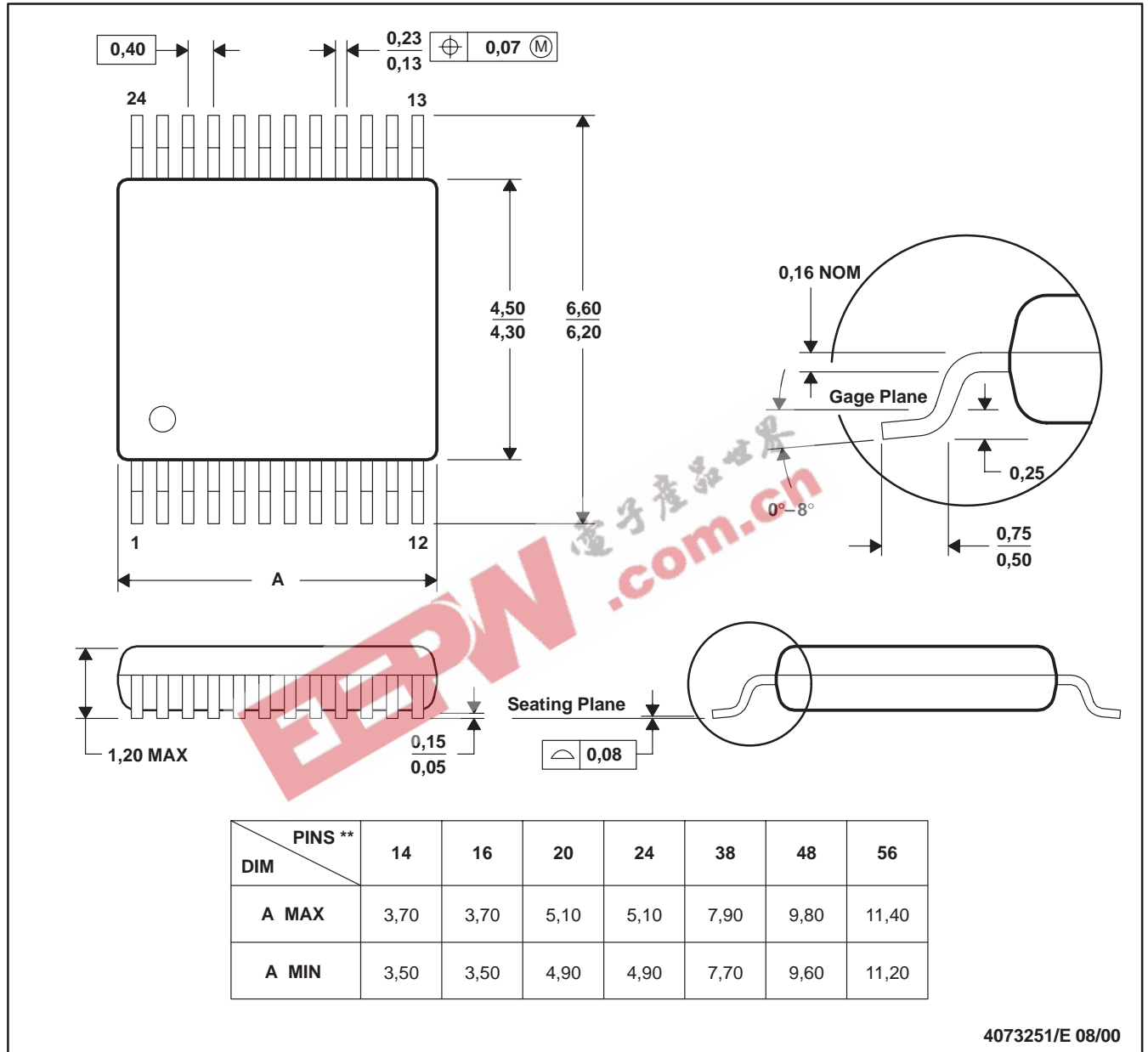
MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G)**

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

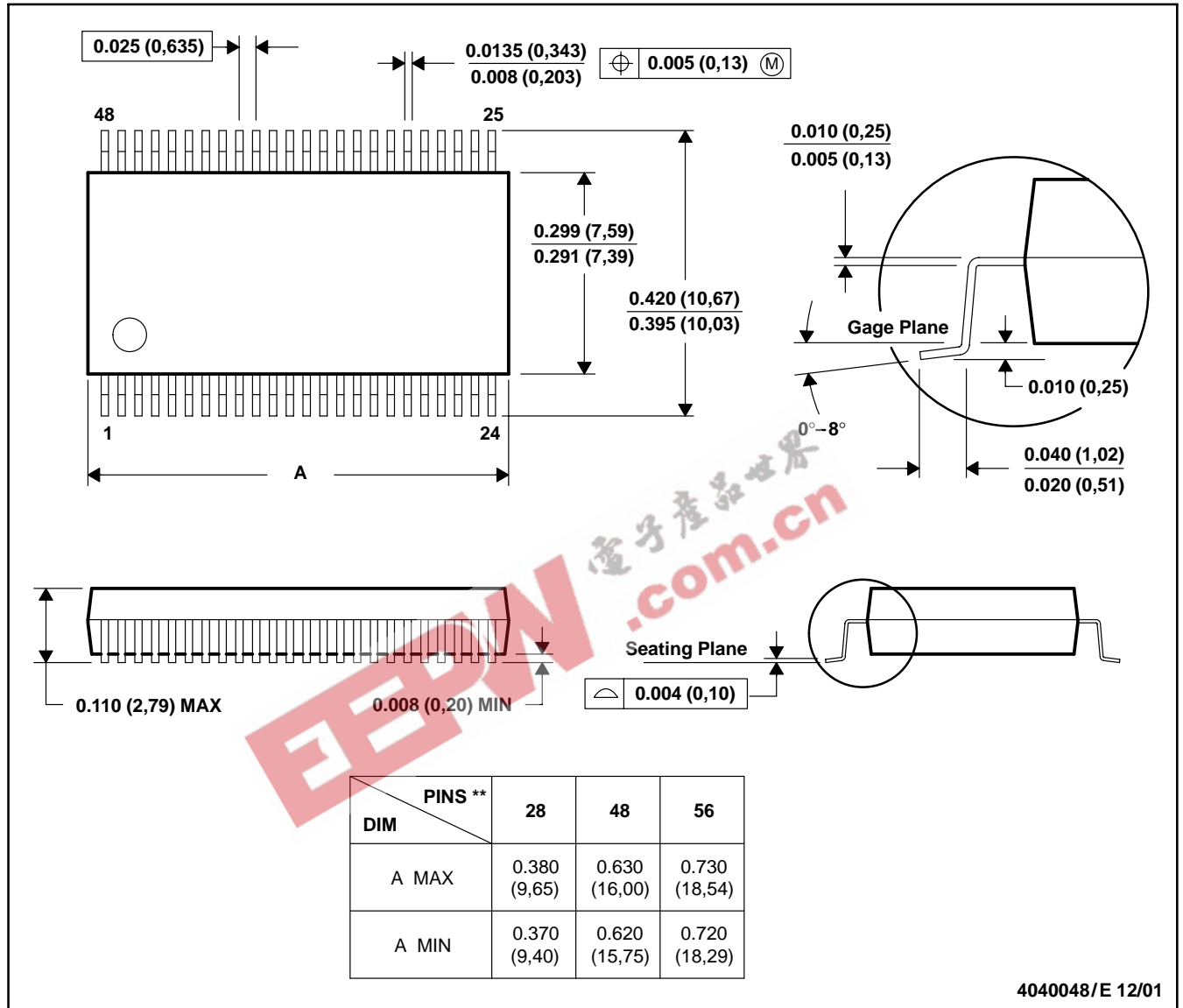
MECHANICAL DATA

MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

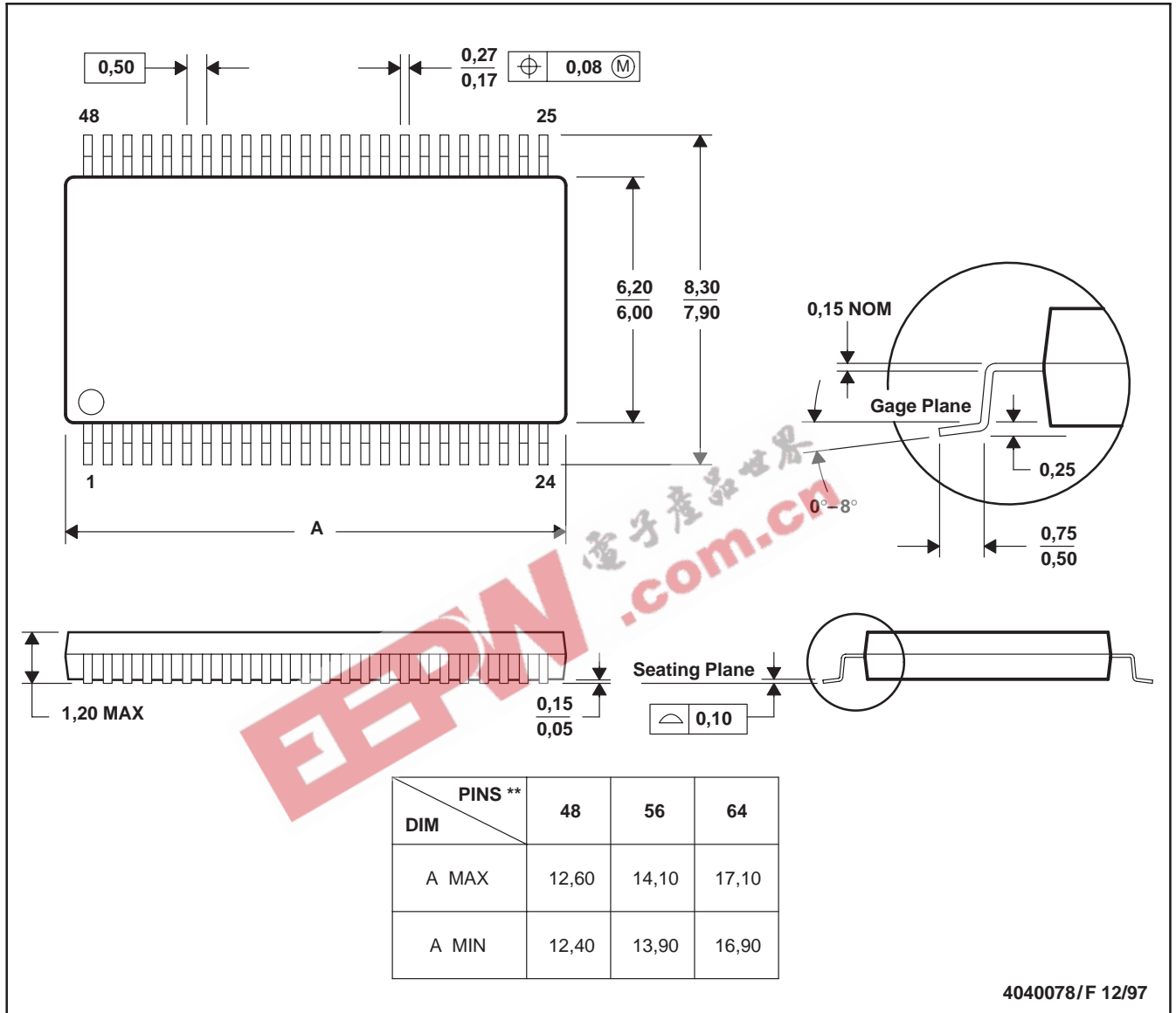
MECHANICAL DATA

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

4040078/F 12/97

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