

MC74HC86A

Quad 2-Input Exclusive OR Gate

High-Performance Silicon-Gate CMOS

The MC74HC86A is identical in pinout to the LS86. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Features

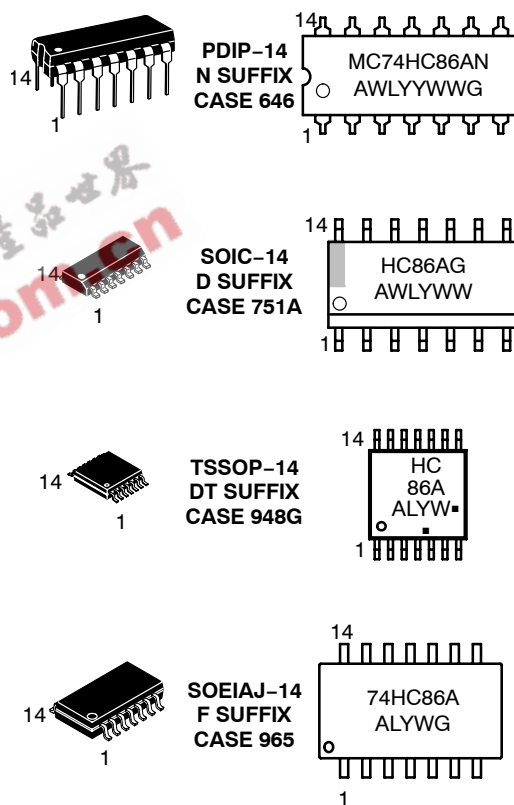
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with JEDEC Standard No. 7A Requirements
- Chip Complexity: 56 FETs or 14 Equivalent Gates
- Pb-Free Packages are Available



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<http://onsemi.com>

MARKING DIAGRAMS



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC74HC86A

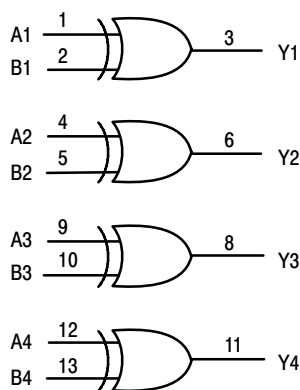
PIN ASSIGNMENT

A1	1	14	V _{CC}
B1	2	13	B4
Y1	3	12	A4
A2	4	11	Y4
B2	5	10	B3
Y2	6	9	A3
GND	7	8	Y3

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

LOGIC DIAGRAM



$$Y = A \oplus B$$

$$= \bar{A}B + A\bar{B}$$

PIN 14 = V_{CC}
PIN 7 = GND

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC86AN	PDIP-14	25 Units / Rail
MC74HC86ANG	PDIP-14 (Pb-Free)	
MC74HC86AD	SOIC-14	55 Units / Rail
MC74HC86ADG	SOIC-14 (Pb-Free)	
MC74HC86ADR2	SOIC-14	2500 / Tape & Reel
MC74HC86ADR2G	SOIC-14 (Pb-Free)	
MC74HC86ADTR2	TSSOP-14*	
MC74HC86ADTR2G	TSSOP-14*	
MC74HC86AF	SOEIAJ-14	50 Units / Rail
MC74HC86AFG	SOEIAJ-14 (Pb-Free)	
MC74HC86AFEL	SOEIAJ-14	2000 / Tape & Reel
MC74HC86AFELG	SOEIAJ-14 (Pb-Free)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	− 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	− 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — Plastic DIP: − 10 mW/°C from 65° to 125°C

SOIC Package: − 7 mW/°C from 65° to 125°C

TSSOP Package: − 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	− 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				− 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 2.4 \text{ mA}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 2.4 \text{ mA}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	V

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	1.0	10	40	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	100 80 20 17	125 90 25 21	150 110 31 26	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Gate)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		33	

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

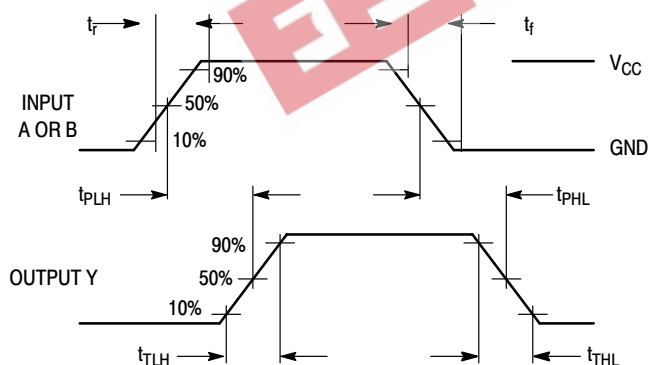
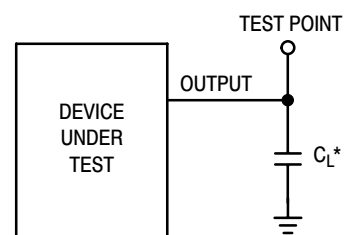


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

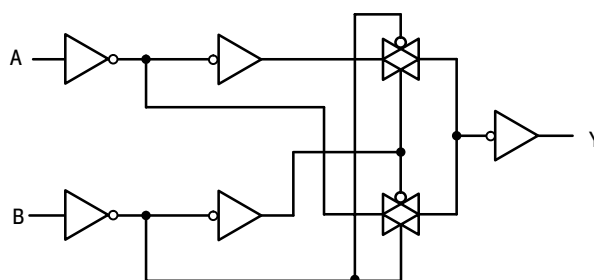
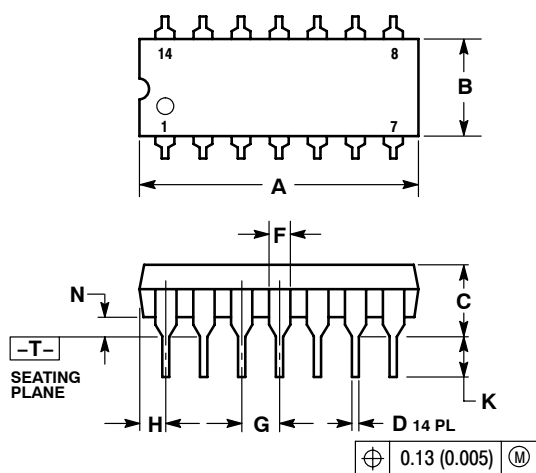


Figure 3. Expanded Logic Diagram
(1/4 of Device)

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PACKAGE DIMENSIONS

PDIP-14
CASE 646-06
ISSUE P



NOTES:

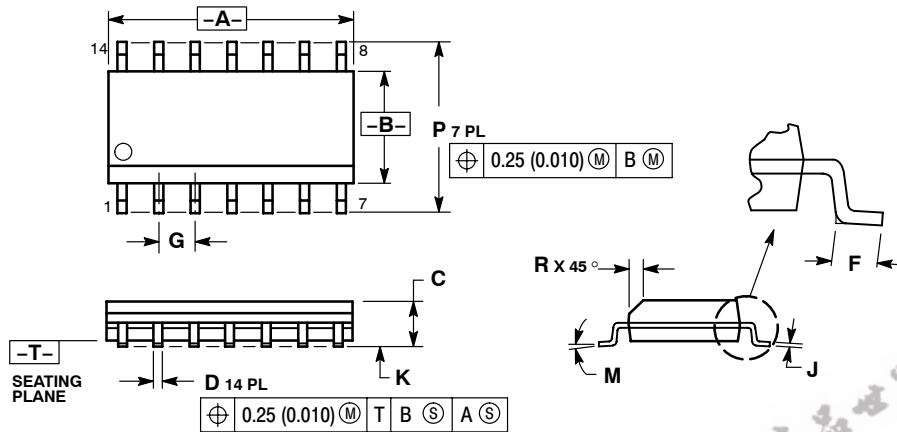
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M		10 °		10 °
N	0.015	0.039	0.38	1.01

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PACKAGE DIMENSIONS

SOIC-14
CASE 751A-03
ISSUE H

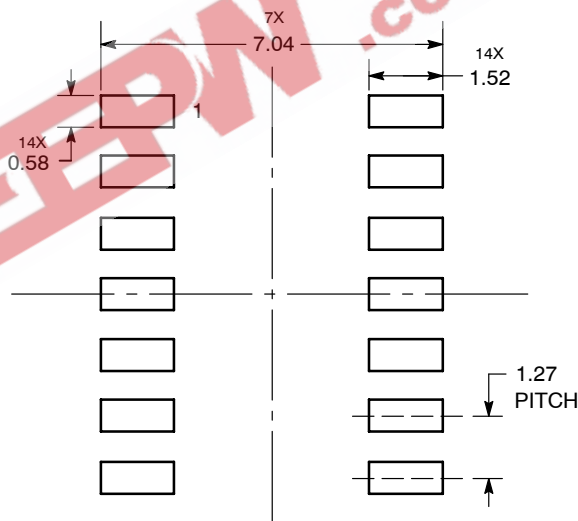


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC	0.050 BSC		
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

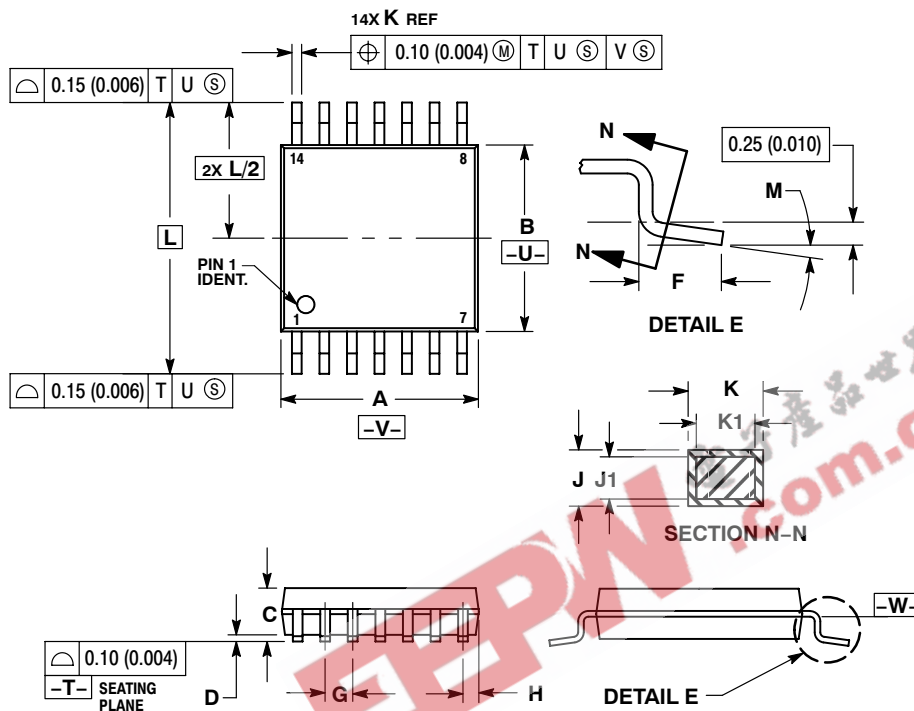


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

TSSOP-14
CASE 948G-01
ISSUE B

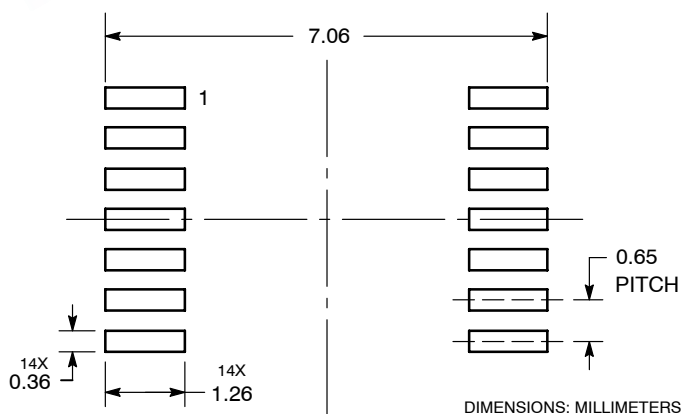


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*

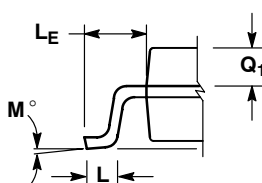
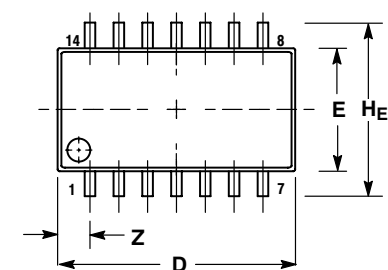


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

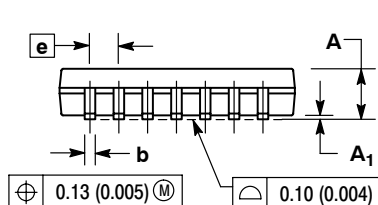
MC74HC86A

PACKAGE DIMENSIONS

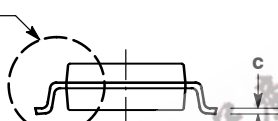
SOEIAJ-14
CASE 965-01
ISSUE A



DETAIL P



VIEW P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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