FAIRCHILD SEMICONDUCTOR®

July 1999
Revised February 2005

74VCX38
Low Voltage Quad 2-Input NAND Gate with Open Drain Outputs and 3.6V Tolerant Inputs and Outputs

General Description

The VCX38 contains four 2-input NAND gates with open drain outputs. This product is designed for low voltage (1.2V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The VCX38 is fabricated with advanced CMOS technology to achieve high-speed operation while maintaining CMOS low power dissipation.

Features

- 1.2V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD}
  2.8 ns max for 3.0V to 3.6V V_{CC}
- Power-Off high impedance inputs and outputs
- Static Drive (I_{OL})
  +24 mA @ 3.0V V_{CC}
- Uses patented Quiet Series™ noise/EMI reduction circuitry
- Latchup performance exceeds JEDEC 78 conditions
- ESD performance:
  Human body model > 2000V
  Machine model > 250V
- Leadless Pb-Free DQFN package

Ordering Code:

Order Number	Package Number	Package Description
74VCX38M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VCX38BQX (Note 1)	MLP014A	Pb-Free 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
74VCX38MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VCX38MTCX_NL	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

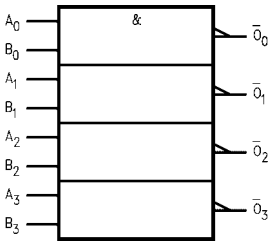
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: DQFN package available in Tape and Reel.

Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

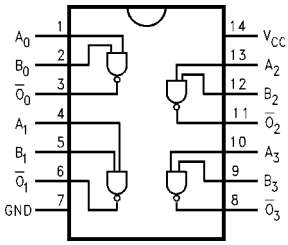
Logic Symbol

IEEE/IEC



Connection Diagrams

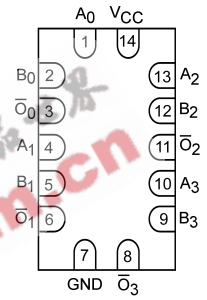
Pin Assignments for SOIC and TSSOP



Pin Descriptions

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

Pad Assignments for DQFN



(Top View)

Absolute Maximum Ratings (Note 2)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
Output Voltage (V_O) (Note 3)	−0.5V to +4.6V
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
DC Output Source/Sink Current (I_{OL})	+50 mA
DC V_{CC} or Ground Current per	±100 mA
Supply Pin (I_{CC} or Ground)	
Storage Temperature Range (T_{stg})	−65°C to +150°C

Recommended Operating Conditions (Note 4)

Power Supply	
Operating	1.2V to 3.6V
Input Voltage	−0.3V to 3.6V
Output Voltage (V_O)	0V to 3.6V
Output Current in I_{OL}	
V_{CC} = 3.0V to 3.6V	+24 mA
V_{CC} = 2.3V to 2.7V	+18 mA
V_{CC} = 1.65V to 2.3V	+6 mA
V_{CC} = 1.4V to 1.6V	+2 mA
V_{CC} = 1.2V	±100 μA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{in} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Floating or unused inputs must be held HIGH or LOW

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		
			2.3 - 2.7	1.6		
			1.65 - 2.3	0.65 × V_{CC}		V
			1.4 - 1.6	0.65 × V_{CC}		
			1.2	0.65 × V_{CC}		
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	
			2.3 - 2.7		0.7	
			1.65 - 2.3		0.35 × V_{CC}	V
			1.4 - 1.6		0.35 × V_{CC}	
			1.2		0.05 × V_{CC}	
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7 - 3.6		0.2	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 18 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
		I_{OL} = 100 μA	2.3 - 2.7		0.2	
		I_{OL} = 12 mA	2.3		0.4	V
		I_{OL} = 18 mA	2.3		0.6	
		I_{OL} = 100 μA	1.65 - 2.3		0.2	
		I_{OL} = 6 mA	1.65		0.3	
		I_{OL} = 100 μA	1.4 - 1.6		0.2	
		I_{OL} = 2 mA	1.4		0.35	
		I_{OL} = 100 μA	1.2		0.05	
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6V	1.2 - 3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	0 ≤ (V_I, V_O) ≤ 3.6V	0		10.0	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	1.2 - 3.6		20.0	μA
		V_{CC} ≤ (V_I) ≤ 3.6V	1.2 - 3.6		±20.0	
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} −0.6V	2.7 - 3.6		750	μA
I_{OHZ}	Off State Current	V_O = 3.6	1.2 - 3.6		10.0	μA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units	Figure Number
				Min	Max		
t_{PZL}, t_{PLZ}	Propagation Delay	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	0.6	2.8	ns	Figures 1, 2
			2.5 ± 0.2	0.8	3.7		
			1.8 ± 0.15	1.0	6.7		
		$C_L = 15$ pF, $R_L = 2k\Omega$	1.5 ± 0.1	1.0	13.4		Figures 3, 4
			1.2		33.5		
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 6)	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		$C_L = 15$ pF, $R_L = 2k\Omega$	1.5 ± 0.1		1.5		
			1.2		1.5		

Note 5: For $C_L = 50_P$F, add approximately 300 ps to the 30 pF AC maximum specification.

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

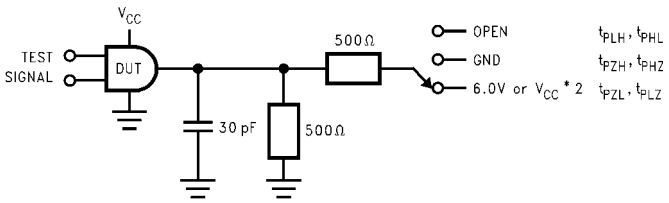
Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	–0.25	V
			2.5	–0.6	
			3.3	–0.8	

Capacitance

Symbol	Parameter	Conditions	T_A +25°C Typical	Units
C_{IN}	Input Capacitance	$V_I = 0v$ OR V_{CC}, $V_{CC} = 1.8V$, 2.5V or 3.3V	6.0	pF
C_{OUT}	Output Capacitance	$V_I = 0V$ or V_{CC}, $V_{CC} = 1.8V$, 2.5V or 3.3V	7.0	pF
C_{PD}	Power Dissipation Capacitance	$V_I = 0V$ or V_{CC}, $f = 10$ MHz, $V_{CC} = 1.8V$, 2.5V or 3.3V	20.0	pF

AC Loading and Waveforms (V_{CC} 3.3V ± 0.3V to 1.8V ± 0.15V)



TEST	SWITCH
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V; V_{CC} × 2 at V_{CC} = 2.5V ± 0.2V; 1.8V

FIGURE 1. AC Test Circuit

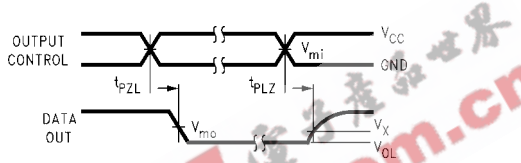
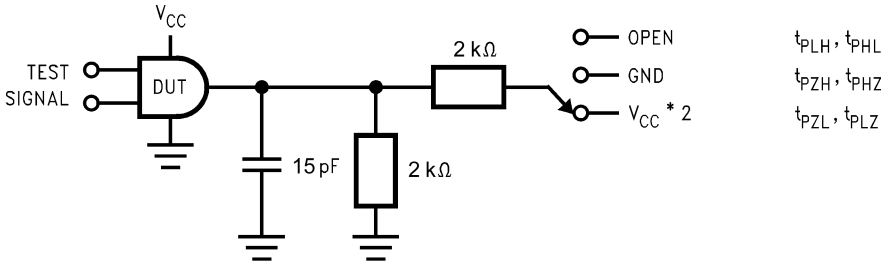


FIGURE 2. Waveform for Open Drain, Inverting and Non-inverting Functions

Symbol	V_{CC}		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V

AC Loading and Waveforms (V_{CC} 1.5 ± 0.1V to 1.2V)



TEST	SWITCH
t_{PZL}, t_{PLZ}	V_{CC} x 2 at V_{CC} = 1.5V ± 0.1V

FIGURE 3. AC Test Circuit

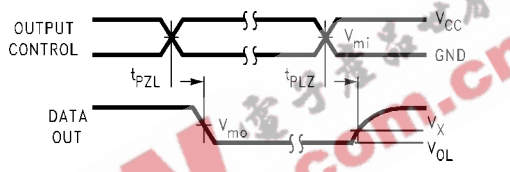


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

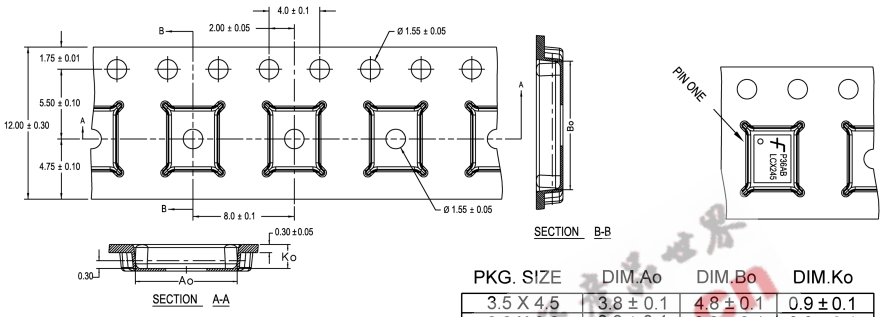
Symbol	V_{CC}
	1.5V ± 0.1V
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$
V_X	V_{OL} +0.1V
V_Y	V_{OH} −0.1V

Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



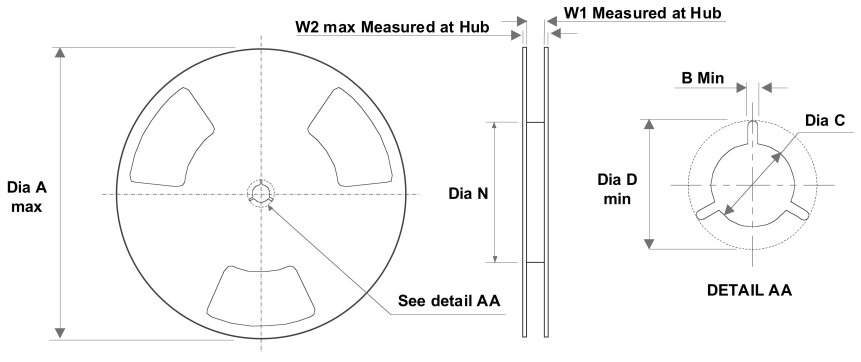
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

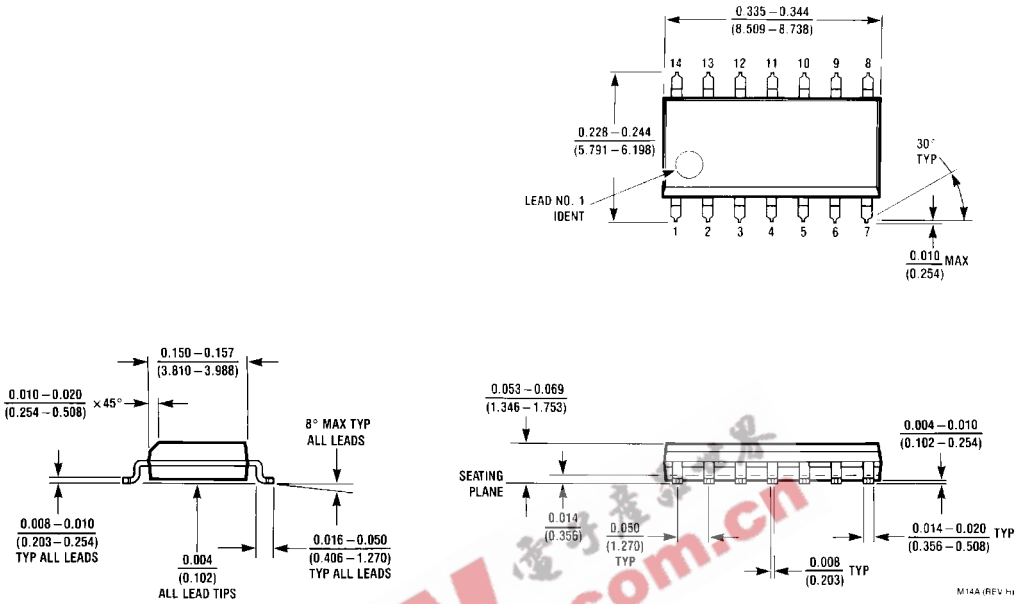
1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.

REEL DIMENSIONS inches (millimeters)



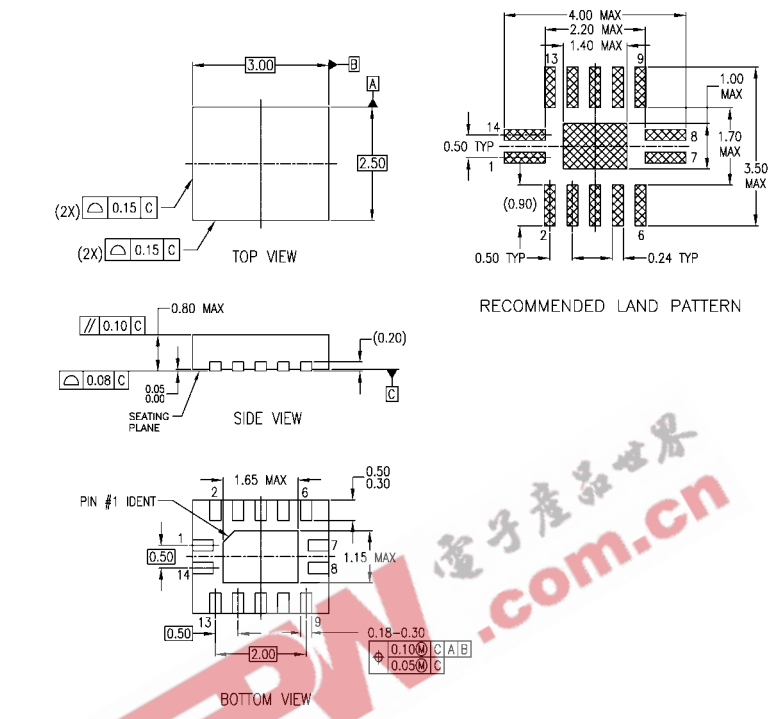
Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–241, VARIATION AA

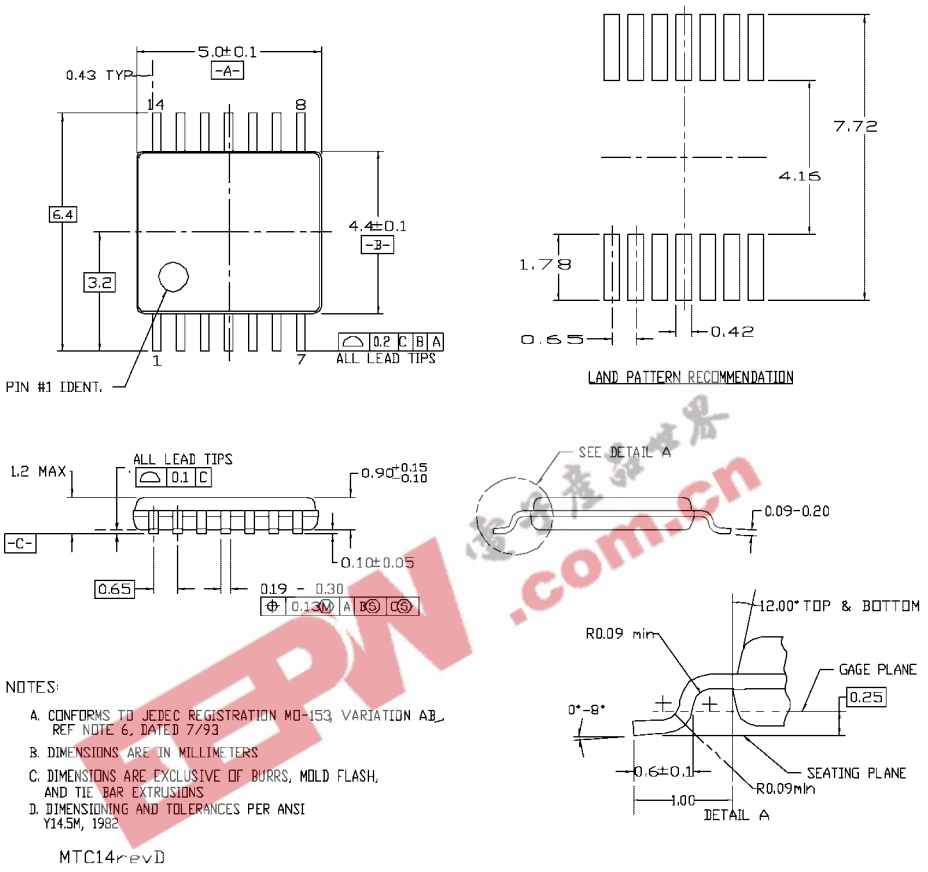
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP014ArevA

Pb-Free 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
Package Number MLP014A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

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