

April 1988 Revised July 1999

# 74F02 Quad 2-Input NOR Gate

#### **General Description**

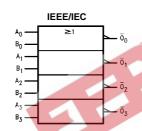
This device contains four independent gates, each of which performs the logic NOR function.

### **Ordering Code:**

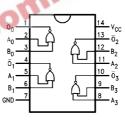
Order Number	Package Number	Package Description
74F02SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F02SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F02PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code

### **Logic Symbol**



### Connection Diagram



## Unit Loading/Fan Out

Pin Names	Description	U.L.	Input I <sub>IH</sub> /I <sub>IL</sub>	
Fill Names	Description	HIGH/LOW	Output I <sub>OH</sub> /I <sub>OL</sub>	
A <sub>n</sub> , B <sub>n</sub>	Inputs	1.0/1.0	20 μA/–0.6 mA	
$\overline{O}_n$	Outputs	50/33.3	−1 mA/20 mA	

#### **Absolute Maximum Ratings**(Note 1)

Storage Temperature  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ 

Input Current (Note 2) —30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with  $V_{CC} = 0V$ )

Standard Output -0.5V to  $V_{CC}$ 3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max)  $\qquad \qquad \text{twice the rated I}_{OL} \, (\text{mA})$ 

# Recommended Operating Conditions

Free Air Ambient Temperature  $0^{\circ}$ C to  $+70^{\circ}$ C Supply Voltage +4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

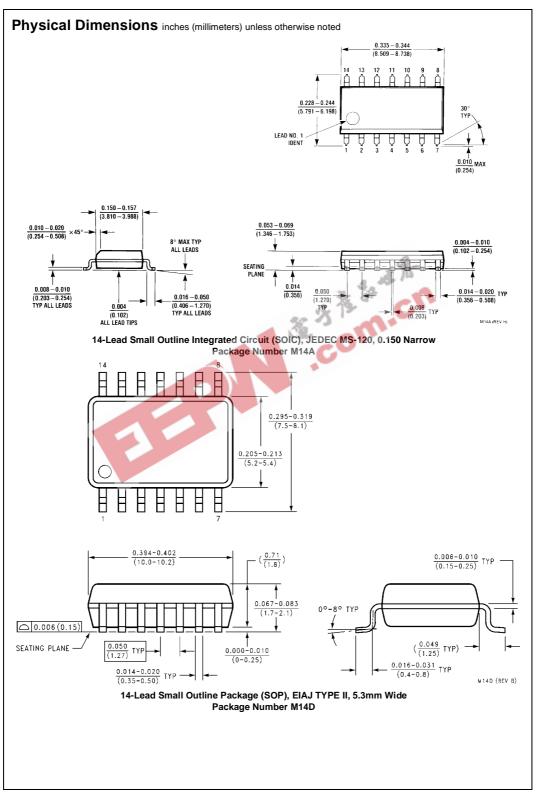
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

#### **DC Electrical Characteristics**

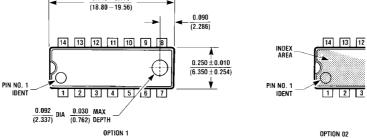
Symbol	Parameter	Min	Тур	Max	Units	V <sub>CC</sub>	Conditions	
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	100	Recognized as a HIGH Signal	
V <sub>IL</sub>	Input LOW Voltage			0.8	V	-1	Recognized as a LOW Signal	
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = −18 mA	
V <sub>OH</sub>	Output HIGH 10% V <sub>CC</sub>	2.5	30	22	V	Min	I <sub>OH</sub> = -1 mA	
	Voltage 5% V <sub>CC</sub>	2.7	A CH				$I_{OH} = -1 \text{ mA}$	
V <sub>OL</sub>	Output LOW 10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA	
	Voltage							
I <sub>IH</sub>	Input HIGH	11		5.0	μΑ	Max	V <sub>IN</sub> = 2.7V	
	Current							
I <sub>BVI</sub>	Input HIGH Current			7.0	μΑ	Max	V <sub>IN</sub> = 7.0V	
	Breakdown Test						V IN = 1.0 V	
I <sub>CEX</sub>	Output HIGH			50	μА	Max	V <sub>OUT</sub> = V <sub>CC</sub>	
	Leakage Current			30	μΑ	IVICA		
V <sub>ID</sub>	Input Leakage	4.75			٧	0.0	$I_{ID} = 1.9 \mu A$	
	Test	4.75			•	0.0	All other pins grounded	
I <sub>OD</sub>	Output Leakage			3.75	μΑ	0.0	V <sub>IOD</sub> = 150 mV	
	Circuit Current						All other pins grounded	
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	$V_{IN} = 0.5V$	
Ios	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V	
I <sub>CCH</sub>	Power Supply Current		3.7	5.6	mA	Max	V <sub>O</sub> = HIGH	
I <sub>CCL</sub>	Power Supply Current		8.7	13.0	mA	Max	$V_O = LOW$	

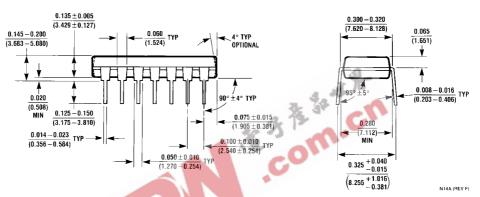
#### **AC Electrical Characteristics**

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		$T_A = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		Units
		Min	Тур	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	2.5	4.4	5.5	2.5	7.5	2.5	6.5	
t <sub>PHL</sub>	$A_n$ , $B_n$ to $\overline{O}_n$	1.5	3.2	4.3	1.5	6.5	1.5	5.3	ns



# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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