



May 2007

# 74F132

## Quad 2-Input NAND Schmitt Trigger

### General Description

The F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt Trigger followed by level shifting circuitry and a standard FAST™ output

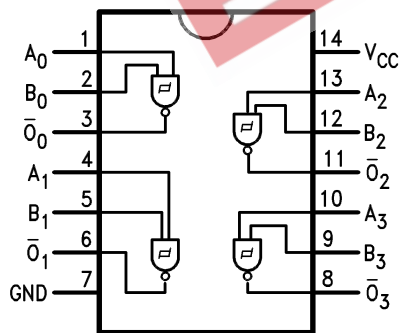
structure. The Schmitt Trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

### Ordering Information

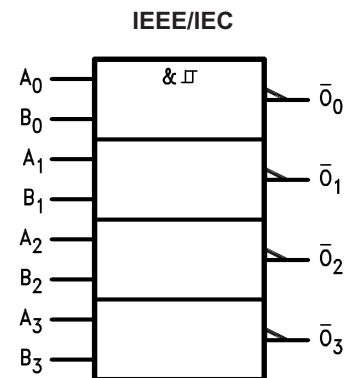
Order Number	Package Number	Package Description
74F132SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74F132SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

### Connection Diagram



### Logic Symbol



### Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ , Output $I_{OH}/I_{OL}$
$A_n, B_n$	Inputs	1.0 / 1.0	20μA / -0.6mA
$\bar{O}_n$	Outputs	50 / 33.3	-1mA / 20mA

### Function Table

Inputs		Outputs
A	B	$\bar{O}$
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

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## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$T_{STG}$	Storage Temperature	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
$T_A$	Ambient Temperature Under Bias	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
$T_J$	Junction Temperature Under Bias	$-55^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
$V_{CC}$	$V_{CC}$ Pin Potential to Ground Pin	$-0.5\text{V}$ to $+7.0\text{V}$
$V_{IN}$	Input Voltage <sup>(1)</sup>	$-0.5\text{V}$ to $+7.0\text{V}$
$I_{IN}$	Input Current <sup>(1)</sup>	$-30\text{mA}$ to $+5.0\text{mA}$
$V_O$	Voltage Applied to Output in HIGH State (with $V_{CC} = 0\text{V}$ ) Standard Output 3-STATE Output	$-0.5\text{V}$ to $V_{CC}$ $-0.5\text{V}$ to $5.5\text{V}$
	Current Applied to Output in LOW State (Max.)	twice the rated $I_{OL}$ (mA)
	ESD Last Passing Voltage (Min.)	4000V

### Note:

1. Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$T_A$	Free Air Ambient Temperature	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$
$V_{CC}$	Supply Voltage	$+4.5\text{V}$ to $+5.5\text{V}$

**DC Electrical Characteristics**

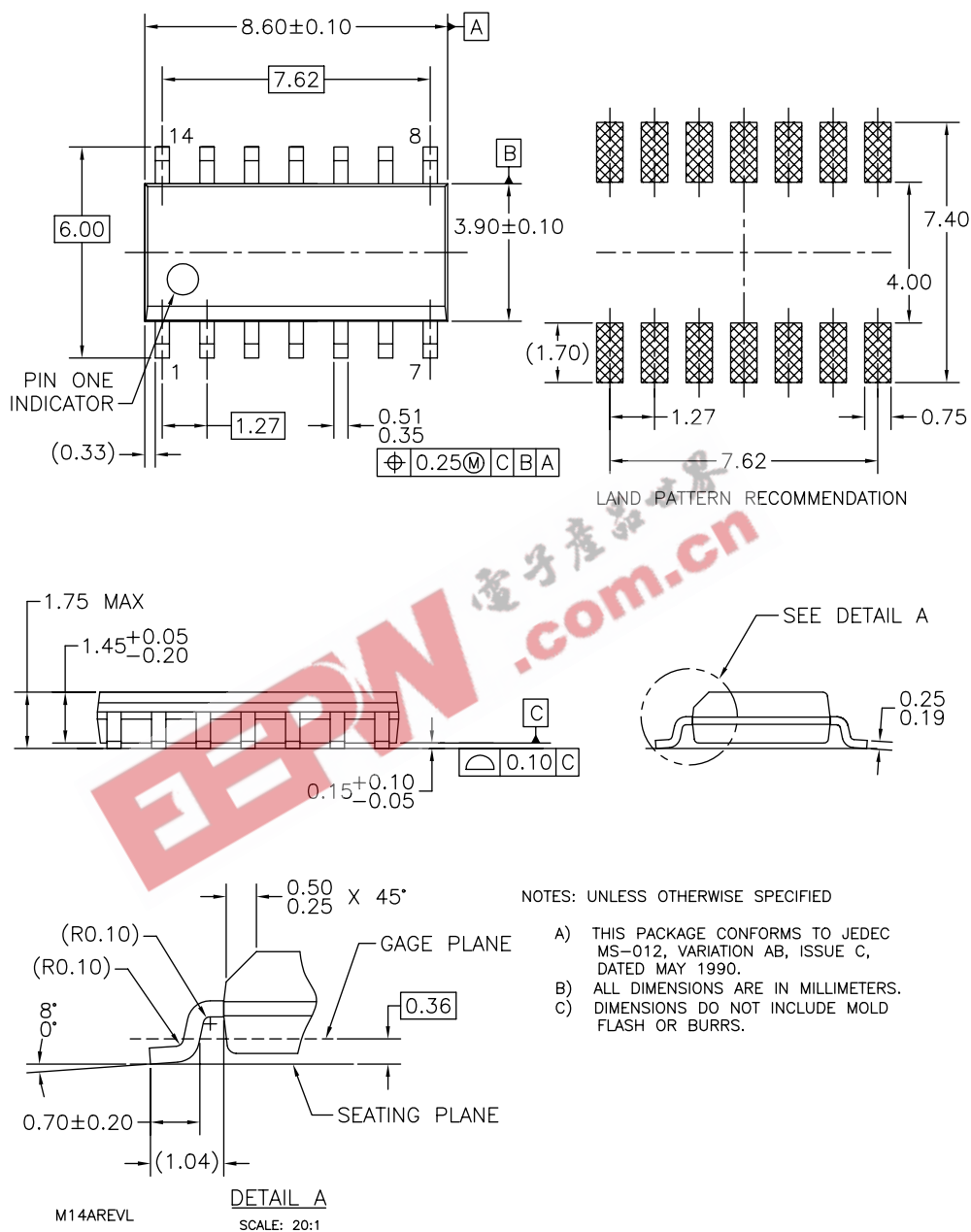
Symbol	Parameter	V <sub>CC</sub>	Conditions	Min.	Typ.	Max.	Units
V <sub>T+</sub>	Positive-going Threshold	5.0		1.5		2.0	V
V <sub>T-</sub>	Negative-going Threshold	5.0		0.7		1.1	V
ΔV <sub>T</sub>	Hysteresis (V <sub>T+</sub> – V <sub>T-</sub> )	5.0		0.4			V
V <sub>CD</sub>	Input Clamp Diode Voltage	Min.	I <sub>IN</sub> = –18mA			–1.2	V
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub>	Min. I <sub>OH</sub> = –1mA	2.5			V
		5% V <sub>CC</sub>	I <sub>OH</sub> = –1mA	2.7			
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>	Min. I <sub>OL</sub> = 20mA			0.5	V
I <sub>IH</sub>	Input HIGH Current	Max.	V <sub>IN</sub> = 2.7V			5.0	μA
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	Max.	V <sub>IN</sub> = 7.0V			7.0	μA
I <sub>CEX</sub>	Output HIGH Leakage Current	Max.	V <sub>OUT</sub> = V <sub>CC</sub>			50	μA
V <sub>ID</sub>	Input Leakage Test	0.0	I <sub>ID</sub> = 1.9μA, All Other Pins Grounded	4.75			V
I <sub>OD</sub>	Output Leakage Circuit Current	0.0	V <sub>IOD</sub> = 150mV, All Other Pins Grounded			3.75	μA
I <sub>IL</sub>	Input LOW Current	Max	V <sub>IN</sub> = 0.5V			–0.6	mA
I <sub>OS</sub>	Output Short-Circuit Current	Max	V <sub>OUT</sub> = 0V	–60		–150	mA
I <sub>CCH</sub>	Power Supply Current	Max	V <sub>O</sub> = HIGH			17.0	mA
I <sub>CCL</sub>	Power Supply Current	Max	V <sub>O</sub> = LOW			18.0	mA

**AC Electrical Characteristics**

Symbol	Parameter	T <sub>A</sub> = +25°C, V <sub>CC</sub> = +5.0V, C <sub>L</sub> = 50pF			T <sub>A</sub> = 0°C to +70°C, V <sub>CC</sub> = +5.0V, C <sub>L</sub> = 50pF		Units
		Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub>	Propagation Delay, A <sub>n</sub> , B <sub>n</sub> to $\overline{O}_n$	4.0		10.5	3.5	12.0	ns
t <sub>PHL</sub>		5.0		12.5	5.0	13.0	

## Physical Dimensions

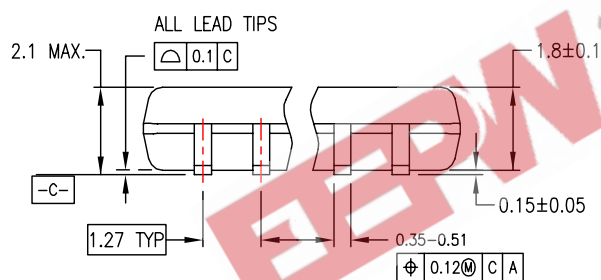
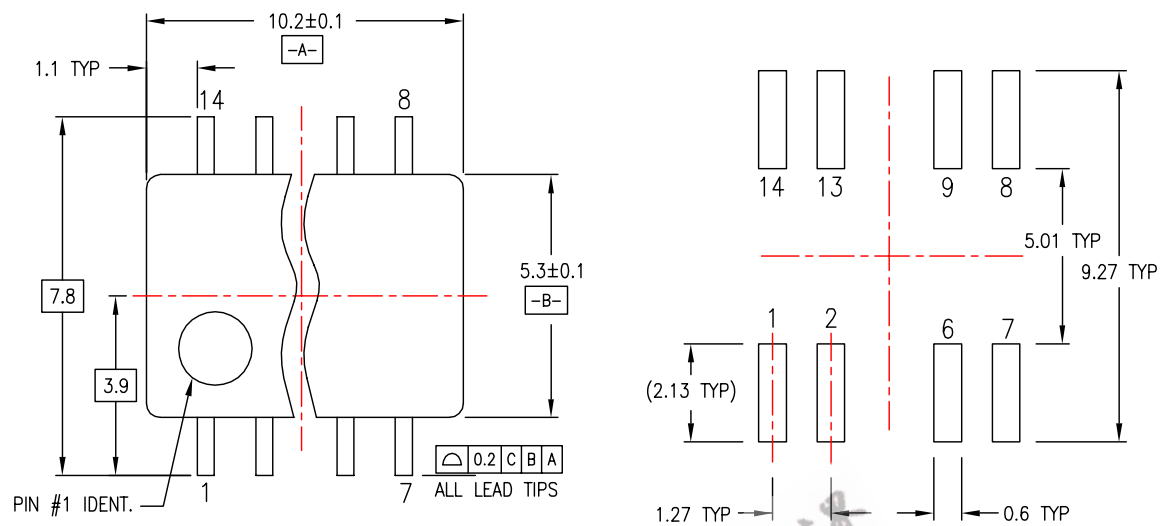
Dimensions are in millimeters unless otherwise noted.



**Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A**

### Physical Dimensions (Continued)

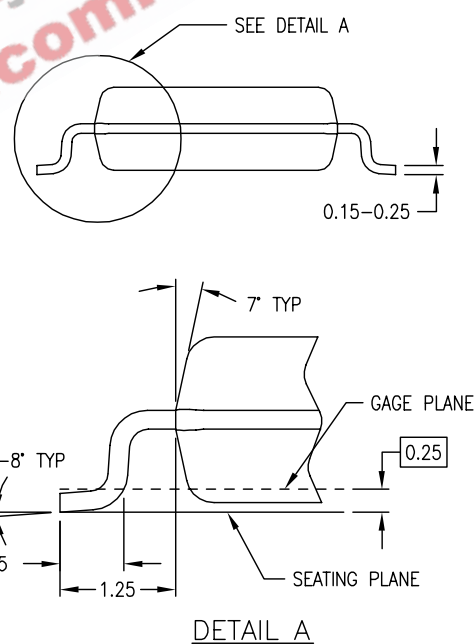
Dimensions are in millimeters unless otherwise noted.



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



M14DREVC

**Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M14D**



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FACT <sup>®</sup>	PACMAN <sup>™</sup>	SuperSOT <sup>™</sup> 3	
FAST <sup>®</sup>	PDP-SPM <sup>™</sup>	SuperSOT <sup>™</sup> 6	
FASTr <sup>™</sup>	POP <sup>™</sup>	SuperSOT <sup>™</sup> 8	
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Rev. 126