

74LVQ02 Low Voltage Quad 2-Input NOR Gate

General Description

The LVQ02 contains four 2-input NOR gates.

Features

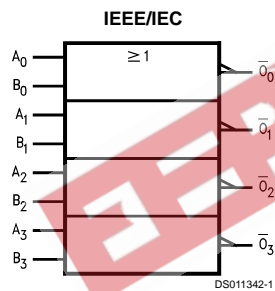
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

Ordering Code:

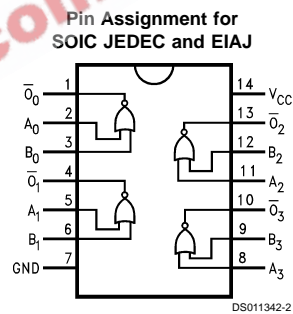
Order Number	Package Number	Package Description
74LVQ02SC	M14A	14-Lead (0.150" Wide) Molded Small Outline Integrated Circuit, SOIC JEDEC
74LVQ02SJ	M14D	14-Lead Small Outline Package, SOIC EIAJ

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	± 200 mA
Storage Temperature (T_{STG})	-65°C to +150°C
DC Latch-Up Source or Sink Current	± 100 mA

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC}) LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A) 74LVQ	-40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) V_{IN} from 0.8V to 2.0V V_{CC} @ 3.0V	125 mV/ns

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ C$		Units	Conditions
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	V	$I_{OUT} = -50 \mu A$
		3.0		2.58	V	$V_{IN} = V_{IL}$ or V_{IH} (Note 3) $I_{OH} = -12$ mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	V	$I_{OUT} = 50 \mu A$
		3.0		0.36	V	$V_{IN} = V_{IL}$ or V_{IH} (Note 3) $I_{OL} = 12$ mA
I_{IN}	Maximum Input Leakage Current	3.6		± 0.1	μA	$V_I = V_{CC}, GND$
I_{OLD}	Minimum Dynamic (Note 4) Output Current	3.6			mA	$V_{OLD} = 0.8V$ Max (Note 5)
I_{OHD}		3.6			mA	$V_{OHD} = 2.0V$ Min (Note 5)
I_{CC}	Maximum Quiescent Supply Current	3.6		2.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.6	1.0	V	(Notes 6, 7)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	-0.7	-1.0	V	(Notes 6, 7)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	V	(Notes 6, 8)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8	V	(Notes 6, 8)

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: Incident wave switching on transmission lines with impedances as low as 75 Ω for commercial temperature range is guaranteed for 74LVQ.

Note 6: Worst case package.

Note 7: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 8: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	2.7 3.3 ±0.3	1.5	6.0	10.6	1.0	12.0	ns
t _{PHL}	Propagation Delay	2.7 3.3 ±0.3	1.5	6.0	10.6	1.0	12.0	
t _{OSSL}	Output to Output Skew (Note 9)	2.7		1.0	1.5		1.5	ns
t _{OSLH}	Data to Output	3.3 ±0.3		1.0	1.5		1.5	

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSSL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

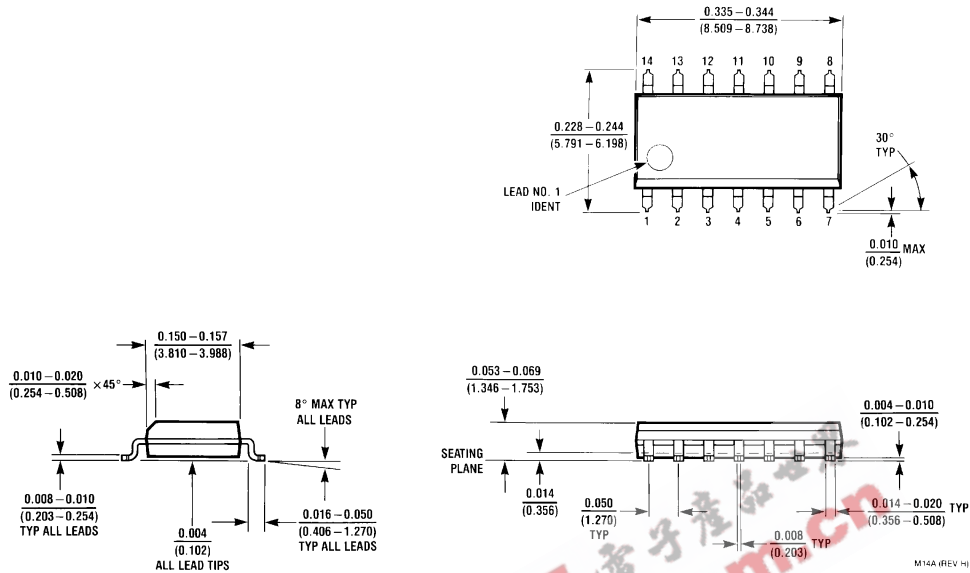
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 10)	Power Dissipation Capacitance	20	pF	V _{CC} = 3.3V

Note 10: C_{PD} is measured at 10 MHz.

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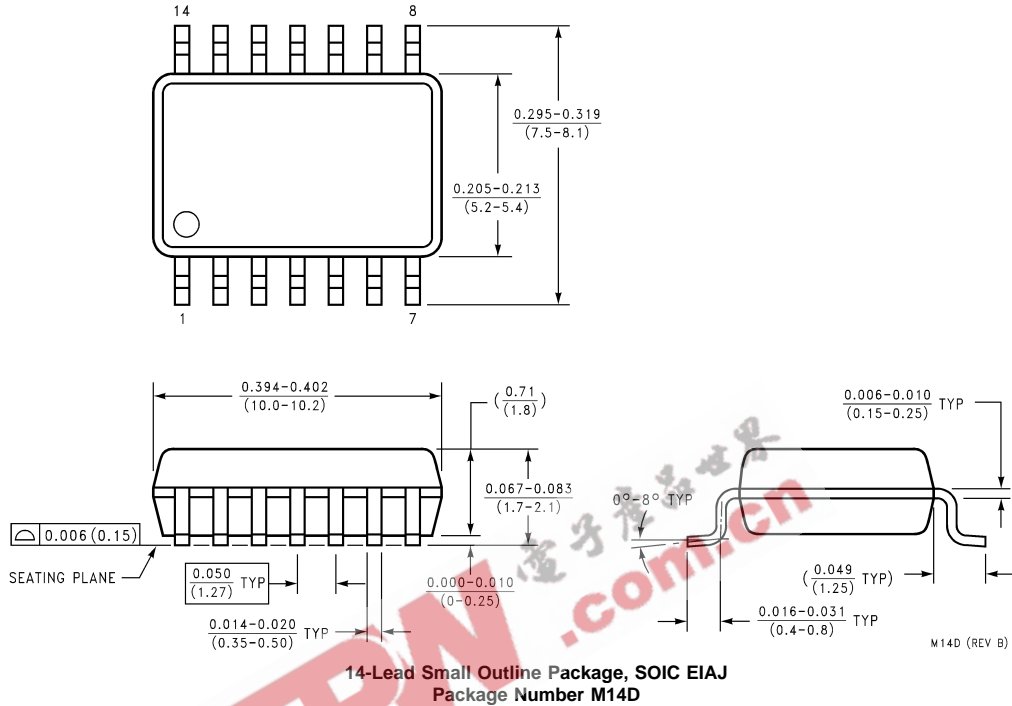
Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead (0.150" Wide) Molded Small Outline Integrated Circuit, SOIC JEDEC
Package Number M14A

M14A (REV. H)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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Fairchild Semiconductor Corporation Americas
Customer Response Center
Tel: 1-888-522-5372
Fax: 972-910-8036

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
8/F Room 808 Empire Centre
68 Mody Road, Tsimshatsui East
Kowloon, Hong Kong
Tel: 852-2722-8338
Fax: 852-2722-8383

Fairchild Semiconductor Japan Ltd.
4F, Natsume Bldg,
2-18-6 Yushima, Bunkyo-ku,
Tokyo 113-0034, Japan
Tel: 81-3-3818-8840
Fax: 81-3-3818-8450

www.fairchildsemi.com