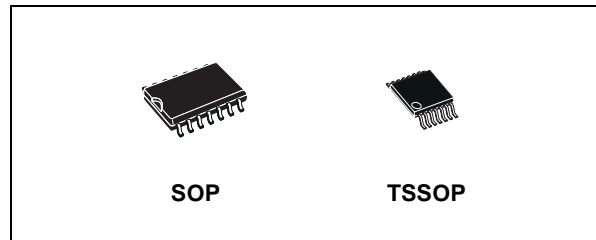


QUAD 2-INPUT NOR GATE

- HIGH SPEED: $t_{PD} = 3.6ns$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 2 \mu A$ (MAX.) at $T_A = 25^\circ C$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8mA$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(OPR) = 2V$ to $5.5V$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 02
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: $V_{OLP} = 0.8V$ (MAX.)



ORDER CODES

| PACKAGE | TUBE | T & R |
|---------|----------|------------|
| SOP | 74VHC02M | 74VHC02MTR |
| TSSOP | | 74VHC02TTR |

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

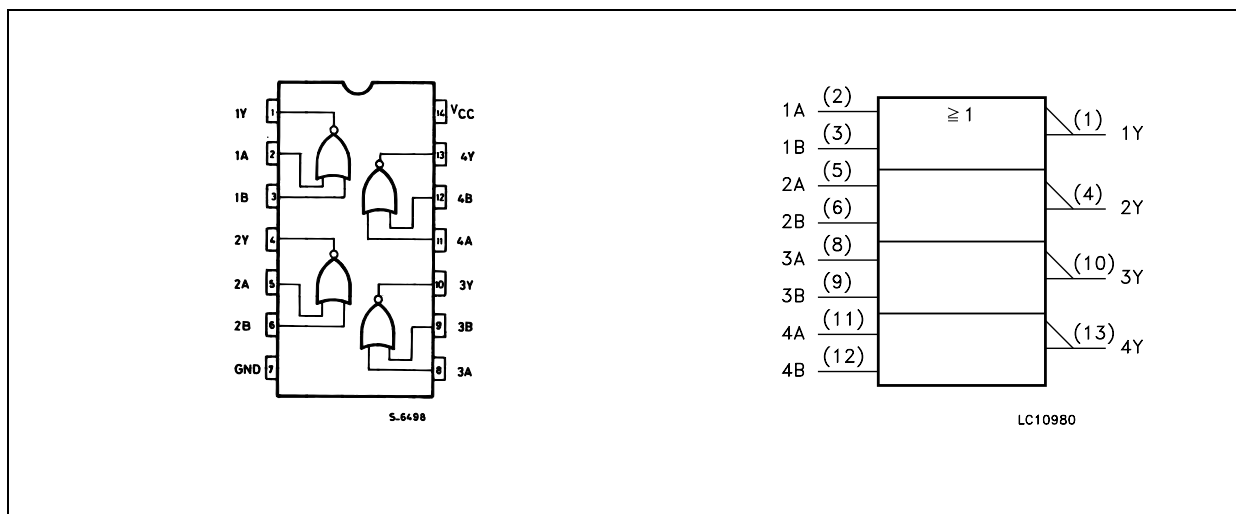
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

DESCRIPTION

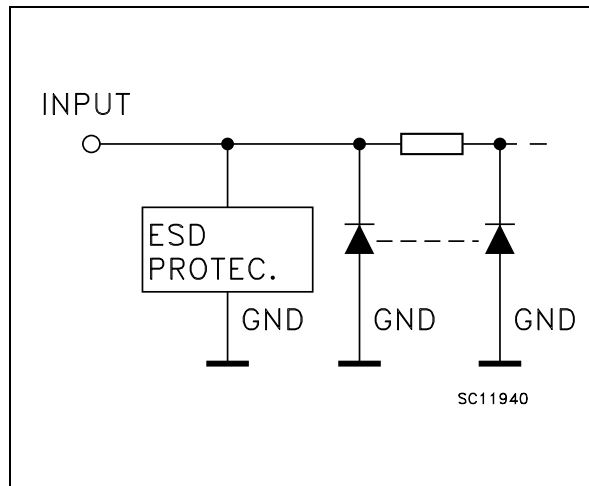
The 74VHC02 is an advanced high-speed CMOS QUAD 2-INPUT NOR GATE fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

The internal circuit is composed of 3 stages including buffer output, which provides high noise immunity and stable output.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

| PIN No | SYMBOL | NAME AND FUNCTION |
|--------------|-----------------|-------------------------|
| 2, 5, 8, 11 | 1A to 4A | Data Inputs |
| 3, 6, 9, 12 | 1B to 4B | Data Inputs |
| 1, 4, 10, 13 | 1Y to 4Y | Data Outputs |
| 7 | GND | Ground (0V) |
| 14 | V _{CC} | Positive Supply Voltage |

TRUTH TABLE

| A | B | Y |
|---|---|---|
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-------------------------------------|--------------------------------------|-------------------------------|------|
| V _{CC} | Supply Voltage | -0.5 to +7.0 | V |
| V _I | DC Input Voltage | -0.5 to +7.0 | V |
| V _O | DC Output Voltage | -0.5 to V _{CC} + 0.5 | V |
| I _{IK} | DC Input Diode Current | - 20 | mA |
| I _{OK} | DC Output Diode Current | ± 20 | mA |
| I _O | DC Output Current | ± 25 | mA |
| I _{CC} or I _{GND} | DC V _{CC} or Ground Current | ± 50 | mA |
| T _{stg} | Storage Temperature | -65 to +150 | °C |
| T _L | Lead Temperature (10 sec) | 300 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|-----------------|--|----------------------|------|
| V _{CC} | Supply Voltage | 2 to 5.5 | V |
| V _I | Input Voltage | 0 to 5.5 | V |
| V _O | Output Voltage | 0 to V _{CC} | V |
| T _{op} | Operating Temperature | -55 to 125 | °C |
| dt/dv | Input Rise and Fall Time (note 1) (V _{CC} = 3.3 ± 0.3V) (V _{CC} = 5.0 ± 0.5V) | 0 to 100 0 to 20 | ns/V |

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|-----------------|---------------------------|------------------------|---|-----------------------|------|--------------------|--------------------|--------------------|--------------------|--------------------|------|
| | | V _{CC} (V) | | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| V _{IH} | High Level Input Voltage | 2.0 | | 1.5 | | | 1.5 | | 1.5 | | V |
| | | 3.0 to 5.5 | | 0.7V _{CC} | | | 0.7V _{CC} | | 0.7V _{CC} | | |
| V _{IL} | Low Level Input Voltage | 2.0 | | | | 0.5 | | 0.5 | | 0.5 | V |
| | | 3.0 to 5.5 | | | | 0.3V _{CC} | | 0.3V _{CC} | | 0.3V _{CC} | |
| V _{OH} | High Level Output Voltage | 2.0 | I _O =-50 μA | 1.9 | 2.0 | | 1.9 | | 1.9 | | V |
| | | 3.0 | I _O =-50 μA | 2.9 | 3.0 | | 2.9 | | 2.9 | | |
| | | 4.5 | I _O =-50 μA | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | 3.0 | I _O =-4 mA | 2.58 | | | 2.48 | | 2.4 | | |
| | | 4.5 | I _O =-8 mA | 3.94 | | | 3.8 | | 3.7 | | |
| V _{OL} | Low Level Output Voltage | 2.0 | I _O =50 μA | | 0.0 | 0.1 | | 0.1 | | 0.1 | V |
| | | 3.0 | I _O =50 μA | | 0.0 | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 | I _O =50 μA | | 0.0 | 0.1 | | 0.1 | | 0.1 | |
| | | 3.0 | I _O =4 mA | | | 0.36 | | 0.44 | | 0.55 | |
| | | 4.5 | I _O =8 mA | | | 0.36 | | 0.44 | | 0.55 | |
| I _I | Input Leakage Current | 0 to 5.5 | V _I = 5.5V or GND | | | ± 0.1 | | ± 1 | | ± 1 | μA |
| I _{CC} | Quiescent Supply Current | 5.5 | V _I = V _{CC} or GND | | | 2 | | 20 | | 20 | μA |

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3ns)

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|-----------------------------------|------------------------|------------------------|------------------------|-----------------------|------|------|-------------|------|--------------|------|------|
| | | V _{CC} (V) | C _L (pF) | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| t _{PLH} t _{PHL} | Propagation Delay Time | 3.3 ^(*) | 15 | | 5.6 | 7.9 | 1.0 | 9.5 | 1.0 | 9.5 | ns |
| | | 3.3 ^(*) | 50 | | 8.1 | 11.4 | 1.0 | 13.0 | 1.0 | 13.0 | |
| | | 5.0 ^(**) | 15 | | 3.6 | 5.5 | 1.0 | 6.5 | 1.0 | 6.5 | |
| | | 5.0 ^(**) | 50 | | 4.5 | 7.5 | 1.0 | 8.5 | 1.0 | 8.5 | |

(*) Voltage range is 3.3V ± 0.3V

(**) Voltage range is 5.0V ± 0.5V

CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|-----------------|--|----------------|----|-----------------------|------|------|-------------|------|--------------|------|------|
| | | | | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| C _{IN} | Input Capacitance | | 6 | 10 | | 10 | | 10 | pF | | |
| C _{PD} | Power Dissipation Capacitance (note 1) | | 19 | | | | | | pF | | |

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$ (per gate)

DYNAMIC SWITCHING CHARACTERISTICS

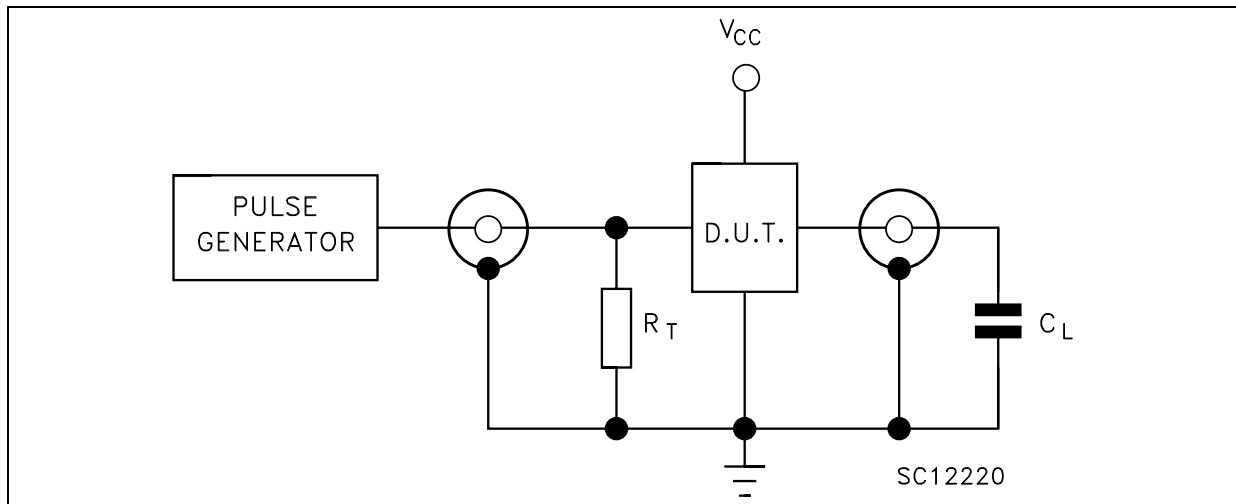
| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | | |
|------------------|--|----------------|------------------------|---------------------|-----------------------|------|------|-------------|------|------|--------------|------|
| | | | | V _{CC} (V) | T _A = 25°C | | | -40 to 85°C | | | -55 to 125°C | |
| | | | | | Min. | Typ. | Max. | Min. | Max. | | Min. | Max. |
| V _{OLP} | Dynamic Low Voltage Quiet Output (note 1, 2) | 5.0 | C _L = 50 pF | | 0.3 | 0.8 | | | | | V | |
| V _{OLV} | | | | -0.8 | -0.3 | | | | | | | |
| V _{IHD} | Dynamic High Voltage Input (note 1, 3) | 5.0 | | 3.5 | | | | | | V | | |
| V _{ILD} | Dynamic Low Voltage Input (note 1, 3) | 5.0 | | | 1.5 | | | | | V | | |

1) Worst case package.

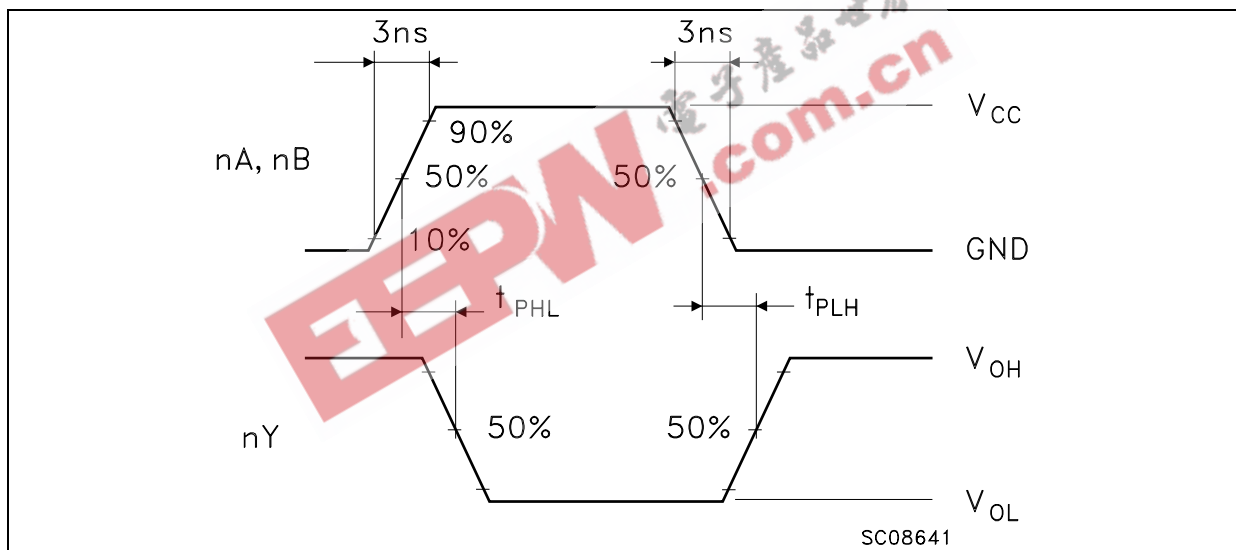
2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

TEST CIRCUIT

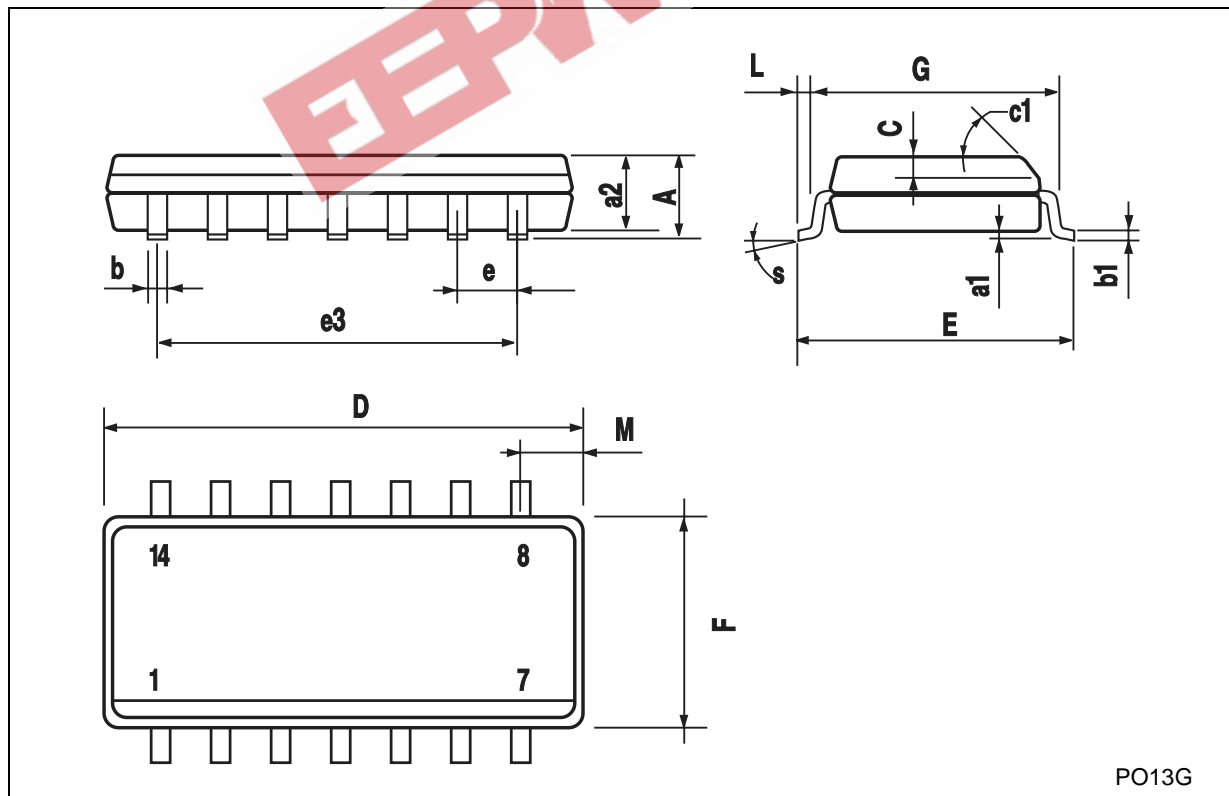


$C_L = 15/50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM: PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)

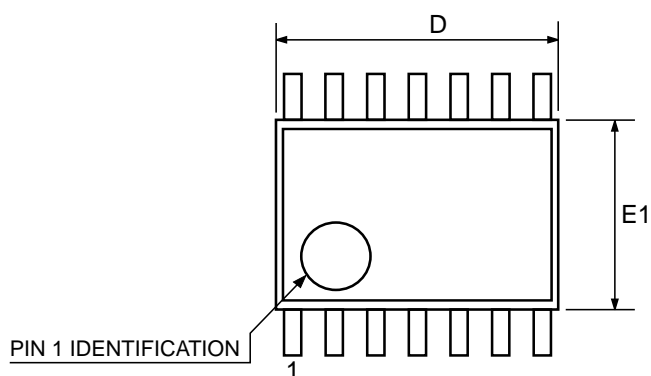
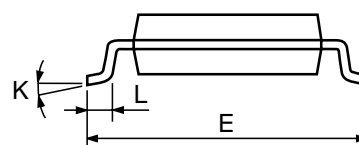
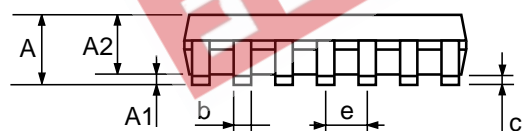
SO-14 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.068 |
| a1 | 0.1 | | 0.2 | 0.003 | | 0.007 |
| a2 | | | 1.65 | | | 0.064 |
| b | 0.35 | | 0.46 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.019 | |
| c1 | 45° (typ.) | | | | | |
| D | 8.55 | | 8.75 | 0.336 | | 0.344 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 7.62 | | | 0.300 | |
| F | 3.8 | | 4.0 | 0.149 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.208 |
| L | 0.5 | | 1.27 | 0.019 | | 0.050 |
| M | | | 0.68 | | | 0.026 |
| S | 8° (max.) | | | | | |



TSSOP14 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|----------|------|-------|------------|--------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0089 |
| D | 4.9 | 5 | 5.1 | 0.193 | 0.197 | 0.201 |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.48 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |



0080337D

EEPW 电子產品世界
.com.cn

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>