

# DATA SHEET

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**74LV03**

Quad 2-input NAND gate

Product specification  
Supersedes data of 1997 Mar 28  
IC24 Data Handbook

1998 Apr 20

## Quad 2-input NAND gate

74LV03

## FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between  $V_{CC} = 2.7V$  and  $V_{CC} = 3.6V$
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8V$  @  $V_{CC} = 3.3V$ ,  $T_{amb} = 25^{\circ}C$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2V$  @  $V_{CC} = 3.3V$ ,  $T_{amb} = 25^{\circ}C$
- Level shifter capability
- Output capability: standard (open drain)
- $I_{CC}$  category: SSI

## DESCRIPTION

The 74LV03 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT03.

The 74LV03 provides the 2-input NAND function.

The 74LV03 has open-drain N-transistor outputs, which are not clamped by a diode connected to  $V_{CC}$ . In the OFF-state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and  $V_{Omax}$ . This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

## QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^{\circ}C$ ;  $t_r = t_f \leq 2.5$  ns

| SYMBOL            | PARAMETER                              | CONDITIONS                      | TYPICAL | UNIT |
|-------------------|--|---------------------------------|---------|------|
| $t_{PZL}/t_{PLZ}$ | Propagation delay<br>nA, nB to nY      | $C_L = 15pF$<br>$V_{CC} = 3.3V$ | 8       | ns   |
| $C_I$             | Input capacitance                      |                                 | 3.5     | pF   |
| $C_{PD}$          | Power dissipation capacitance per gate | Notes 1, 2                      | 4       | pF   |

## NOTES:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
- The condition is  $V_I = GND$  to  $V_{CC}$
- The given value of  $C_{PD}$  is obtained with :  $C_L = 0$  pF and  $R_L = \infty$

## ORDERING INFORMATION

| PACKAGES                    | TEMPERATURE RANGE                 | OUTSIDE NORTH AMERICA | NORTH AMERICA | PKG. DWG. # |
|-----------------------------|-----------------------------------|-----------------------|---------------|-------------|
| 14-Pin Plastic DIL          | $-40^{\circ}C$ to $+125^{\circ}C$ | 74LV03 N              | 74LV03 N      | SOT27-1     |
| 14-Pin Plastic SO           | $-40^{\circ}C$ to $+125^{\circ}C$ | 74LV03 D              | 74LV03 D      | SOT108-1    |
| 14-Pin Plastic SSOP Type II | $-40^{\circ}C$ to $+125^{\circ}C$ | 74LV03 DB             | 74LV03 DB     | SOT337-1    |
| 14-Pin Plastic TSSOP Type I | $-40^{\circ}C$ to $+125^{\circ}C$ | 74LV03 PW             | 74LV03PW DH   | SOT402-1    |

## PIN DESCRIPTION

| PIN NUMBER   | SYMBOL   | FUNCTION                |
|--------------|----------|-------------------------|
| 1, 4, 9, 12  | 1A to 4A | Data inputs             |
| 2, 5, 10, 13 | 1B to 4B | Data inputs             |
| 3, 6, 8, 11  | 1Y to 4Y | Data outputs            |
| 7            | GND      | Ground (0V)             |
| 14           | $V_{CC}$ | Positive supply voltage |

## FUNCTION TABLE

| INPUTS |    | OUTPUT |
|--------|----|--------|
| nA     | nB | nY     |
| L      | L  | Z      |
| L      | H  | Z      |
| H      | L  | Z      |
| H      | H  | L      |

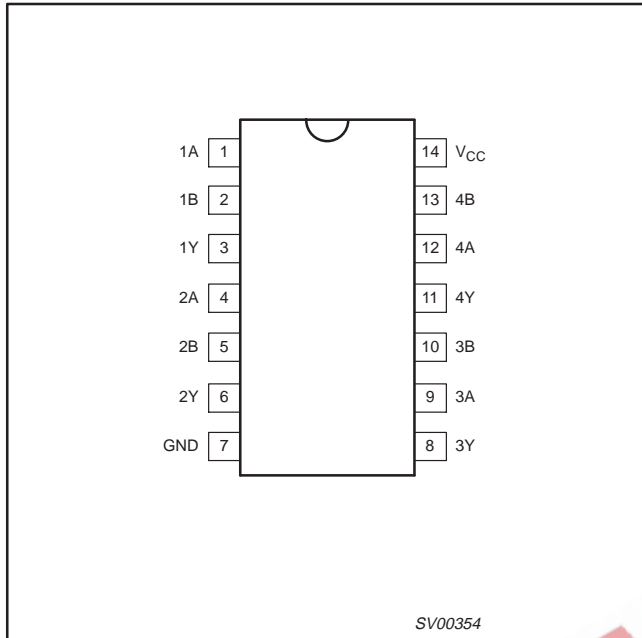
## NOTES:

H = HIGH voltage level  
 L = LOW voltage level  
 Z = High impedance OFF-state

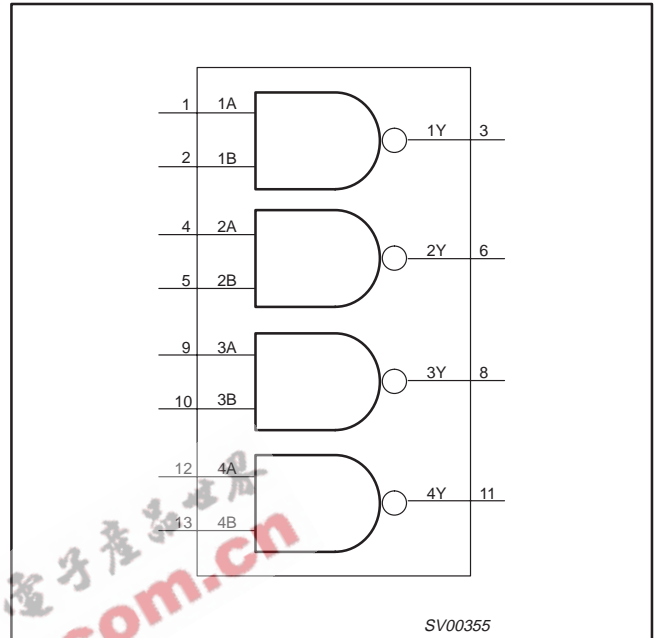
# Quad 2-input NAND gate

74LV03

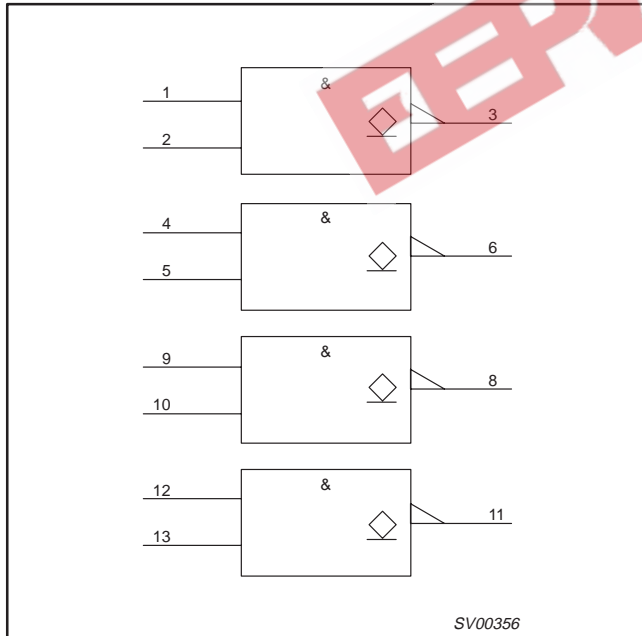
## PIN CONFIGURATION



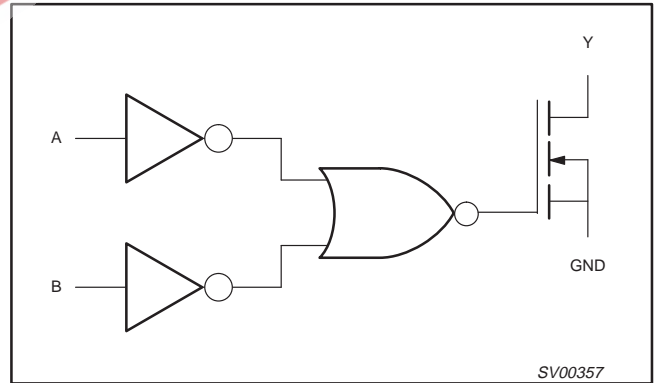
## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM



## Quad 2-input NAND gate

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## RECOMMENDED OPERATING CONDITIONS

| SYMBOL     | PARAMETER                                       | CONDITIONS   | MIN              | TYP.             | MAX                     | UNIT |
|------------|---|--|------------------|------------------|-------------------------|------|
| $V_{CC}$   | DC supply voltage                               | See Note1  | 1.0              | 3.3              | 5.5                     | V    |
| $V_I$      | Input voltage                                   |  | 0                | –                | $V_{CC}$                | V    |
| $V_O$      | Output voltage                                  |  | 0                | –                | $V_{CC}$                | V    |
| $T_{amb}$  | Operating ambient temperature range in free air | See DC and AC characteristics  | –40<br>–40       |                  | +85<br>+125             | °C   |
| $t_r, t_f$ | Input rise and fall times                       | $V_{CC} = 1.0V$ to $2.0V$<br>$V_{CC} = 2.0V$ to $2.7V$<br>$V_{CC} = 2.7V$ to $3.6V$<br>$V_{CC} = 3.6V$ to $5.5V$ | –<br>–<br>–<br>– | –<br>–<br>–<br>– | 500<br>200<br>100<br>50 | ns/V |

## NOTES:

1 The LV is guaranteed to function down to  $V_{CC} = 1.0V$  (input levels GND or  $V_{CC}$ ); DC characteristics are guaranteed from  $V_{CC} = 1.2V$  to  $V_{CC} = 5.5V$ .

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

| SYMBOL                    | PARAMETER  | CONDITIONS  | RATING            | UNIT |
|---------------------------|--|---|-------------------|------|
| $V_{CC}$                  | DC supply voltage  |   | –0.5 to +7.0      | V    |
| $\pm I_{IK}$              | DC input diode current   | $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$   | 20                | mA   |
| $\pm I_{OK}$              | DC output diode current  | $V_O < -0.5$ or $V_O > V_{CC} + 0.5V$   | 50                | mA   |
| $\pm I_O$                 | DC output source or sink current<br>– standard outputs   | $-0.5V < V_O < V_{CC} + 0.5V$   | 25                | mA   |
| $\pm I_{GND}, \pm I_{CC}$ | DC $V_{CC}$ or GND current for types with<br>–standard outputs   |   | 50                | mA   |
| $T_{stg}$                 | Storage temperature range  |   | –65 to +150       | °C   |
| $P_{TOT}$                 | Power dissipation per package<br>–plastic DIL<br>–plastic mini-pack (SO)<br>–plastic shrink mini-pack (SSOP and TSSOP) | for temperature range: –40 to +125°C<br>above +70°C derate linearly with 12mW/K<br>above +70°C derate linearly with 8 mW/K<br>above +60°C derate linearly with 5.5 mW/K | 750<br>500<br>400 | mW   |

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## Quad 2-input NAND gate

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**DC CHARACTERISTICS**

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

| SYMBOL           | PARAMETER                                     | TEST CONDITIONS   | LIMITS              |                  |                     |                     |                     | UNIT |
|------------------|---|---|---------------------|------------------|---------------------|---------------------|---------------------|------|
|                  |   |   | -40°C to +85°C      |                  |                     | -40°C to +125°C     |                     |      |
|                  |   |   | MIN                 | TYP <sup>1</sup> | MAX                 | MIN                 | MAX                 |      |
| V <sub>IH</sub>  | HIGH level Input voltage                      | V <sub>CC</sub> = 1.2V  | 0.9                 |                  |                     | 0.9                 |                     | V    |
|                  |   | V <sub>CC</sub> = 2.0V  | 1.4                 |                  |                     | 1.4                 |                     |      |
|                  |   | V <sub>CC</sub> = 2.7 to 3.6V   | 2.0                 |                  |                     | 2.0                 |                     |      |
|                  |   | V <sub>CC</sub> = 4.5 to 5.5V   | 0.7*V <sub>CC</sub> |                  |                     | 0.7*V <sub>CC</sub> |                     |      |
| V <sub>IL</sub>  | LOW level Input voltage                       | V <sub>CC</sub> = 1.2V  |                     |                  | 0.3                 |                     | 0.3                 | V    |
|                  |   | V <sub>CC</sub> = 2.0V  |                     |                  | 0.6                 |                     | 0.6                 |      |
|                  |   | V <sub>CC</sub> = 2.7 to 3.6V   |                     |                  | 0.8                 |                     | 0.8                 |      |
|                  |   | V <sub>CC</sub> = 4.5 to 5.5  |                     |                  | 0.3*V <sub>CC</sub> |                     | 0.3*V <sub>CC</sub> |      |
| V <sub>OH</sub>  | HIGH level output voltage; all outputs        | V <sub>CC</sub> = 1.2V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100μA     |                     | 1.2              |                     |                     |                     | V    |
|                  |   | V <sub>CC</sub> = 2.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100μA     | 1.8                 | 2.0              |                     | 1.8                 |                     |      |
|                  |   | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100μA     | 2.5                 | 2.7              |                     | 2.5                 |                     |      |
|                  |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100μA     | 2.8                 | 3.0              |                     | 2.8                 |                     |      |
|                  |   | V <sub>CC</sub> = 4.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100μA     | 4.3                 | 4.5              |                     | 4.3                 |                     |      |
| V <sub>OH</sub>  | HIGH level output voltage; STANDARD outputs   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 6mA       | 2.40                | 2.82             |                     | 2.20                |                     | V    |
|                  |   | V <sub>CC</sub> = 4.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 12mA      | 3.60                | 4.20             |                     | 3.50                |                     |      |
| V <sub>OL</sub>  | LOW level output voltage; all outputs         | V <sub>CC</sub> = 1.2V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA      |                     | 0                |                     |                     |                     | V    |
|                  |   | V <sub>CC</sub> = 2.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA      |                     | 0                | 0.2                 |                     | 0.2                 |      |
|                  |   | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA      |                     | 0                | 0.2                 |                     | 0.2                 |      |
|                  |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA      |                     | 0                | 0.2                 |                     | 0.2                 |      |
|                  |   | V <sub>CC</sub> = 4.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA      |                     | 0                | 0.2                 |                     | 0.2                 |      |
| V <sub>OL</sub>  | LOW level output voltage; STANDARD outputs    | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA        |                     | 0.25             | 0.40                |                     | 0.50                | V    |
|                  |   | V <sub>CC</sub> = 4.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA       |                     | 0.35             | 0.55                |                     | 0.65                |      |
| I <sub>OZ</sub>  | HIGH level output leakage current             | V <sub>CC</sub> = 2.0 to 3.6V; V <sub>I</sub> = V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND |                     |                  | 5.0                 |                     | 10                  | μA   |
| I <sub>OZ</sub>  | HIGH level output leakage current             | V <sub>CC</sub> = 2.0 to 3.6V; V <sub>I</sub> = V <sub>IL</sub> ; V <sub>O</sub> = 6.0V <sup>2</sup>      |                     |                  | 10                  |                     | 20                  | μA   |
| I <sub>I</sub>   | Input leakage current                         | V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub> or GND   |                     |                  | 1.0                 |                     | 1.0                 | μA   |
| I <sub>CC</sub>  | Quiescent supply current; SSI                 | V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0                       |                     |                  | 20.0                |                     | 40                  | μA   |
| ΔI <sub>CC</sub> | Additional quiescent supply current per input | V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V                                   |                     |                  | 500                 |                     | 850                 | μA   |

**NOTES:**

- All typical values are measured at T<sub>amb</sub> = 25°C.
- The maximum operating output voltage (V<sub>O(max)</sub>) is 6.0V.

# Quad 2-input NAND gate

74LV03

## AC CHARACTERISTICS FOR 74LV03

GND = 0V;  $t_r = t_f \leq 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 1\text{K}\Omega$

| SYMBOL                  | PARAMETER                          | WAVEFORM      | CONDITION  | LIMITS<br>-40 to +85 °C |                 |                  | LIMITS<br>-40 to +125 °C |     | UNIT |
|-------------------------|------------------------------------|---------------|------------|-------------------------|-----------------|------------------|--------------------------|-----|------|
|                         |                                    |               |            | $V_{CC}(V)$             | MIN             | TYP <sup>1</sup> | MAX                      | MIN |      |
| $t_{PZL}/\hat{t}_{PLZ}$ | Propagation delay<br>nA, nB, to nY | Figures, 1, 2 | 1.2        | -                       | 50              | -                | -                        | -   | ns   |
|                         |                                    |               | 2.0        | -                       | 17              | 26               | -                        | 31  |      |
|                         |                                    |               | 2.7        | -                       | 13              | 19               | -                        | 23  |      |
|                         |                                    |               | 3.0 to 3.6 | -                       | 10 <sup>2</sup> | 16               | -                        | 19  |      |
|                         |                                    |               | 4.5 to 5.5 | -                       | - <sup>3</sup>  | 13               | -                        | 16  |      |

**NOTE:**

- 1 Unless otherwise stated, all typical values are at  $T_{amb} = 25^\circ\text{C}$ .
- 2 Typical value measured at  $V_{CC} = 3.3\text{V}$ .
- 3 Typical value measured at  $V_{CC} = 5.0\text{V}$ .

## AC WAVEFORMS

$V_M = 1.5\text{V}$  at  $V_{CC} \geq 2.7\text{V} \leq 3.6\text{V}$

$V_M = 0.5 * V_{CC}$  at  $V_{CC} < 2.7\text{V}$  and  $\geq 4.5\text{V}$

$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

$V_X = V_{OL} + 0.3\text{V}$  at  $V_{CC} \geq 2.7\text{V}$  and  $\leq 3.6\text{V}$

$V_X = V_{OL} + 0.1 * V_{CC}$  at  $V_{CC} < 2.7\text{V}$  and  $\geq 4.5\text{V}$

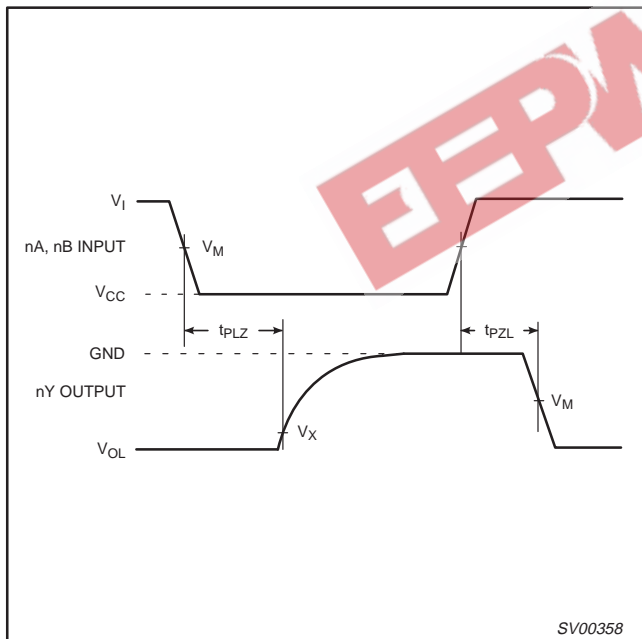
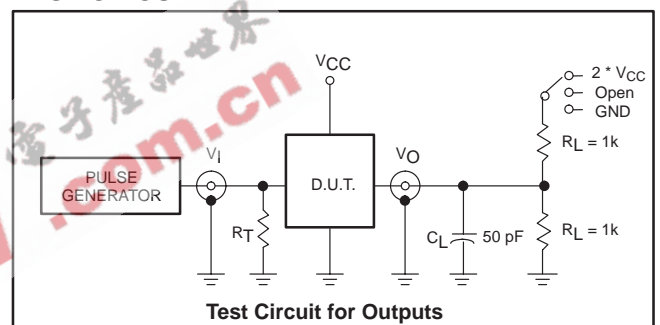


Figure 1. Input (nA, nB) to output (nY) propagation delays.

## TEST CIRCUIT



**DEFINITIONS**

- $R_L$  = Load resistor
- $C_L$  = Load capacitance includes jig and probe capacitance.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

**SWITCH POSITION**

| TEST                    | $S_1$        | $V_{CC}$           | $V_I$    |
|-------------------------|--------------|--------------------|----------|
| $t_{PLH}/\hat{t}_{PHL}$ | Open         | < 2.7V             | $V_{CC}$ |
| $t_{PLZ}/\hat{t}_{PZL}$ | $2 * V_{CC}$ | 2.7-3.6V           | 2.7V     |
| $t_{PHZ}/\hat{t}_{PZH}$ | GND          | $\geq 4.5\text{V}$ | $V_{CC}$ |

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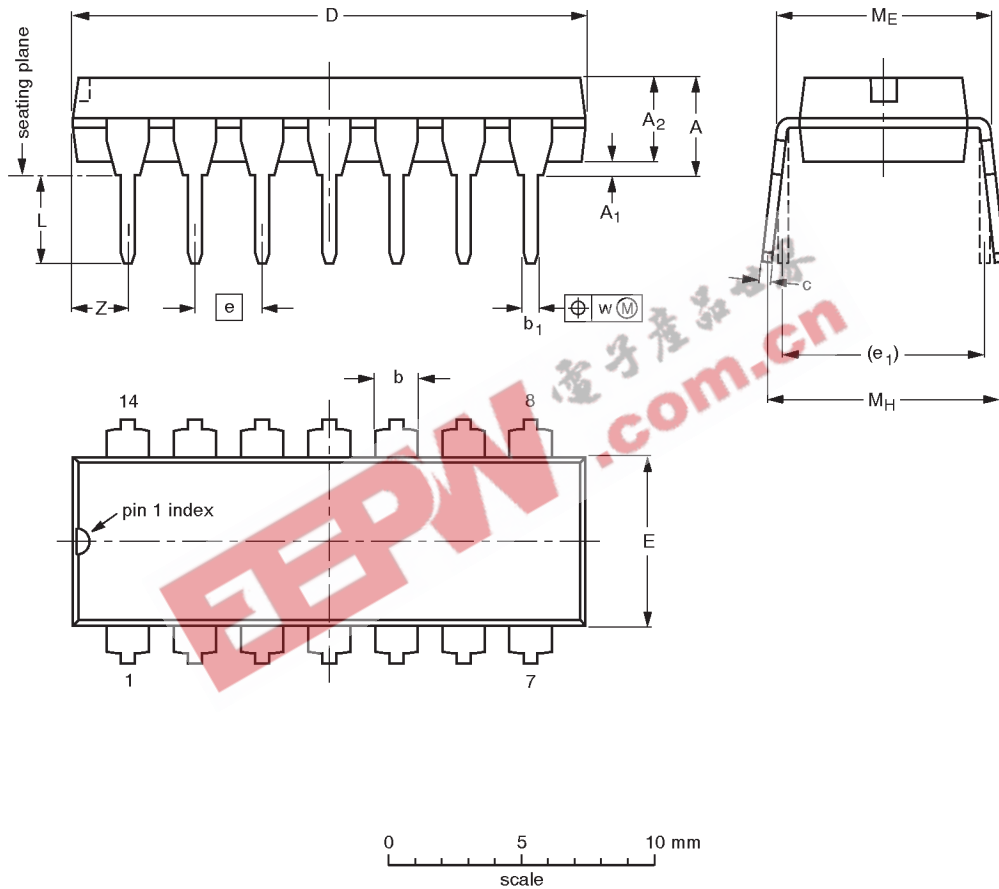
Figure 2. Load circuitry for switching times

Quad 2-input NAND gate

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub> min. | A <sub>2</sub> max. | b              | b <sub>1</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>1</sub> | L            | M <sub>E</sub> | M <sub>H</sub> | w     | Z <sup>(1)</sup> max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm     | 4.2    | 0.51                | 3.2                 | 1.73<br>1.13   | 0.53<br>0.38   | 0.36<br>0.23   | 19.50<br>18.55   | 6.48<br>6.20     | 2.54 | 7.62           | 3.60<br>3.05 | 8.25<br>7.80   | 10.0<br>8.3    | 0.254 | 2.2                   |
| inches | 0.17   | 0.020               | 0.13                | 0.068<br>0.044 | 0.021<br>0.015 | 0.014<br>0.009 | 0.77<br>0.73     | 0.26<br>0.24     | 0.10 | 0.30           | 0.14<br>0.12 | 0.32<br>0.31   | 0.39<br>0.33   | 0.01  | 0.087                 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

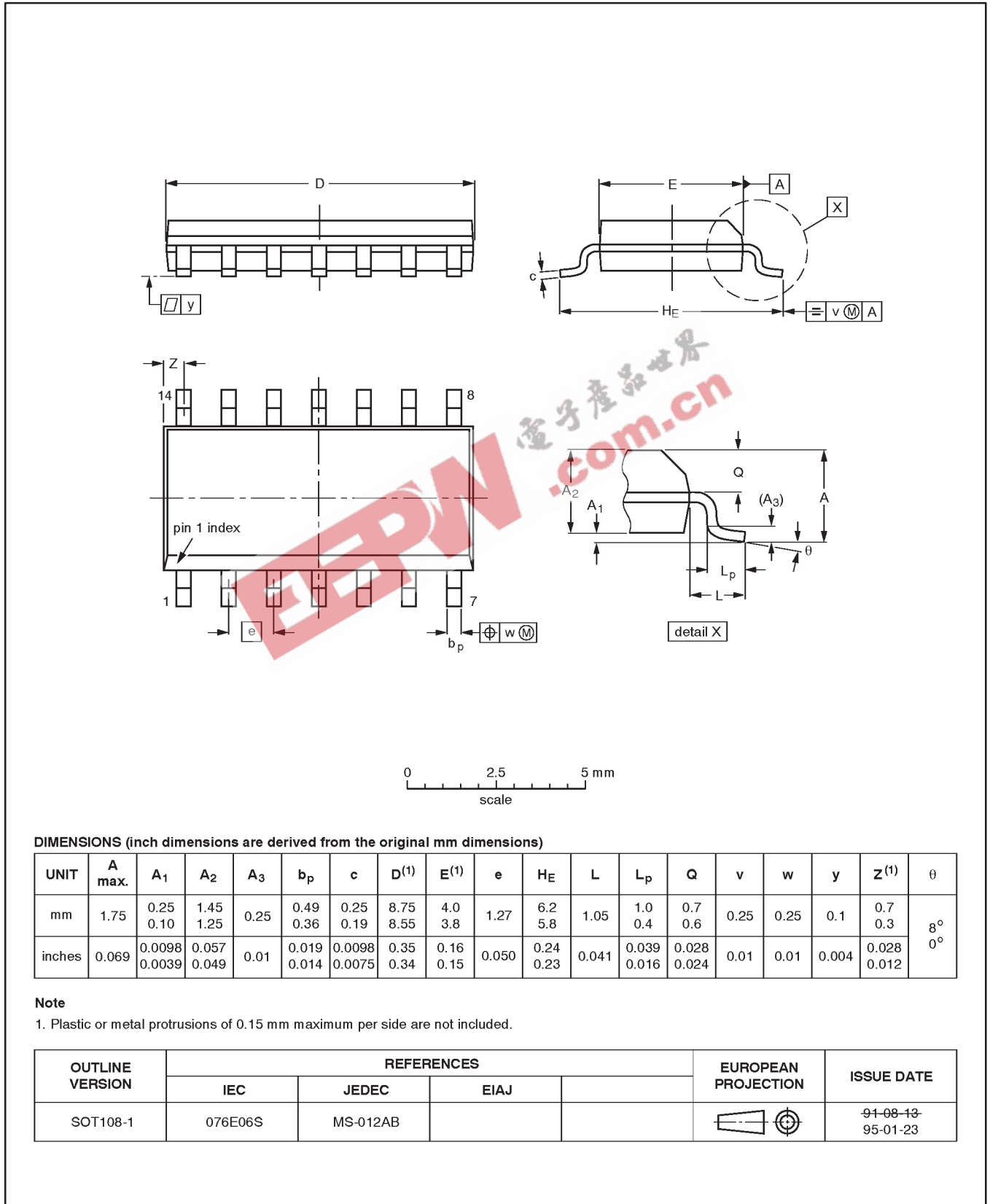
| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT27-1         | 050G04     | MO-001AA |      |  |                     | 92-11-17<br>95-03-11 |

Quad 2-input NAND gate

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub>   | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c                | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | z <sup>(1)</sup> | θ        |
|--------|--------|------------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 1.75   | 0.25<br>0.10     | 1.45<br>1.25   | 0.25           | 0.49<br>0.36   | 0.25<br>0.19     | 8.75<br>8.55     | 4.0<br>3.8       | 1.27  | 6.2<br>5.8     | 1.05  | 1.0<br>0.4     | 0.7<br>0.6     | 0.25 | 0.25 | 0.1   | 0.7<br>0.3       | 8°<br>0° |
| inches | 0.069  | 0.0098<br>0.0039 | 0.057<br>0.049 | 0.01           | 0.019<br>0.014 | 0.0098<br>0.0075 | 0.35<br>0.34     | 0.16<br>0.15     | 0.050 | 0.24<br>0.23   | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012   |          |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT108-1        | 076E06S    | MS-012AB |      |  |                     | 91-08-13<br>95-01-23 |

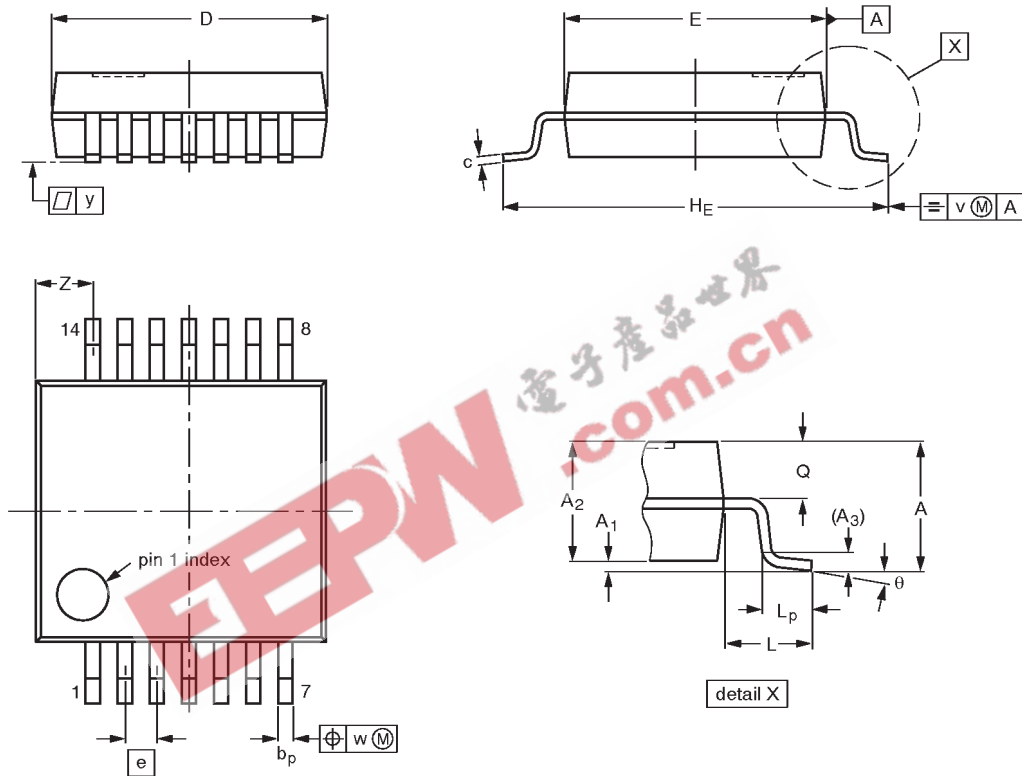


Quad 2-input NAND gate

74LV03

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | H <sub>E</sub> | L    | L <sub>p</sub> | Q          | v   | w    | y   | z <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm   | 2.0    | 0.21<br>0.05   | 1.80<br>1.65   | 0.25           | 0.38<br>0.25   | 0.20<br>0.09 | 6.4<br>6.0       | 5.4<br>5.2       | 0.65 | 7.9<br>7.6     | 1.25 | 1.03<br>0.63   | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.4<br>0.9       | 8°<br>0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

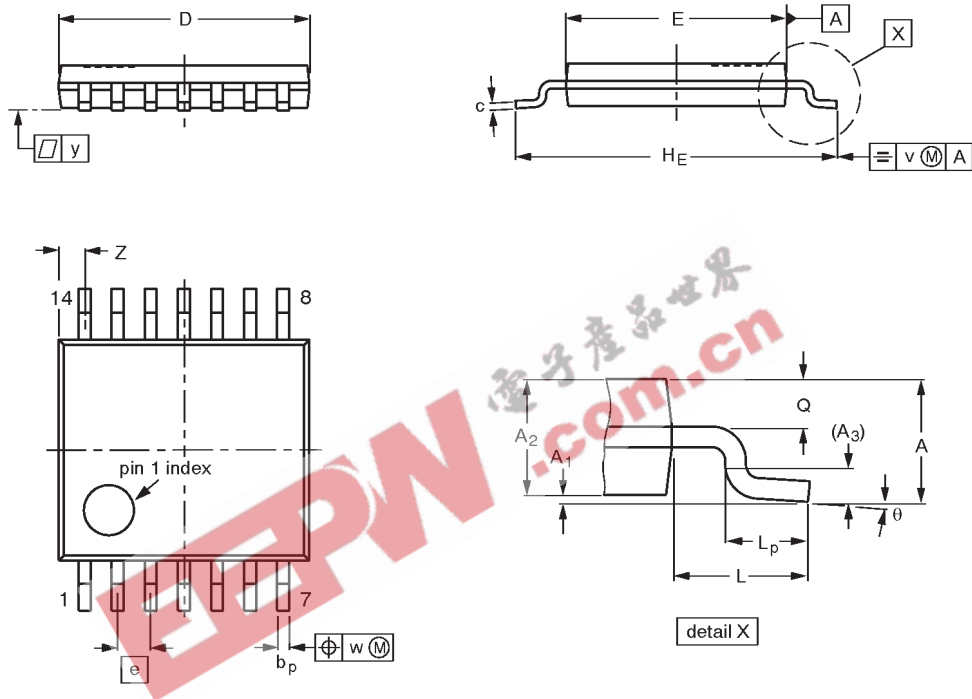
| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE                      |
|-----------------|------------|----------|------|--|---------------------|---------------------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                                 |
| SOT337-1        |            | MO-150AB |      |  |                     | <del>95-02-04</del><br>96-01-18 |

Quad 2-input NAND gate

74LV03

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c          | D <sup>(1)</sup> | E <sup>(2)</sup> | e    | H <sub>E</sub> | L   | L <sub>p</sub> | Q          | v   | w    | y   | Z <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|-----|----------------|------------|-----|------|-----|------------------|----------|
| mm   | 1.10   | 0.15<br>0.05   | 0.95<br>0.80   | 0.25           | 0.30<br>0.19   | 0.2<br>0.1 | 5.1<br>4.9       | 4.5<br>4.3       | 0.65 | 6.6<br>6.2     | 1.0 | 0.75<br>0.50   | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.72<br>0.38     | 8°<br>0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |        |      |  | EUROPEAN PROJECTION | ISSUE DATE             |
|-----------------|------------|--------|------|--|---------------------|------------------------|
|                 | IEC        | JEDEC  | EIAJ |  |                     |                        |
| SOT402-1        |            | MO-153 |      |  |                     | -94-07-12-<br>95-04-04 |

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Quad 2-input NAND gate

74LV03

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NOTES



## Quad 2-input NAND gate

74LV03

## Data sheet status

| Data sheet status         | Product status | Definition [1]   |
|---------------------------|----------------|--|
| Objective specification   | Development    | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.  |
| Preliminary specification | Qualification  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification     | Production     | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.   |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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