INTEGRATED CIRCUITS

DATA SHEET



74F02Quad 2-input NOR gate

Product specification

1990 Oct 04

IC15 Data Handbook





Quad 2-input NOR gate

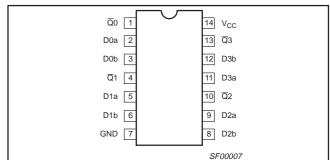
74F02

FEATURE

• Industrial temperature range available (-40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F02	3.4ns	4.4mA

PIN CONFIGURATION



ORDERING INFORMATION

	O	RDER CODE	
DESCRIPTION	COMMERCIAL RANGE V _{CC} = 5V ±10%, T _{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = -40°C to +85°C	PKG DWG #
14-pin plastic DIP	N74F02N	174F02N	SOT27-1
14-pin plastic SO	N74F02D	174F02D	SOT108-1

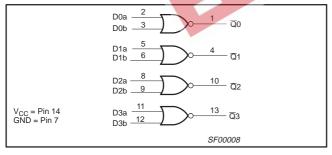
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION		74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs		1.0/1.0	20μA/0.6mA
Qn	Data output		50/33	1.0mA/20mA

NOTE:

One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

LOGIC DIAGRAM



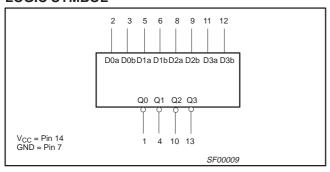
FUNCTION TABLE

INP	JTS	OUTPUT
Dna	Dnb	Ūn
L	L	Н
L	Н	L
Н	L	L
Н	Н	L

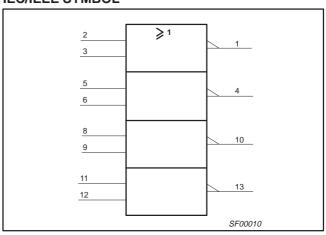
NOTES:

- 1 H = High voltage level
- 2 L = Low voltage level

LOGIC SYMBOL



IEC/IEEE SYMBOL



Quad 2-input NOR gate

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V _{CC}	Supply voltage		-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V	
I _{IN}	Input current	−30 to +5	mA	
V _{OUT}	Voltage applied to output in high output state		−0.5 to V _{CC}	V
I _{OUT}	Current applied to output in low output state		40	mA
T _{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T _{stg}	Storage temperature range	-65 to +150	°C	

RECOMMENDED OPERATING CONDITIONS

	ENDED OPERATING CONDITIONS			4				
SYMBOL	PARAMETER			3 35 11	LIMITS		UNIT	
			. A.	MIN	NOM	MAX		
V _{CC}	Supply voltage	96	3	4.5	5.0	5.5	V	
V_{IH}	High-level input voltage	1,3	-0	2.0			V	
V_{IL}	Low-level input voltage		0			0.8	V	
I _{lk}	Input clamp current					-18	mA	
I _{OH}	High-level output current					-1	mA	
I _{OL}	Low-level output current					20	mA	
T _{amb}	Operating free air temperature range	Commerc	al range	0		+70	°C	
		Industria	l range	-40		+85	°C	

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIO	NS ¹		LIMITS		UNIT	
					MIN	TYP ²	MAX		
V _{OH}	High-level output voltage		$V_{CC} = MIN, V_{IL} = MAX$	±10%V _{CC}	2.5			V	
			$V_{IH} = MIN, I_{OH} = MAX$ $\pm 5\% V_{CC}$		2.7	3.4		V	
V _{OL}	Low-level output voltage		$V_{CC} = MIN, V_{IL} = MAX$	±10%V _{CC}		0.30	0.50	V	
			$V_{IH} = MIN, I_{OI} = MAX$	±5%V _{CC}		0.30	0.50	V	
V _{IK}	Input clamp voltage		$V_{CC} = MIN, I_I = I_{IK}$		-0.73	-1.2	V		
I _I	Input current at maximum voltage	input	$V_{CC} = MAX, V_I = 7.0V$				100	μА	
I _{IH}	High-level input current		$V_{CC} = MAX, V_I = 2.7V$				20	μΑ	
I _{IL}	Low-level input current		$V_{CC} = MAX, V_I = 0.5V$				-0.6	mA	
los	Short-circuit output currer	ıt ³	V _{CC} = MAX		-60		-150	mA	
I _{CC}	Supply current (total) ⁴	I _{CCH}	V _{CC} = MAX			3.0	5.6	mA	
	I _{CCL}		$V_{CC} = MAX$			7.0	13.0	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V$, $T_{amb} = 25^{\circ}C$. Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

4 I_{CC} is measured with outputs open.

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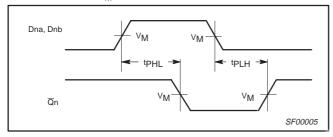
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AC ELECTRICAL CHARACTERISTICS

			LIMITS									
SYMBOL	PARAMETER	TEST CONDITION	Tai	_{CC} = +5.0 _{mb} = +25 0pF, R _L =	°C	T _{amb} = 0°0	0V ± 10% C to +70°C R _L = 500Ω	$T_{amb} = -40^\circ$	0V ± 10% °C to +85°C R _L = 500Ω	UNIT		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t _{PLH}	Propagation delay Dna, Dnb to Qn	Waveform 1	2.5 2.0	4.4 3.2	5.5 4.3	2.5 2.0	6.5 5.3	2.5 1.5	7.0 6.0	ns		

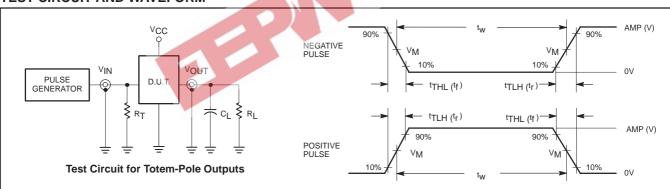
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.



Waveform 1. Propagation delay for inverting outputs

TEST CIRCUIT AND WAVEFORM



DEFINITIONS:

R_L = Load resistor;

see AC ELECTRICAL CHARACTERISTICS for value.

CL = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INP	UT PU	LSE REQU	IREMEN	TS	
lailily	amplitude	V_{M}	rep. rate	t _w	t _{TLH}	t _{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

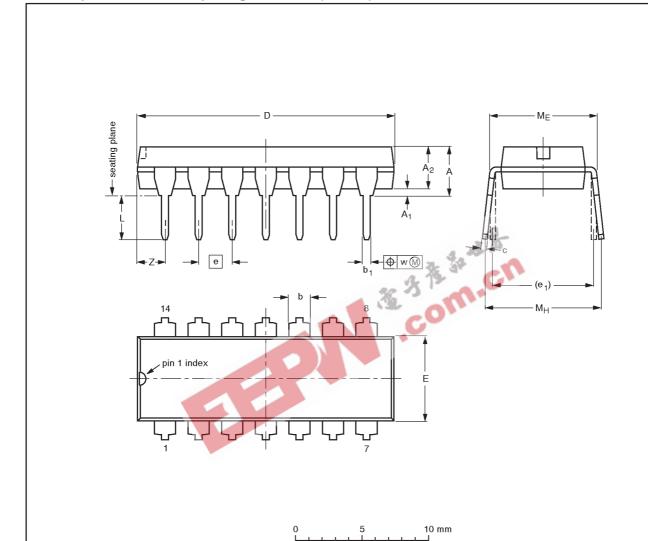
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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

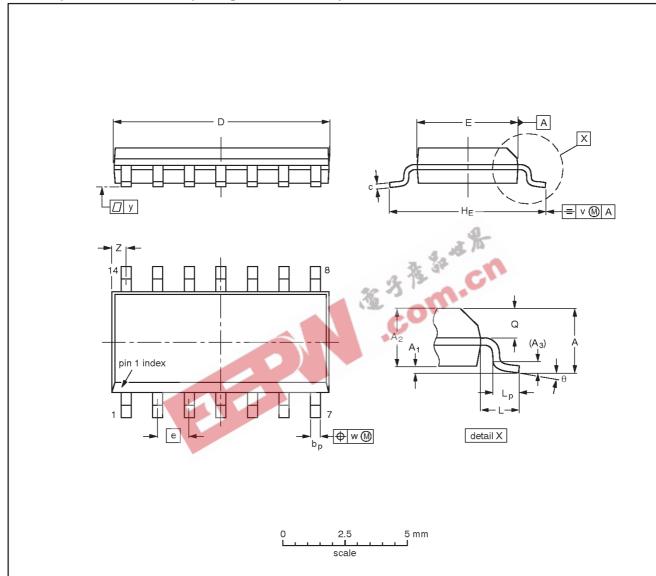
OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	EIAJ	PROJECTION	1930E DATE	
SOT27-1	050G04	MO-001AA			92-11-17 95-03-11	

Quad 2-input NOR gate

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
SOT108-1	076E06S	MS-012AB			95-01-23 97-05-22	

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NOTES

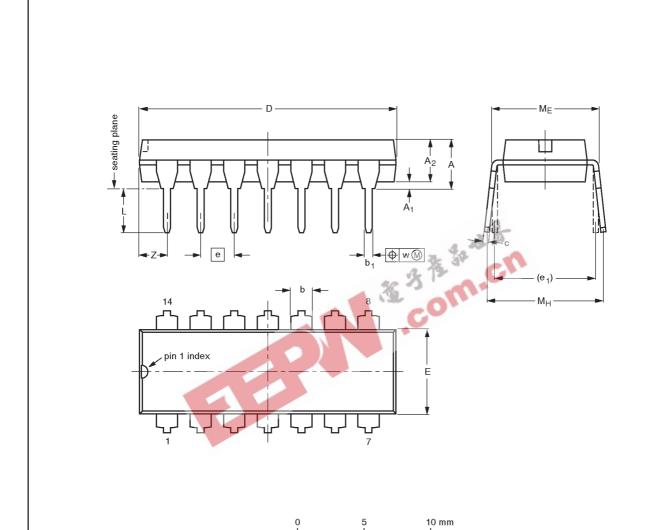


Quad 2-input NOR gate

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

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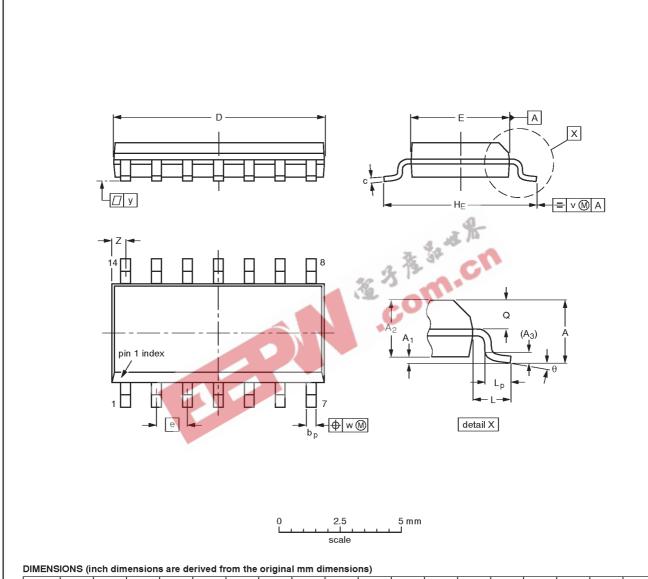
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SO14: plastic small outline package; 14 leads; body width 3.9 mm

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UNIT	A max.	A ₁	A ₂	A ₃	bp	ပ	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	٧	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.0098 0.0039		0.01	1	0.0098 0.0075		0.16 0.15	0.050	0.24 0.23	0.041		0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

Note

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OUTLINE		REFER	EUROPEAN	ISSUE DATE			
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SOT108-1	076E06\$	MS-012AB				91-08-13- 95-01-23	

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NOTES



Quad 2-input NOR gate

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		SEI INTIONS
Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
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