

## 74VHCT00A Quad 2-Input NAND Gate

### General Description

The VHCT00A is an advanced high-speed CMOS 2-Input NAND Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages, including buffer output, which provide high noise immunity and stable output.

Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the supply voltage and to the output pins with  $V_{CC} = 0V$ . These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3V to 5V systems and two supply systems such as battery backup.

### Features

- High speed:  $t_{PD} = 5.0$  ns (typ) at  $T_A = 25^\circ C$
- High noise immunity:  $V_{IH} = 2.0V$ ,  $V_{IL} = 0.8V$
- Power down protection is provided on all inputs and outputs
- Low noise:  $V_{OLP} = 0.8V$  (max)
- Low power dissipation:  
 $I_{CC} = 2 \mu A$  (max) at  $T_A = 25^\circ C$
- Pin and function compatible with 74HCT00

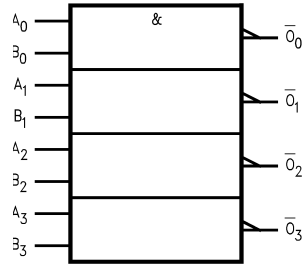
### Ordering Code:

Order Number	Package Number	Package Description
74VHCT00AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHCT00ASJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHCT00AMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHCT00AMTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHCT00AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74VHCT00AN_NL (Note 1)	N14A	Pb-Free 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

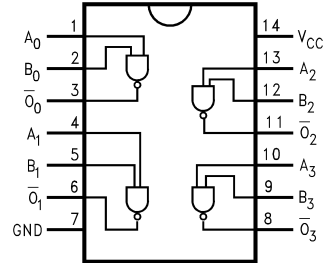
Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

**Note 1:** "\_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Use this number to order device.

**Logic Symbol**



**Connection Diagram**



**Pin Descriptions**

Pin Names	Description
$A_n, B_n$	Inputs
$\bar{O}_n$	Outputs

**Truth Table**

A	B	$\bar{O}$
L	L	H
L	H	H
H	L	H
H	H	L

**Absolute Maximum Ratings** (Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +7.0V
DC Output Voltage ( $V_{OUT}$ ) (Note 3)	-0.5V to $V_{CC} + 0.5V$
(Note 4)	-0.5V to 7.0V
Input Diode Current ( $I_{IK}$ )	-20 mA
Output Diode Current ( $I_{OK}$ ) (Note 5)	$\pm 20$ mA
DC Output Current ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}/GND$ Current ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Lead Temperature ( $T_L$ ) (Soldering, 10 seconds)	260°C

**Recommended Operating Conditions** (Note 6)

Supply Voltage ( $V_{CC}$ )	4.5V to 5.5V
Input Voltage ( $V_{IN}$ )	0V to +5.5V
Output Voltage ( $V_{OUT}$ ) (Note 3)	0V to $V_{CC}$
(Note 4)	0V to 5.5V
Operating Temperature ( $T_{OPR}$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ ) $V_{CC} = 5.0V \pm 0.5V$	0 ns/V ~ 20 ns/V

**Note 2:** Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

**Note 3:** HIGH or LOW state.  $I_{OUT}$  absolute maximum rating must be observed.

**Note 4:**  $V_{CC} = 0V$ .

**Note 5:**  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$  (Outputs Active)

**Note 6:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions
			Min	Typ	Max	Min	Max		
$V_{IH}$	HIGH Level Input Voltage	4.5	2.0			2.0		V	
		5.5	2.0			2.0			
$V_{IL}$	LOW Level Input Voltage	4.5		0.8			0.8	V	
		5.5		0.8			0.8		
$V_{OH}$	HIGH Level Output Voltage	4.5	4.40	4.50		4.40		V	$V_{IN} = V_{IH}$ or $V_{IL}$
		4.5	3.94			3.80			
$V_{OL}$	LOW Level Output Voltage	4.5		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or $V_{IL}$
		4.5			0.36		0.44		
$I_{IN}$	Input Leakage Current	0 – 5.5			$\pm 0.1$		$\pm 1.0$	$\mu A$	$V_{IN} = 5.5V$ or GND
$I_{CC}$	Quiescent Supply Current	5.5			2.0		20.0	$\mu A$	$V_{IN} = V_{CC}$ or GND
$I_{CCT}$	Maximum $I_{CC}/$ Input	5.5			1.35		1.50	mA	$V_{IN} = 3.4V$ Other Inputs = $V_{CC}$ or GND
$I_{OFF}$	Output Leakage Current (Power Down State)	0.0			0.5		5.0	$\mu A$	$V_{OUT} = 5.5V$

**Noise Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ C$		Units	Conditions
			Typ	Limit		
$V_{OLP}$ (Note 7)	Quiet Output Maximum Dynamic $V_{OL}$	5.0	0.4	0.8	V	$C_L = 50$ pF
$V_{OLV}$ (Note 7)	Quiet Output Minimum Dynamic $V_{OL}$	5.0	-0.4	-0.8	V	$C_L = 50$ pF
$V_{IHD}$ (Note 7)	Minimum HIGH Level Dynamic Input Voltage	5.0		2.0	V	$C_L = 50$ pF
$V_{ILD}$ (Note 7)	Maximum LOW Level Dynamic Input Voltage	5.0		0.8	V	$C_L = 50$ pF

**Note 7:** Parameter guaranteed by design.

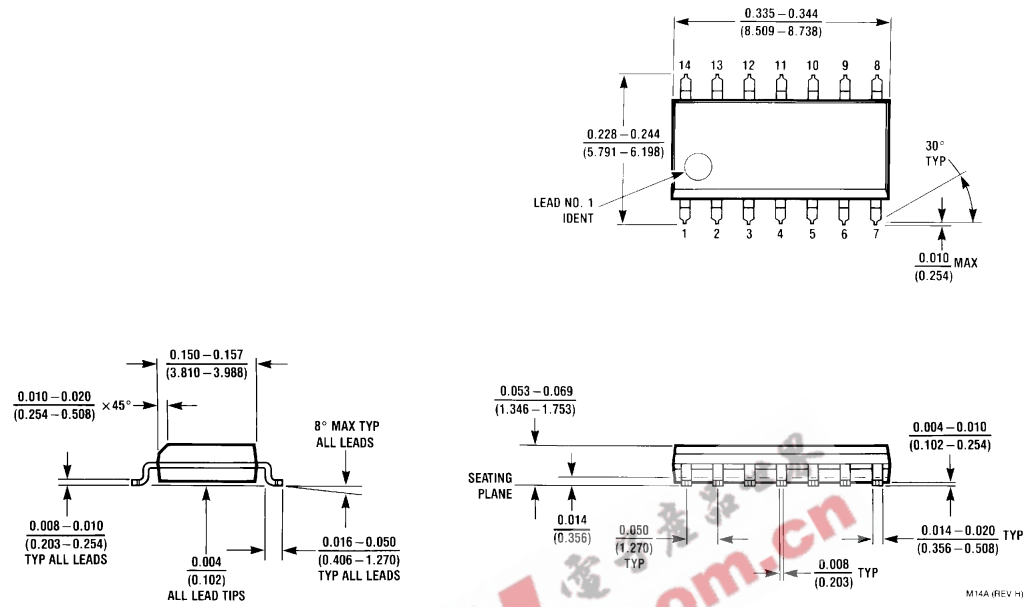
## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	5.0 ± 0.5	5.0	6.9		1.0	8.0	ns	C <sub>L</sub> = 15 pF
t <sub>PHL</sub>			5.5	7.9		1.0	9.0		C <sub>L</sub> = 50 pF
C <sub>IN</sub>	Input Capacitance		4	10		10	pF	V <sub>CC</sub> = Open	
C <sub>PD</sub>	Power Dissipation Capacitance		17				pF	(Note 8)	

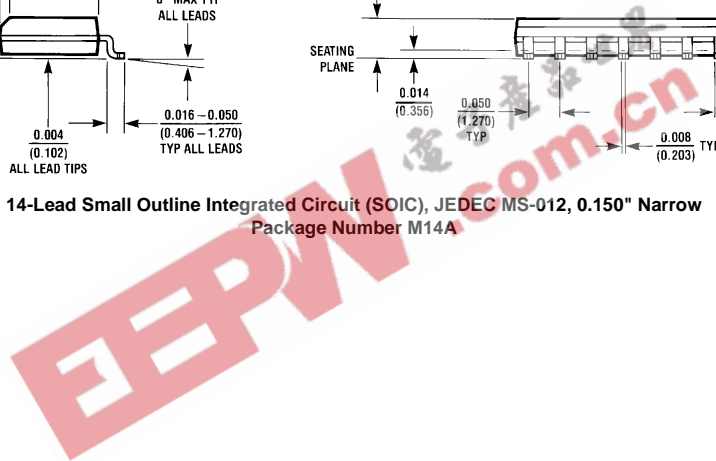
**Note 8:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance, which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I<sub>CC (opr.)</sub> = C<sub>PD</sub> \* V<sub>CC</sub> \* f<sub>IN</sub> + I<sub>CC</sub>/4 (per gate)

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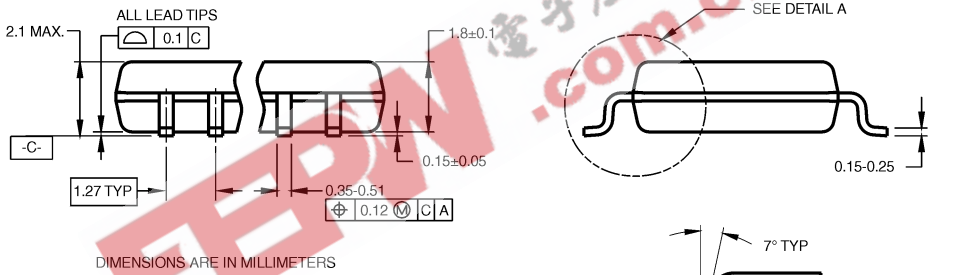
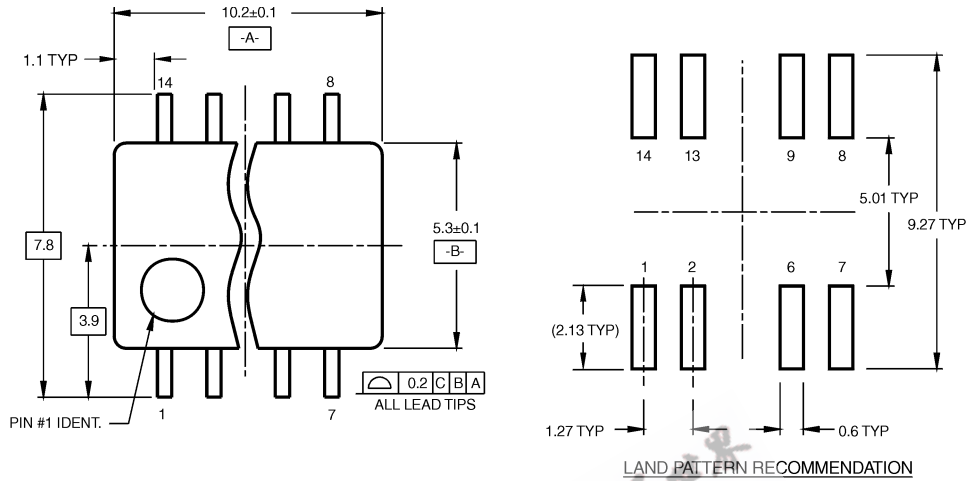
**Physical Dimensions** inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M14A



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

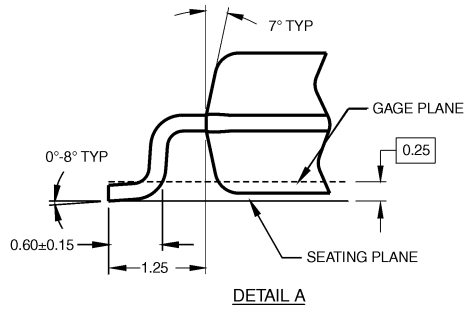


DIMENSIONS ARE IN MILLIMETERS

NOTES:

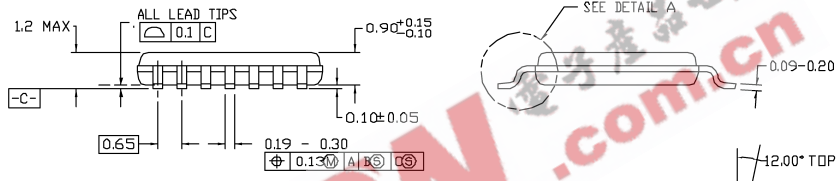
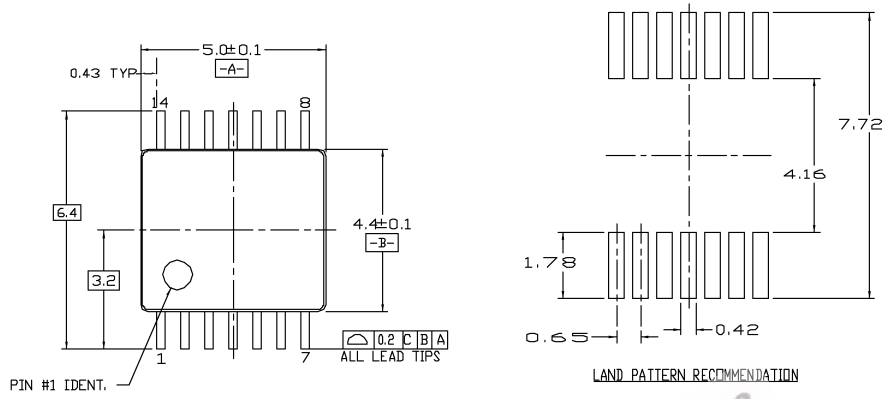
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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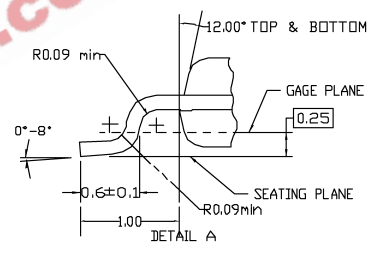


**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

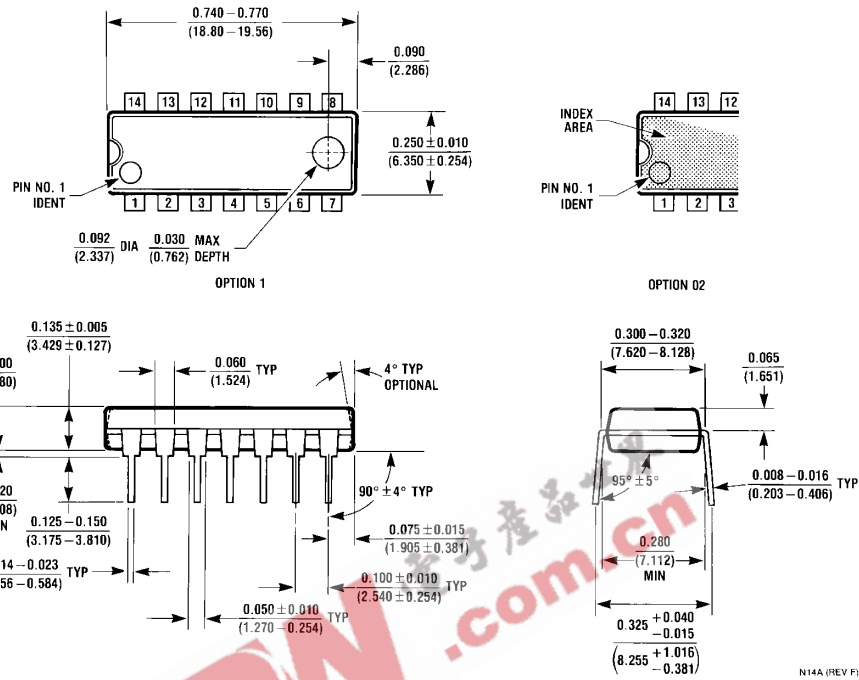


- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153 VARIATION AB, REF NOTE 6, DATED 7/93
  - B. DIMENSIONS ARE IN MILLIMETERS
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
  - D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- MTC14revD



**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

N14A (REV F)

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